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Characterization of CMOS Four Quadrant Analog Multiplier

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ABSTRACT

Real-time analog multiplication of two signals is one of the most important operations in analog signal processing. The design and various analysis of low power, high bandwidth analog multiplier is presented. The multiplier combines the features of both, the Differential structure of Flipped voltage follower cell and Source Follower. This design will improve the multiplier bandwidth by reducing the power dissipation, with low power supply. Simulation results are obtained in 0.35µm, 0.25µm, 0.18µm and 90nm with supply voltages of 1.8v, 1.5v, 0.9v and 0.5v respectively.

Keywords - Analog Multiplier, Four-Quadrant, FVF Differential Structure, Source Follower.

1. INTRODUCTION

In analog-signal processing the need often arises for a circuit that takes two analog inputs and produces an output proportional to their product. Such circuits are termed analog multiplier. So, the ideal output of the multiplier is Vout = Km·VxVy where Km = multiplier gain Unit. Different architecture of multipliers has been designed for different optimization objectives. Analog multiplier seems to be most obvious representative for this class, since it is hard to overestimate the importance of analog multipliers in mixed-signal systems. They are widely used in contemporary VLSI chips for modulation &demodulation, other non-linear operations including division, square rooting as well as frequency conversion. Four quadrant variants may also be used as a phase or with large signal driving, coincidence detectors.

In this paper, authors have discussed a CMOS analog multiplier classified as Voltage mode multiplier with Type IV quadrant, which has single low supply voltage, and is compatible with low-power operation. In order to get a lower power supply and power consumption, concentrating on compact circuit topologies, this circuit cell called "flipped voltage followers" (FVF), used for design since it needs only a supply voltage of $V_{TH} - V_{eff}$, where V_{TH} is the threshold voltage and $V_{eff} = (V_{GS} - V_{TH})$ is the effective gate voltage.

2. PRINCIPLE OF OPERATION

MOS Transistor is an important piece of device used for circuit design. By using drain circuit equation of MOS Transistor which works on saturated range. The relationship of the drain current is given by:

$$I_D = K_N (V_{GS} - V_{TN})^2 \; ; \; V_{GS} > V_{TN} \; , \; V_{DS} \geq V_{GS} - V_{TN}$$

$$I_D = K_P (V_{GS} - V_{TP})^2 \; ; \; V_{GS} > V_{TP} \; , \; V_{DS} \geq V_{GS} - V_{TP}$$

Where, K_N and K_P are the transconductance parameter of NMOS and PMOS, respectively V_{TN} and V_{TP} are the threshold voltages of NMOS and PMOS. V_{GS} and V_{DS} are the gate to source voltage and drain to source voltage respectively.

1.1 SOURCE FOLLOWER

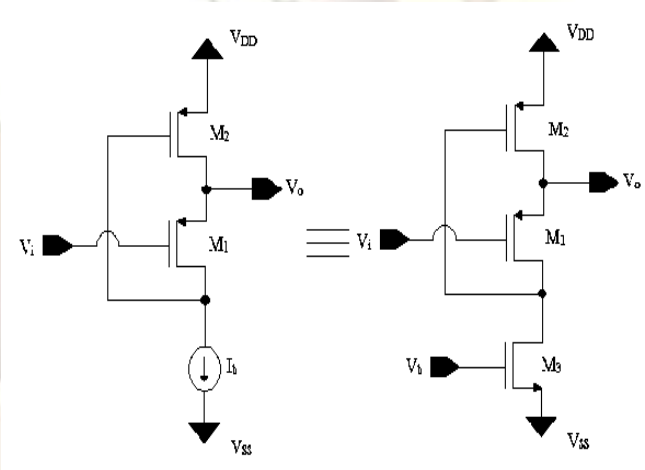

Fig.1. Source Follower

The circuit in Fig. 1 is source follower where the current through transistor M1 is held constant,and not depend on the output current. It could be also described as a voltage follower with shunt feedback. This circuit known as "flipped voltage followers"(FVF). Neglecting body effect and the short-channel effect, V_{GSM1} is held constant, and voltage gain is unity. Circuit is able to source a large amount of current, but its sinking capability is

limited by the biasing current source $I_{b,}$ due to the low impedance at the output node,

$$R_O = \frac{1}{g_{m1} g_{m2} . r_{O1}} \qquad (1)$$

Where, gm_1 and gm_2 are the transconductance of the transistor M_1 and M_2 respectively, and ro_1 is the output resistance.

1.2 FVF DIFFERENTIAL STRUCTURE (DFVF)

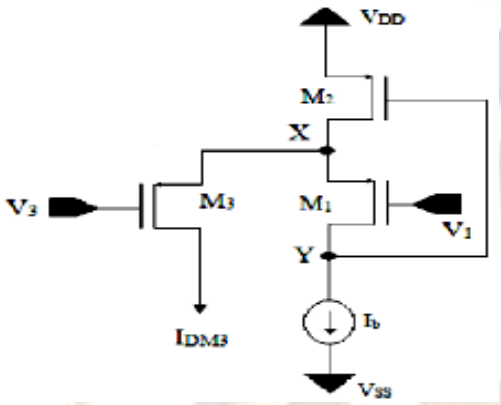

Fig. 2 Differential FVF Structure [3]

The first differential structure based on the FVF cell can be built by adding an extra transistor connected to node X, as it is shown in Fig.2 It will be called the "FVF differential structure (DFVF)".This circuit consists of an MOS transistor (M_3) and the flipped voltage follower (M_1 and M_2).The transistor M3 uses as a simple current to voltage converter. When source terminal voltage of M_3 is equal to $-V_{TN}$ therefore, the current of equation shown as:

$$I_{in} = I_{D3} \qquad (2)$$

Where, $I_{D3} = K_N (V_O - (-V_{TN}) - V_{TN})^2 = K_N V_O^2$.

3 THE COMPLETE MULTIPLIER

Fig.3 shows Four quadrant analog multiplier based on FVF cell consisting of combination of common source amplifier with a differential voltage controlled square rooting circuit. The multiplier circuit formed by common source amplifiers M1-M4 connected pair of differential flipped voltage followers (DFVF), M5- M7 and M8 – M10.

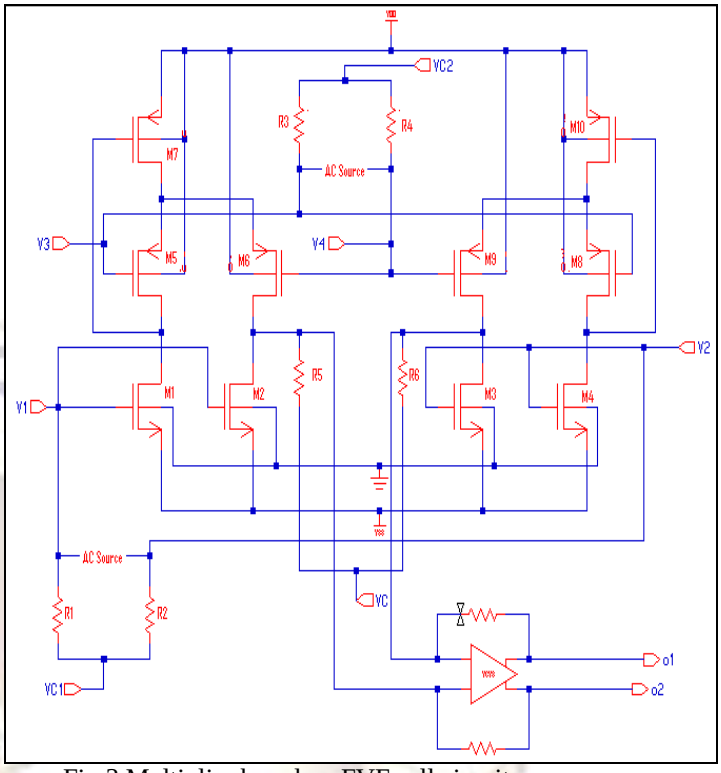

Fig.3 Multiplier based on FVF cell circuit

All transistor work on saturation region, so, the drain currents of M1 to M4 are:

$$I_{D1} = K_n (V_1 - V_{tn})^2 \qquad (3.a)$$

$$I_{D2} = K_n (V_1 - V_{tn})^2 \qquad (3.b)$$

$$I_{D3} = K_n (V_2 - V_{tn})^2 \qquad (3.c)$$

$$I_{D4} = K_n (V_2 - V_{tn})^2 \qquad (3.d)$$

From (a) and (b), we can write

$I_{D1} = I_{D2}$

And from(c) and (d), we can write

$I_{D3} = I_{D4}$

Where, $K_n = 0.5\mu_n C_{ox} W/L$ is transconductance parameter V_{tn} is the threshold voltage of each n-channel MOSFET. And input biasing circuit voltage,

$V_1 = V_{c1} + 1/2\ V_{12}$,

$V_2 = V_{c1} + 1/2\ V_{12}$ so,

$$\sqrt{I_{D1}} - \sqrt{I_{D4}} = \sqrt{I_{D2}} - \sqrt{I_{D3}} = \sqrt{K_n} V_{12} \qquad (4)$$

Where V_{12} is differential input voltage with DC common mode $V_{c1.}$The nonlinear relation can be removed by injecting the output current into square-rooting circuit, which I_{D1} is injected from bias current of the differential-FVF (DFVF).

Similarly, the bias current of the differential-FVF M8-M10 is obtained by injecting I_{D4} into the M8. This results in $I_{D5} = I_{D4}$ and $I_{D8} = I_{D4}$.
In the differential FVF, which operate as a voltage controlled square-rooting circuit.
From Fig.3 we observe that

$$V_3 - V_4 = V_{SG6} - V_{SG5} = V_{SG8} - V_{SG7} \quad (5)$$

By applying the square law relation of a p-channel MOSFET so drain current is: $I_D = K_p (V_{SG} - |V_{tp}|)^2$.
And input biasing circuit voltage
$V_3 = V_{c2} + 0.5\ V_{34}$,
$V_4 = V_{c2} + 0.5\ V_{34}$,
Considering the output nodes, the differential output voltage is $V_{out} = V_{o1} - V_{o2}$. Where,

$$V_{o1} = V_o + (I_{D6} - I_{D2})\ R \quad (6.a)$$

$$V_{o2} = V_o + (I_{D8} - I_{D3})\ R \quad (6.b)$$

Where V_o is reference common mode output voltage and R are load resisters.

$$\cdot V_{out} = 2R\sqrt{Kp}\left(\sqrt{I_{D1}} - \sqrt{I_{D4}}\right)\cdot V_{id2} \quad (7)$$

At last, substituting (6) into (9) so

$$\cdot V_{out} = 2R\sqrt{KnKp}V_{id1}V_{id2} \quad (8)$$

Thus voltage gain can be adjusted by the load resistor and transconductance parameters.

TABLE I
CMOS TRANSISTOR WIDTHS AND LENGTHS IN MICROMETER FOR DIFFERENT TECHNOLOGIES

Transistor	Technology							
	0.35µm		0.25µm		0.18µm		90nm	
	W	L	W	L	W	L	W	L
M1-M4	0.97	0.97	0.69	0.25	0.5	0.5	0.25	0.25
M5, M6, M8, M9	48.6	3.88	24.72	2.77	17.8	2	8.9	1
M7, M10	297.05	3.88	152.77	2.77	110	2	55	1

Proper aspect ratio must be chosen according to the technology used. Table1 shows the widths and length of different transistors depending on the technology chosen.

4 SIMULATION RESULT

The simulation results are obtained for different technologies of 0.35µm, 0.25µm, 0.18µm and 90nm.

TABLE II
DIFFERENT PARAMETERS FOR DIFFERENT TECHNOLOGIES

Parameters	Technology			
	0.35µm	0.25µm	0.18µm	0.90nm
Vdd	1.5	1.3	0.9	0.5
Vc	0.35	0.35	0.35	0.35
Vc_1	0.70	0.70	0.70	0.70
V_{c2}	0.12	0.12	0.12	0.12
R1-R6 (K_{HZ})	4	4	4	4
Rn, Rp(K_{HZ})	20	20	20	20

The DC-transfer characteristic of multiplier based on fvf cell is shown in Fig. 4, 7, 10, 13. Here when V_{12} is input voltage varied from -0.1v to 0.1v with increment of 0.01v and V_{34} is varied from -0.08v to 0.08v with increment of 0.1v.
The application of the Four quadrant multiplier as a balance modulator. The modulation is performed when the input voltage is 0.6v, 300MHz sinusoidal V_{id1} is a carrier signal multiplied with another signal voltage is 0.6v, 25MHZ sinusoidal V_{id2} is modulated signal.
Frequency response of the multiplier topology is shown in Fig. 6, 9, 12, 15. Here the output voltage Vo versus the input voltage V_{12}.

4.1 Simulated waveforms in 0.35µm technology

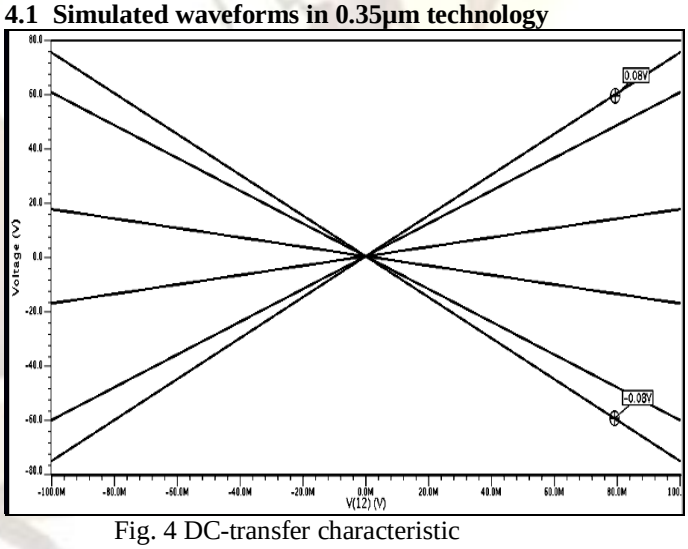

Fig. 4 DC-transfer characteristic

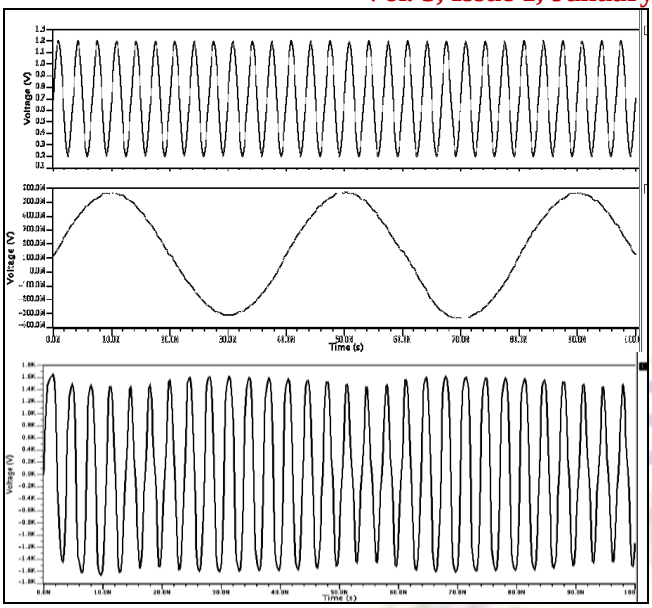

Fig.5Transient response

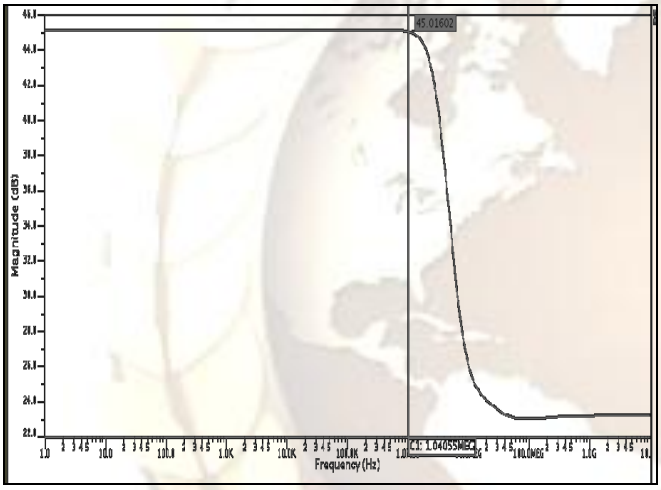

Fig.6 Frequency response

4.2 Simulated waveforms in 0.25µm technology

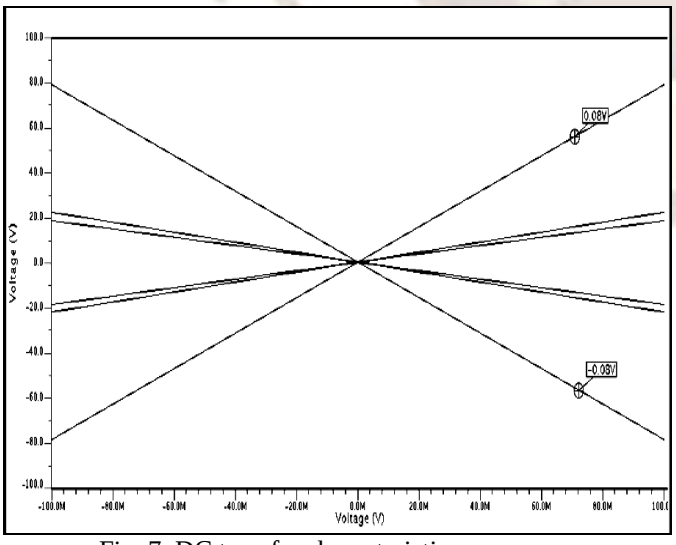

Fig. 7 DC transfer characteristic

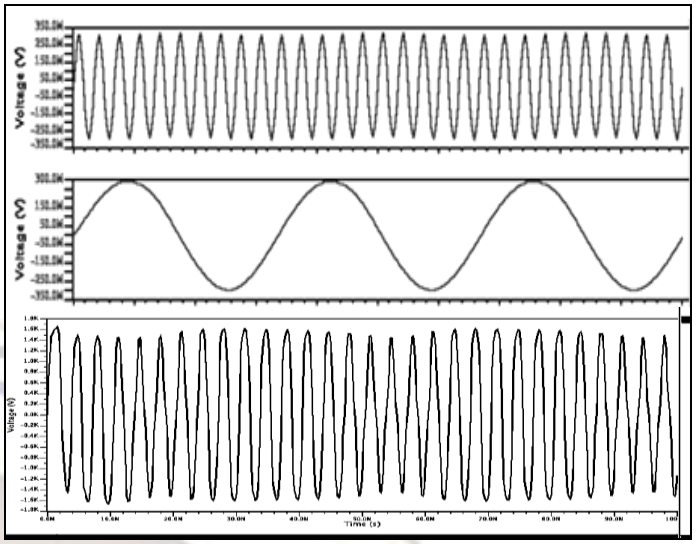

Fig.8 Transient response

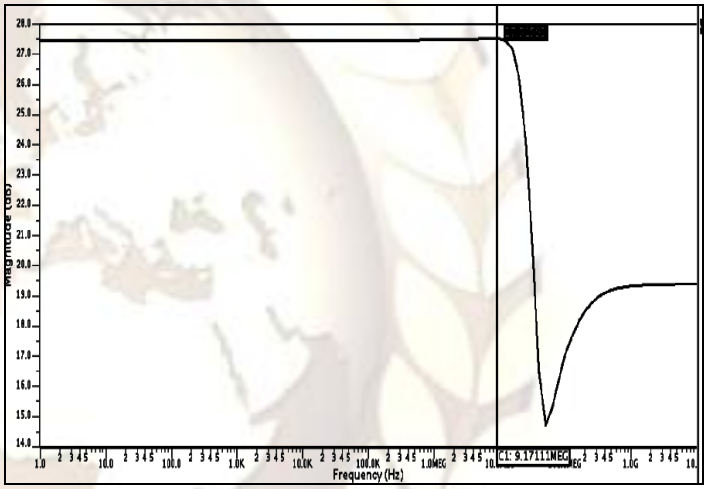

Fig.9 Frequency response

4.3 Simulated waveforms in 0.18µm technology

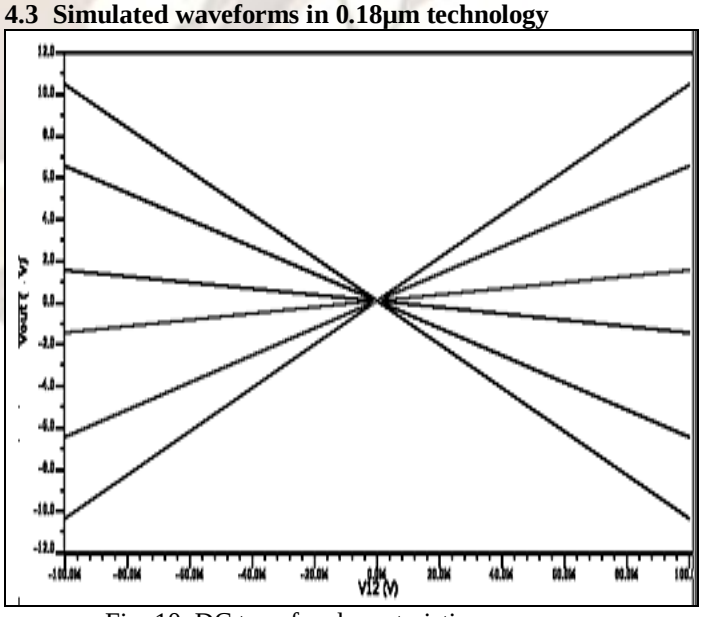

Fig. 10 DC transfer characteristic

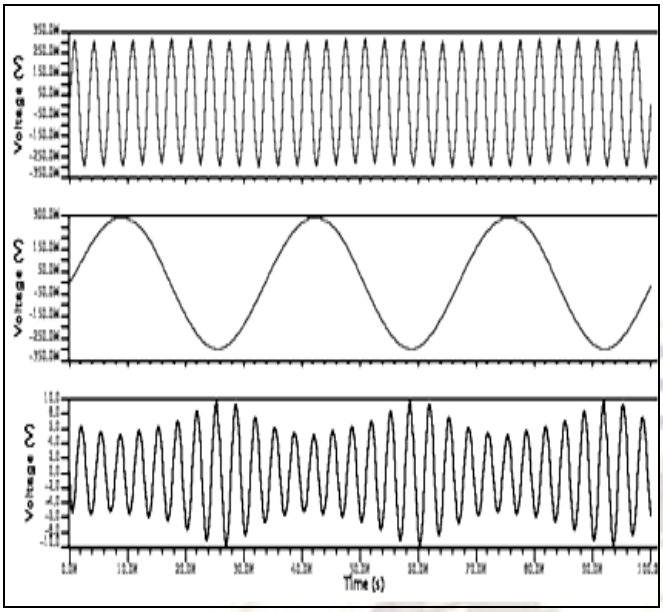

Fig.11 Transient response

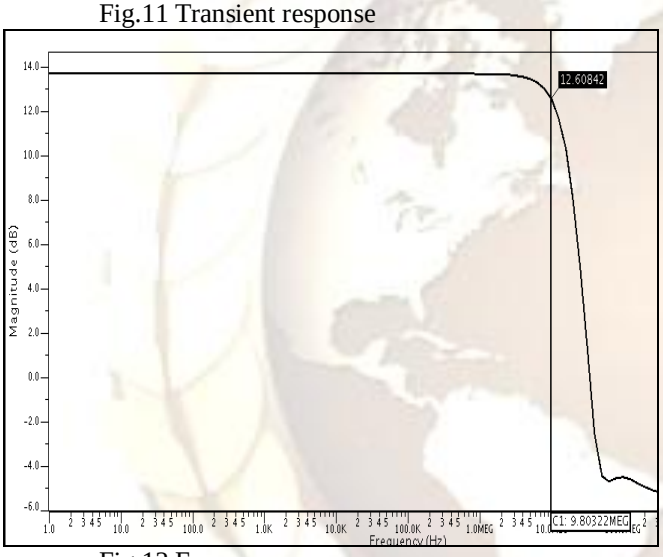

Fig.12 Frequency response

4.4 Simulated waveforms in 90 nm technology

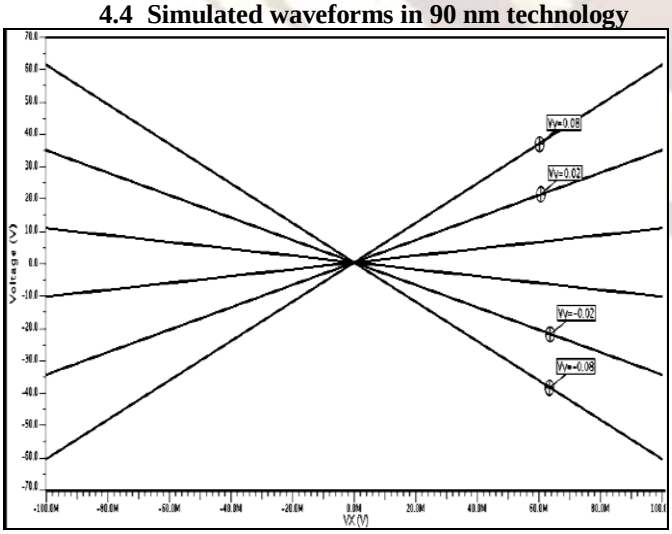

Fig. 13 DC-transfer characteristic

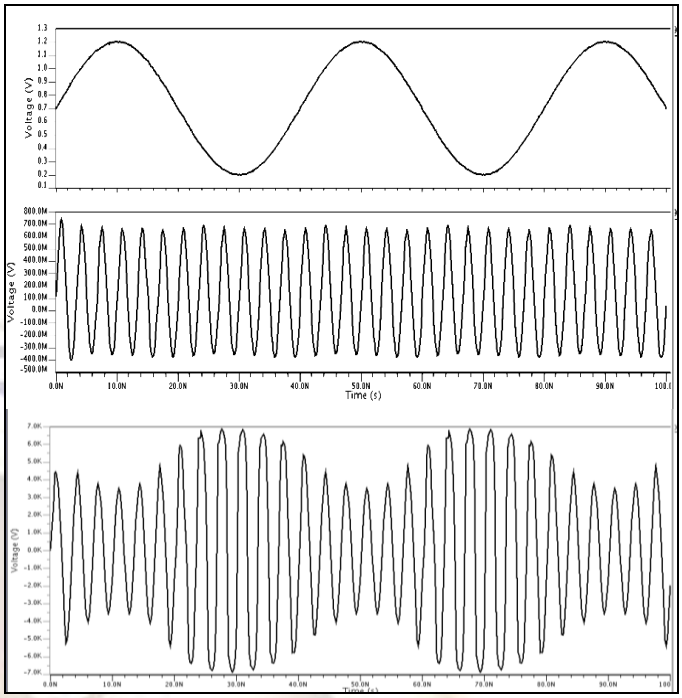

Fig.14 Transient response

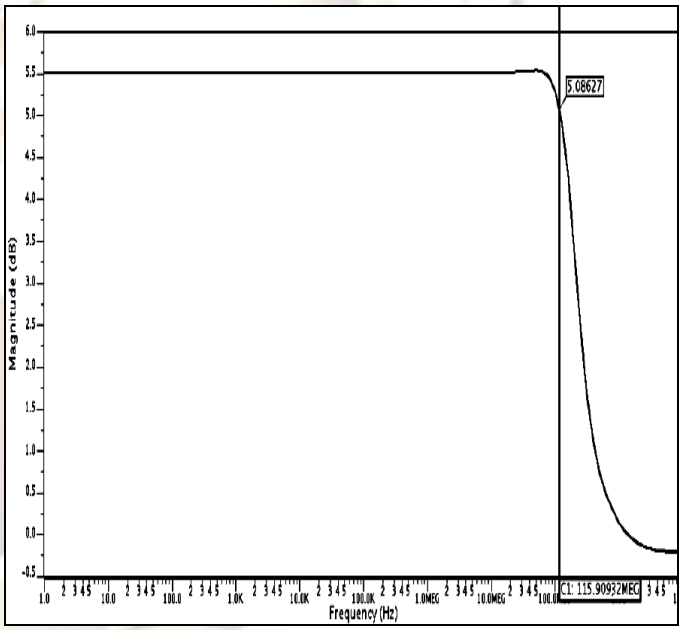

Fig.15 Frequency response

5 CONCLUSION

The simulation results of various characteristics have been presented in this paper in three different technologies 0.35µm, 0.25µm, 0.18µm and 90nm.The comparison of these technologies has been summarized in Table III.

TABLE III
DIFFERENT MEASURED PARAMETERS FOR DIFFERENT TECHNOLOGIES

Parameters	**Technology**			
	0.35µm	**0.25µm**	**0.18µm**	**90nm**
Bandwidth (MHZ)	1.04	9.17	10	115.9
Gain(db)	45.01	27.51	32	50.9
Power Dissipation (mV)	56.06	11.52	28.46	17.87

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