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Delay estimation of a Hierarchical Decoder with the help of Logical Effort and Transistor Sizing

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ABSTRACT

This paper deals with the design of a 2-to-4 hierarchical decoder, designed with the help of a static CMOS logic. The decoders are designed using 180nm technology parameters and are simulated with PSPICE. The 2-to-4 decoders designed are compared with the simulated results on the basis of propagation delay with different branching effort and different load capacitances. The designed decoders are also compared in terms of total power dissipation with different V_{DD} applied. It is found that, a decoder designed by using static CMOS based NAND gates has less propagation delay as compared to the one designed by using static CMOS based NOR gates, this can be verified by theoretical and simulated results. Also, the NAND decoder (3-stage) tends to have low power as compared to a NOR decoder (2-stage).

Keywords: **Capacitances, Hierarchical Decoder, Logical Effort, Propagation Delay, Power Dissipation.**

I. INTRODUCTION

A decoder is a combinational logic circuit that converts binary code data at its input into one of a different number of output lines, one at a time producing an equivalent decimal code at its output.
An N-to- 2^N decoder takes an N-bit input and produces a 2^N outputs. The N inputs represent a binary number that determines which of the 2^N output is uniquely true, [1].
The method of logical effort is an easy way to estimate delay in a CMOS circuit, [2]. It also specifies the proper number of logic stages on a path and the best transistor sizes for the logic gates.
Logical effort is a method to make following decisions [3]:

- It uses a simple model of delay.
- Allows back – of – the – envelope calculations.
- Helps make rapid comparisons between alternatives.
- It emphasizes remarkable symmetries.

With logical effort minimum delay of the path can be estimated by only knowing number of stages, path effort, and parasitic delay without the need to assign transistor sizes. This is superior to simulation where delay depends on sizes and you never achieve certainty that the size selected would offer minimum delay [3].

This paper is summarized as follows: Section II gives a brief introduction about computation of branching effort. Section III consists of proposed work and comparison of results.

II. BRANCHING EFFORT

To account for branching between the stages of a path, an effort was introduced, [3]. This branching effort 'b' is the ratio of the total capacitance seen by stage to the capacitance on path.

$$b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}}$$

The path branching effort 'B' is the product of the branching efforts between stages.

$$B = \prod b_i$$

The path effort 'F' is defined as the product of path logical, electrical and branching effort of the path.

$$F = GBH$$

Where: G – path logical effort, H – path electrical effort, B – path branching effort.

If a path has N stages and each bears the same effort then stage effort must be:

$$f = F^{1/N}$$

Thus minimum possible delay of an N-stage path with path effort F and path parasitic delay P is,

$$D = NF^{1/N} + P$$

This is the key result of logical effort.

Logical effort generalizes to multistage logical networks, [4]. Here, we will analyze dependence of branching effort on the propagation delay of a 2-to-

4 decoder designed by using NAND and NOR gates respectively and comparison of their results.

A. Effect of branching effort on delay of a 2-to-4 NAND based decoder:

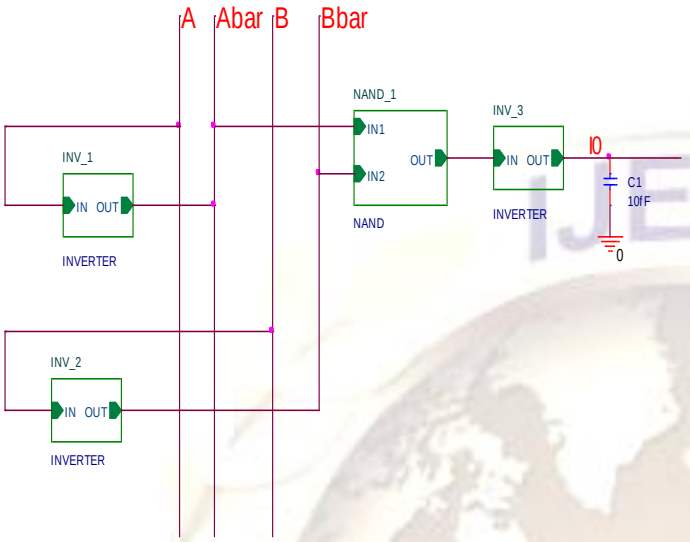

Fig1. 2-to-4 Decoder designed using static CMOS based NAND gates

Considering the selected on path of a 2-to-4 decoder as shown in Fig1, we can easily compute the delay of this path. This analysis is same for the other paths of a decoder.

Here, we have taken C_L = 10fF, N = 3 (number of stages in a decoder), P = 4. Let us assume C_{in} = 1fF, so

$H = C_L / C_{in} = 10$

G = 4/3 (path logical effort of a NAND gate, [2])

B = 2

F = GBH = 26.67

$f = F^{1/3} = 2.98$

$D = NF^{1/N} + P = 12.94$

This is the estimated delay theoretically. It can be concluded that when branching effort is increased then delay is also increased. This has been summarized and depicted in the following table and graph resp.

BRANCHING EFFORT	ESTIMATED DELAY
2	12.94
4	15.59
6	17.30
8	18.67
10	19.83
12	20.83

Table1. Variation of delay w.r.t branching effort of a 2-to-4 NAND based decoder [Fig1.]

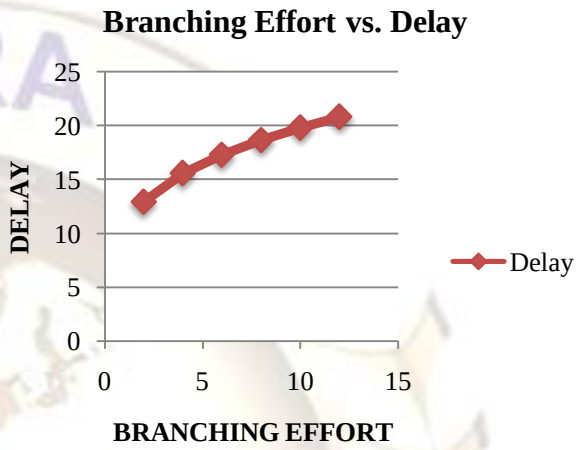

Fig2. Graph showing relation between branching effort and delay as shown in table1.

B. Effect of branching effort on delay of a 2-to-4 NOR based decoder:

Consider the selected on-path of 2-to-4 nor based decoder as shown in fig3; we can easily compute the delay of this path. This analysis is same for the other paths of a decoder.

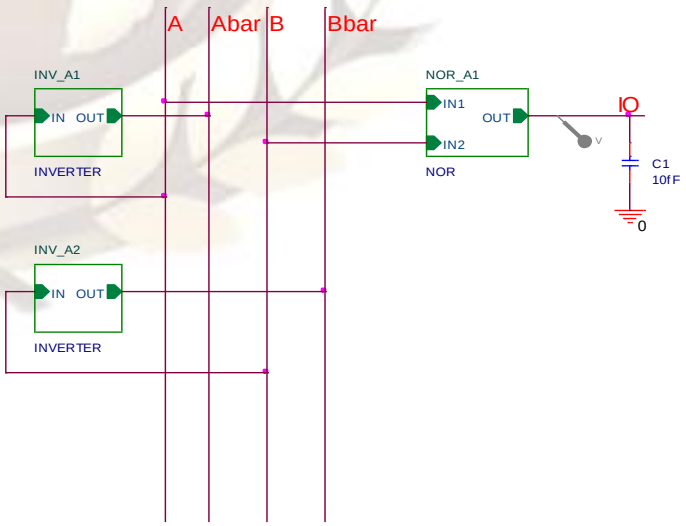

Fig3. 2-to-4 Decoder designed using static CMOS based NOR gates

Here, we have taken C_L = 10fF, N = 2 (number of stages in a decoder), P = 3. Let us assume C_{in} = 1fF, so

$H = C_L / C_{in} = 10$

G = 5/3 (path logical effort of a NOR gate, [2])

B = 2

F = GBH = 33.33

$f = F^{1/2} = 5.77$

$D = NF^{1/N} + P = 14.54$

This is the theoretically estimated delay of a NOR based 2-to-4 decoder. Now from the table2, we can conclude that when branching effort is increased, the propagation delay also increases. This is depicted in the following graph shown in Fig4.

BRANCHING EFFORT	ESTIMATED DELAY
2	14.54
4	19.32
6	23.00
8	26.09
10	28.82
12	31.28

Table2. Variation of delay w.r.t branching effort of a 2-to-4 NOR based decoder [Fig3.]

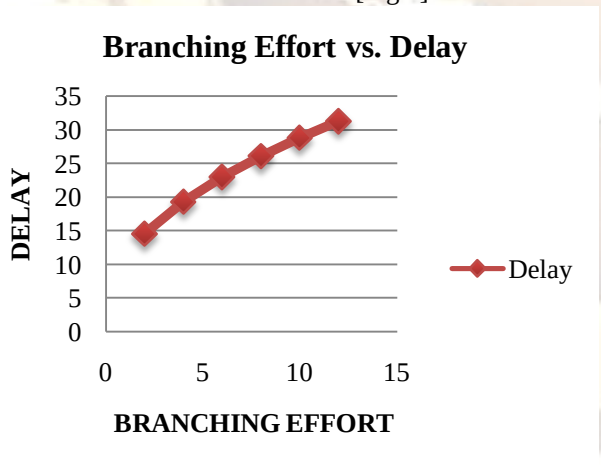

Fig4. Graph shows relation between branching effort and delay as shown in table2.

III. PROPOSED WORK

Here, we have simulated both the 2-to-4 decoders by varying load capacitance, C_L and by varying voltage supply, V_{DD}. Delay depends on the number of input applied to the gate and the number of stages in the multistage network. As the number of input is reduced delay is reduced. The increase in V_{DD} supply will lead to an increase in switching speed but this will also increase the power dissipation, [5]. Considering only one selected path all the calculations are performed. All the other paths of a 2-to-4 decoder will give the same results as of the path taken under consideration. Our proposed work is being explained in two sections A and B.

A. Effect of load capacitance on delay of a 2-to-4 decoder.

The propagation delay of the 2-to-4 NAND based decoder [Fig1.] has been estimated by varying C_L. Here, we have used 180nm technology in consideration. The time constant used for calculating the theoretical delay is 15ps [2]. The analysis is done with the input supply voltage of 0.8V and the power dissipation calculated is found to be P_D = 2.30E-09 W. Both the simulated and theoretical delays are depicted below in the following table and graph:

LOAD CAPACITANCE C_L (fF)	THEORETICAL DELAY (ns)	SIMULATED DELAY (ns)
10	0.194	0.141
50	0.289	0.308
100	0.349	0.446
250	0.453	1.028
500	0.555	1.902

Table3. Variation of delay w.r.t load capacitance of a 2-to-4 NAND based decoder [Fig1.]
This table3 proves that as the load capacitance is increased the propagation delay is also increased.

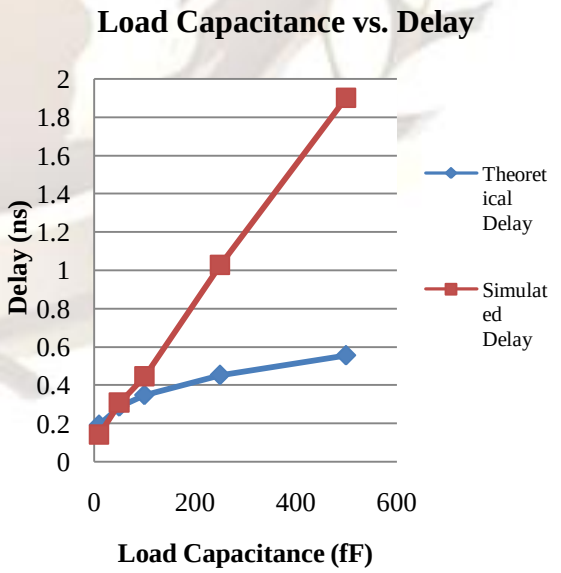

Fig5. Graph showing relation between delay and load capacitance of a 2-to-4 NAND based decoder [Fig1.]

Similarly, the propagation delay of the 2-to-4 NOR based decoder [Fig3.] has been estimated by varying C_L. Also, same technology parameters have been taken under consideration. The power dissipation calculated is found to be P_D = 2.05E-09 W. Both the simulated and theoretical delays are depicted in the following table and graph:

LOAD CAPACITANCE C_L (fF)	THEORETICAL DELAY (ns)	SIMULATED DELAY (ns)
10	0.218	0.209
50	0.432	0.385
100	0.592	0.734
250	0.911	1.427
500	1.269	2.202

Table4. Variation of delay w.r.t load capacitance of a 2-to-4 NOR based decoder [Fig3.]

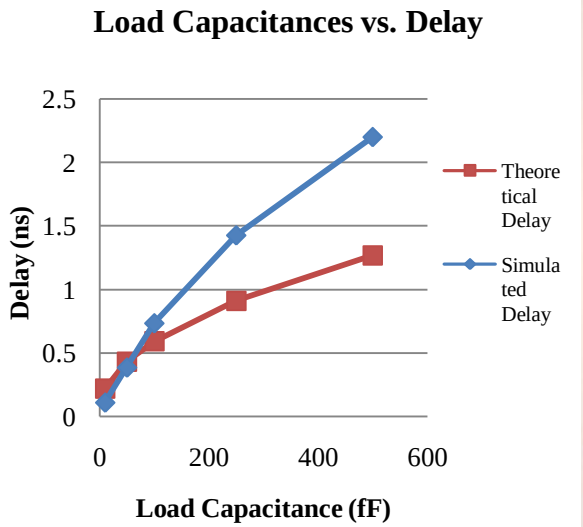

Fig6. Graph depicting relation between delay and load capacitance of a 2-to-4 NOR based decoder [Fig3.]

B. Effect of V_{DD} on delay and power dissipation of a 2-to-4 decoder.

The propagation delay decreases with an increase in V_{DD} but as a penalty the power dissipation increases. The propagation delay and power dissipation of the 2-to-4 NAND based decoder [Fig1.] has been estimated by varying V_{DD}. Here, 180nm technology parameters are taken under consideration. The analysis is done by keeping C_L = 10fF in both the decoders.

INPUT SUPPLY, V_{DD} (V)	DELAY, T_P(ns)	POWER DISSIPATION (W)
0.5	0.477	1.14E-09
0.8	0.141	2.30E-09
1.0	0.079	3.36E-09
1.4	0.064	6.38E-09
1.8	0.058	1.11E-08

Table5. Variation of delay and power dissipation w.r.t V_{DD} of a 2-to-4 NAND based decoder [Fig1.]

Similarly, the propagation delay and power dissipation of the 2-to-4 NOR based decoder [Fig3.] has been estimated by varying V_{DD}.

INPUT SUPPLY, V_{DD} (V)	DELAY, T_P(ns)	POWER DISSIPATION (W)
0.5	0.844	1.02E-09
0.8	0.209	2.05E-09
1.0	0.144	2.99E-09
1.4	0.115	5.68E-09
1.8	0.097	9.92E-09

Table6. Variation of delay and power dissipation w.r.t V_{DD} of a 2-to-4 NOR based decoder [Fig3.]

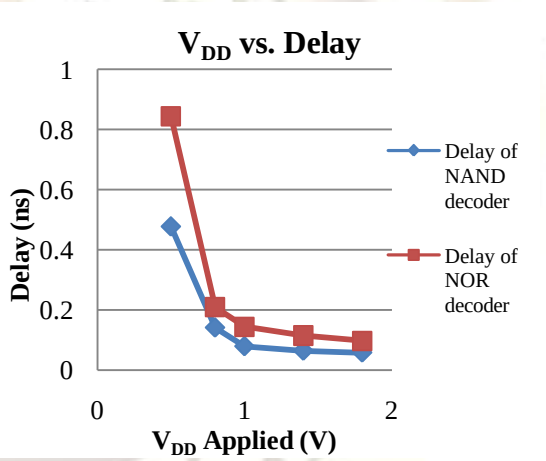

Fig7. Graph between delay w.r.t V_{DD} of both the 2-to-4 NAND and NOR based decoders.

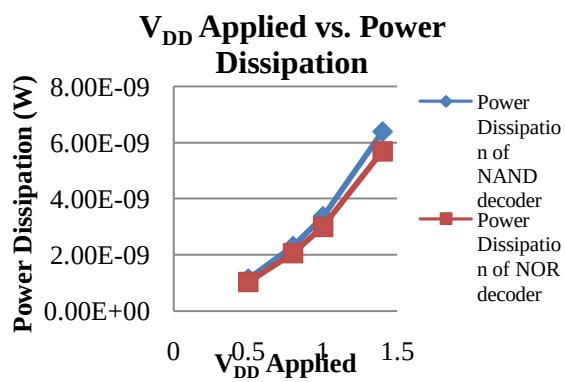

Fig8. Graph between power dissipation w.r.t V_{DD} of both the 2-to-4 NAND and NOR based decoders.

IV. CONCLUSION

From the study of logical effort, variation of load capacitance and V_{DD}, we come to a conclusion that static CMOS based decoder designed with NAND gates having 3 stages have less propagation delay (theoretically and simulated delay) and less power dissipation as compared to the one designed using NOR gates having 2 stages. It is also concluded that with the increase in branching effort and load capacitance the propagation delay increases but with increase in V_{DD} delay decreases.

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