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Computer investigation of a sine and cosine based phase-locked loop for single phase grid connected inverter

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ABSTRACT

This paper presents a new approach for PLL for synchronization with the public grid phase and frequency of grid-connected single phase inverter. The approach uses trigonometric transformations of the inverter output voltage and the grid voltage. The proposed mathematical model is then studied by means of computer simulation for different voltage amplitudes of the grid voltage as well as the inverter output voltage.

Keywords–**grid-connected inverter, PLL, trigonometric transformations**

I. Introduction

Due to the constant decrease of conventional fuels, the use of renewable distributed energy sources constantly increases. These systems are interfaced by power electronic converters in order to connect to the utility grid. Different standards and requirements are applicable to these systems in order to maintain grid energy quality. That is why a very good synchronization between the power system of the renewable energy source and the utility grid at the point of common coupling (PCC) is needed.

Widely used traditional synchronization methods of the control system and the grid voltage are algorithms based on the phase-locked loops (PLL). Various PLL techniques have been proposed and are used because of the efficiency and robustness of the algorithm, but all of them contain the basic PLL blocks- phase detector (PD), loop filter (LF) and voltage-controlled oscillator (VCO) [1], [2]. The block diagram of such a PLL is presented in Fig.1 Major difference in the different proposed PLLs is the phase-detector block.

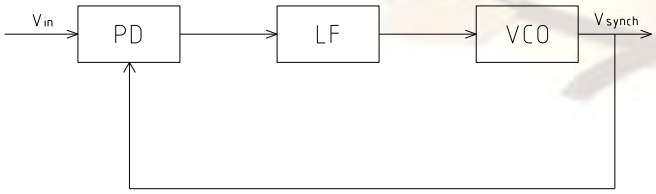

Fig.1 Block diagram of PLL

One of the state-of-the-art used PLL techniques is the synchronous-reference-frame (SRF) phase-locked loop (SRF-PLL) which can estimate instantaneous grid voltage phase [2], [3]. Improved version of the SRF-PLL is the proposed in [4] adaptive synchronous-reference-frame PLL which purpose is to reject disturbances introduced by the voltage harmonic distortion. The system is based on adaptive filtering of the harmonics of the grid voltage projected to the SRF in case of unbalanced grid or distortion in the grid voltage.

Another method for stability in the adaptive process is the positive-negative sequence of grid components proposed in [5] or the fundamental frequency detection of the utility grid voltage in [6].

New approach recently presented uses frequency-locking loop instead of traditionally used phase-locking loop. Its main idea is based on the operation of the PLL presented in [6] e.g. adaptive filter.

This paper presents another approach for PLL technique for synchronization of single-phase on-grid inverter with the public grid. Its PD block operation is based on sinus and cosines transformations of the voltage of the inverter and a reference voltage signal which is the grid voltage.

This paper is organized as follows: Section II described the sinus and cosines PLL for single-phase on-grid inverter. Section III presents the simulation results of the proposed algorithm of PLL and Section IV is the conclusion.

II. Operation

The operation scheme of the proposed PLL is synthesized on the following assumption -the input voltage contains only sinusoidal component or $v_{in} = V_m \sin\theta$.;the output voltage is obtained as $v_{sync} = 1.\sin\hat{\theta}$.

Then the following two trigonometric equations are used:

$$\sin\theta \,.\cos\hat{\theta} = \frac{1}{2}\left[\sin(\theta+\hat{\theta}) + \sin(\theta-\hat{\theta})\right] \quad (1)$$

$$-\cos\theta \,.\sin\hat{\theta} = -\frac{1}{2}\left[\sin(\theta+\hat{\theta}) - \sin(\theta-\hat{\theta})\right] \quad (2)$$

If we make the sum of (1) and (2) we can obtain the following result $\sin(\theta-\hat{\theta})$.

III. Simulation results

Computer simulation of the mathematical model is done with the software product PSIM. The simulation model is presented in Fig.2. The obtained sine $V_{inM}\sin(\theta-\hat{\theta})$ is compared to 0 and the result

is passed to the PI regulator. Thus the output synchronized signal has amplitude 1. The operation of the method is studied in three different cases: with unity value of the input voltage amplitude, with voltage amplitude value equal to 5V and voltage amplitude value equal to 10V.

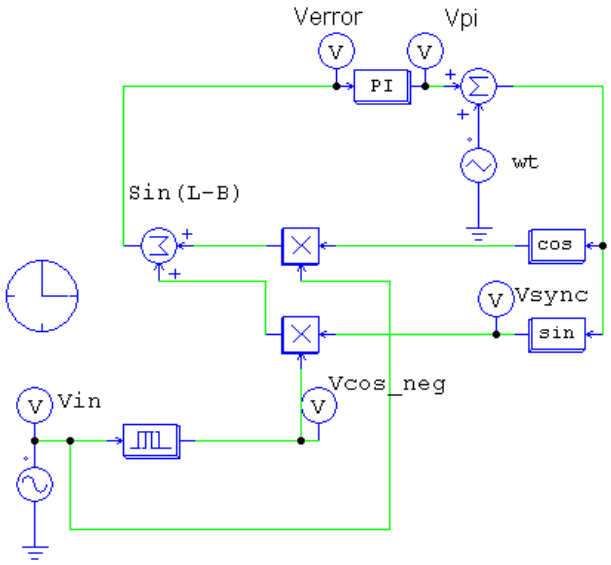

Fig. 2. Simulation model of the proposed sine and cosine PLL for single phase grid connected inverter

3.1. Simulation results with input voltage $V_{in} = 1V$

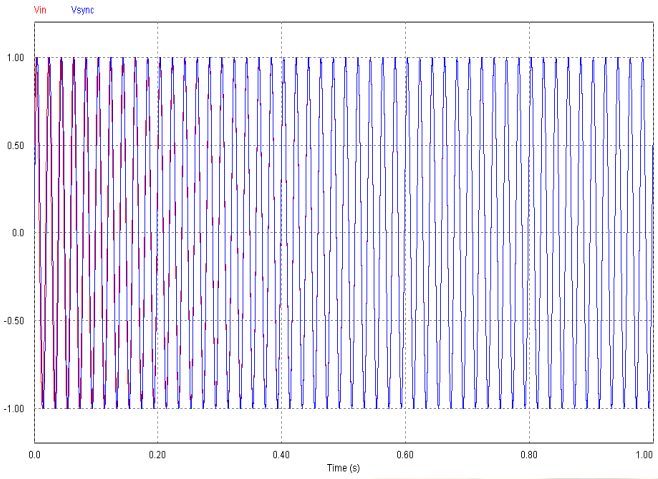

Fig.3. Simulation results for the operation of the PLL with unity input voltage – input voltage and synhronized voltage. The time span is (0,1s)

Fig.3 to Fig 7 display the simulation results for the operation of the PLL with unity input voltage. In Fig.3 one can observe the process of synchronisation for period of 1s.

In Fig.4 and Fig.5 one can observe the same operation of the PLL but devided into two figures for two time periods – from 0-400ms and from 400-800ms. This way it is easy to see that the output signal is synchronized with the input signal at the time t=150ms. After this moment both signal have the same phase constants and angular frequencies.

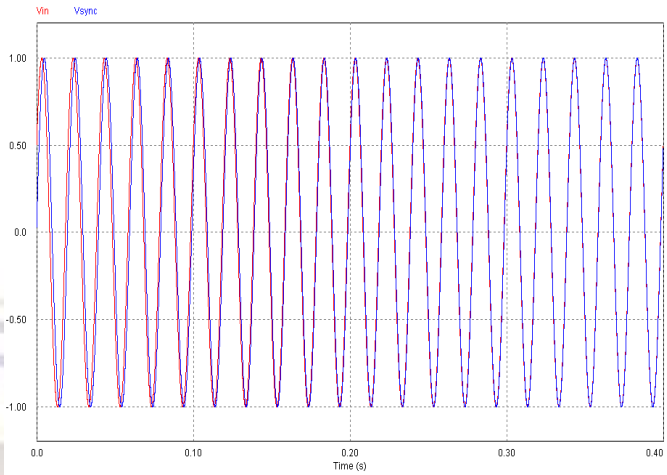

Fig.4. Simulation results for the operation of the PLL with unity input voltage – input voltage and synhronized voltage. The time span is (0,400ms)

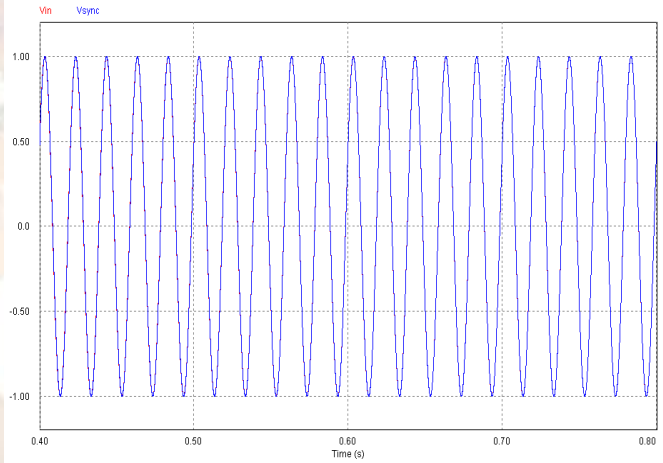

Fig.5.Simulation results for the operation of the PLL with unity input voltage – input voltage and synhronized voltage. The time span is (400ms,800ms)

3.2. Simulation results with input voltage$V_{in} = 5V$

Fig.6. displays the simulation results for the operation of the PLL with $V_{in} = 5V$ – input voltage and synhronized voltage. The time span is (0,100ms). The synhronization is within two periods of the grid voltage.

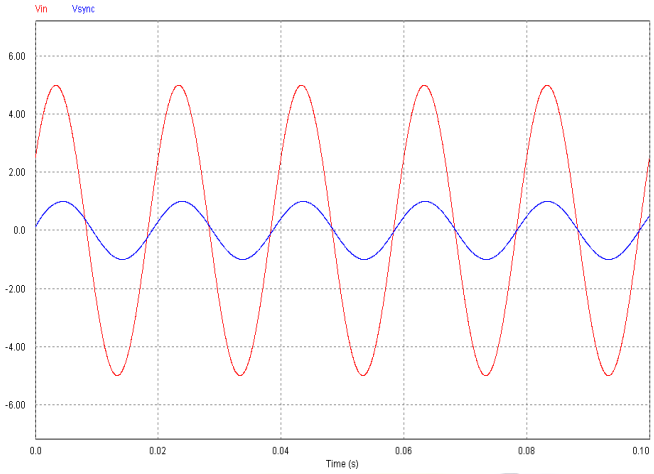

Fig.6.Simulation results for the operation of the PLL with $V_{in} = 5V$ – input voltage and synhronized voltage. The time span is (0,100ms)

3.3. Simulation results with input voltage$V_{in} = 10V$

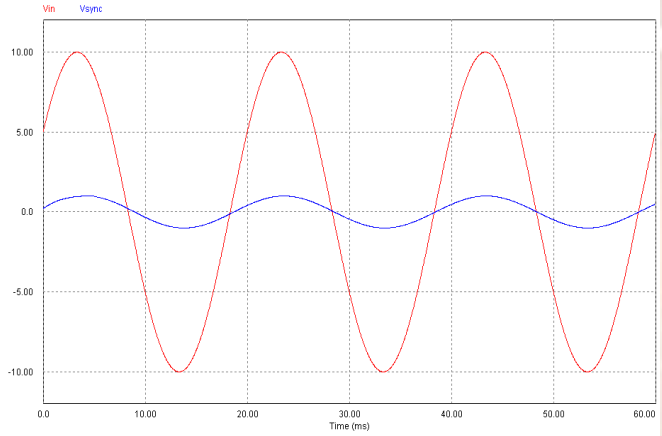

Fig. 7. Simulation results for the operation of the PLL with $V_{in} = 10V$ – input voltage and synhronized voltage. The time span is (0,60ms)

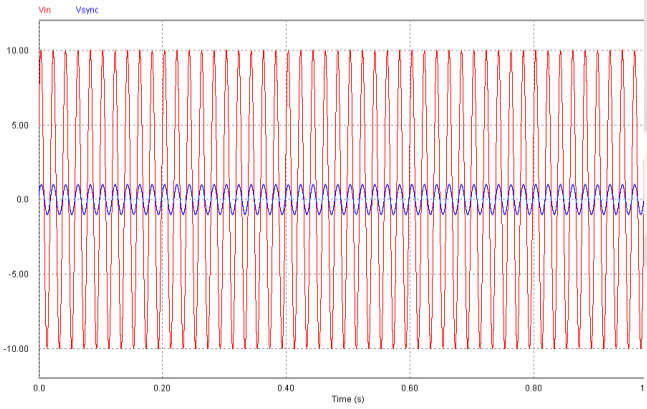

Fig.8. Simulation results for the operation of the PLL with $V_{in} = 10V$ – input voltage and synhronized voltage. The time span is (0,1s)

Fig.7. and Fig.8 display the simulation resultsfor the operation of the PLL with $V_{in} = 10V$ – input voltage and synhronized voltage. The time span is (0,60ms) for Fig.7 and (0,1s) for Fig.8. The synhronization is within a period and a half of the grid voltage

IV. Conclusion

Based on the presented results of the computer simulation above we can conclude that the proposed PLL technique achieve excellent results in the synchronization of the both signals. We can observe that the bigger the amplitude of the input voltage is the faster the synchronization is done- for $V_{in} = 1V$ the synchronisation is done for 150ms, for $V_{in} = 5V$the synchronisation is done for 40ms and for $V_{in} = 10V$the synchronisation is done for 28ms. We recommend during the practical realization to use an input signal with amplitude of 10V which in case of fluctuation of the grid voltage by $\pm 10\%$ is going to assure the synchronization for a time approximately equal to the duration of one and a half period. It is necessary of course to take into account the acceptable input voltage for the elements used for the realization.

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