Adaptive body biasing process compensation techniques for Digital circuit

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ABSTRACT

The present invention relates generally to the integrated circuits(ICs) & in particular to process, voltage & temperature(PVT) variations in an ICs. PVT variations are critical factor that hamper performance of Ics forexample PVT variations can result in a change in setup &hold times of synchronous circuits. Different components of asynchronous circuit are driven by a common system clock. Therefore any change in setup or hold times corresponding to any one component causes an erroneous circuit ouput.one technique to reduce PVT variations in a circuit isbased on sensing the variations in the circuit &then taking the appropriate action to reducethese variations.

Keywords: PVT compensation,Adaptive body biasing.

INTRODUCTION

In this era of ultra large scale integration for a chip to be efficient , the I/O structures requires the circuit design expertise along with the knowledge of processes in detail. It is the I/O element which finally interfaces with the core signal to the off chip environment. The i/o cells are placed on the periphery of chip along with supply cells, corners & fillers. The supply for the core is separated from supply of I/O's because the noise that arise at the switching of the large output buffer .PAD is basically a sandwitch of various metal layers from where user can either receive the output or apply the input. The present work describes some of the basic design considerations for I/O pads. Wherever possible, design option for smaller area ,low power &high speed has been comprehensively dealt with. The emphasis is on having an idea of the various circuit elements involved in an I/O library &an understanding of the behavior & their performance & finally an optimized design is proposed for 3.3V tolerant bidirectional I/O.

2. I/Os: problems & solutions

Main problems occur in I/Os are Latchup,Electrostatic discharge, electromigration& simultaneous switching noise.

2.1 LATCH UP

Latch-up is a failure mechanism of CMOS integrated circuits characterized by excessive current drain coupled with functional failure, parametric failure and/or device destruction.latch-up is an-undesirable but controllable phenomenon.
This Latchup may be prevented in two basic ways:• Latchup resistant CMOS process• Layout technique.[16]

2.2 ELCTROSTATIC DISCHARGE

Electrostatic discharge is a subclass of the failure causes known as electrical overstress (EOS). The ESD events have four major stages: (1) charge generation (2) charge transfer (3) charge conduction (4) charge induced damage.There are two basic ways that circuits are protected: 1) Improve the unprotected elements 2) Add additional circuit elements to divert the charge and clamp the voltage most circuits use a combination of these three techniques.

2.3 ELECTROMIGRATION

Electro migration refers to the gradual displacement of the metal atoms of a conductor as a result of the current flowing through that conductor. Electromigration can be prevented by:1) Proper design of the device 2) Good selection and deposition of the passivation

2.4 SIMULTANEOUS SWITCHING NOISE (SSN):

This Switching Noise is called Simultaneous Switching Noise (SSN).SSN is studied byFeiYuan, Ph.D, P.Eng[8] and discussed lot of methods to reduce it.SSN Reduction Techniques-Separate power and ground pins and pads for analog and digital circuits whenever possible.
Corner pads will have long bond wire and there inductance is very high.

3. DESIGN SPECIFICATION

The specifications are a set of conditions and functionality which are required by the customer. For a designer it is necessary to observe specifications properly and then provide optimized solution. The design must be ensured to work under the process, temperature and Voltage variation.Here by the design presented ensured to work under type process, temperature variation from 0°C to 50°C , core supply variation from 1.1 to 1.2 and VDDE variation from 3.0 V to 3.6 V. Other specifications are delay, frequency of operation, VIL and VIH

levels. These specifications are defined separately for the input and output path.

3.1 DESIGN OPTIMIZATION

The designer has to ensure that the design is efficient as well as cost effective. The cost of production of a chip is much more expensive then to design. It is necessary to optimize area so that production in each batch increases thereby reduction in cost. Power consumption is also very important issue. There are some important parameters among which we have to compromise during the design: Area, power consumption, delay, speed, etc. Hence by taking care of all these parameters we have to provide an optimized design.

3.1.1 DECISION OF W/L RATIO

Area of a chip is basically determined by the (W/L) ratio of transistors. we have taken transistor model from the Linear Technology 130nm technology and then with suitable biasing simulated the ckt and plots are obtained. According to application specific, we will decide the lengths if there is the issue of leakage current then we have to choose the length according to the plot of leakage current wrt length.

3.1.2 SPEEDS VERSUS AREA TRADE-OFF

The speed of a circuitry is determined by the switching response of the circuit. The rise time and fall time of output determines how fast the circuit is operating. Faster the circuit lesser time it will take to settle. The basic cause of the rise time and fall time is the parasitic offered by the circuit.

3.1.3 DESIGN AND OPTIMIZATION TECHNIQUES

The physical design is a design process which is an intermediate between circuit design and circuit on silicon. During the physical design we use different polygon layers which represent the different layers on the silicon. By using these layers a schematic is transformed into layout which is used later for mask preparation during fabrication process. So layout is a heart of all over the circuit design because it transfers the circuit into real world. After the layout design we check it for certain rules known as DRC (Design Rule Check) and LVS (Layout versus Schematic) check. When our layout passesboth these checks then we extract netlist from the layout. By simulating this postlayoutnetlist we verify our results, the dc results will remain same but there may be some changes in transient results due to the parasitics .

4. ADAPTIVE BODY BIASING

Adaptive Body Bias (ABB) involves recovering dies impacted by process variations through post silicon tuning.ABB is a dynamic control technique used to tighten the distribution of maximum operational frequency and the maximum leakage power,in the presence of within die(WID) variations

5. RESULT & ANALYSIS

Output Buffer output slope can be adjusted through compensation technique. Either by change in compensation codes or by adjusting proper substrate biasing voltage. Here in this project I am trying to adjust output slope which is affected by process variation through substrate biasing control mechanism. Adaptive biasing technique used to control the output slope of buffer. Hereby we are able to design output path having a compensated output slope under all PVT conditions. Using feedback signals from I/O PAD slew rate control is also achieved. LTSPICE simulation results are shown here.

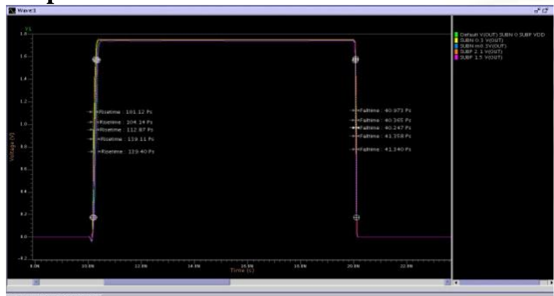
Wave form	SUBP=1.8 V	SUBP=2.1 V	SUBP=1.5V
P Buffer-Rising Wave form	61.159ps	60.281ps	63.348ps
P Buffer-Falling Wave form	90.354ps	78.139ps	116.5ps
	SUBN=0.0	SUBN=0.3 V	SUBN=-0.3V
N Buffer-Rising Wave form	406.7ps	388.06ps	416.79ps
N Buffer-Falling Wave form	34.236ps	32.779ps	39.042ps

N PRE-BUFFER PULSE

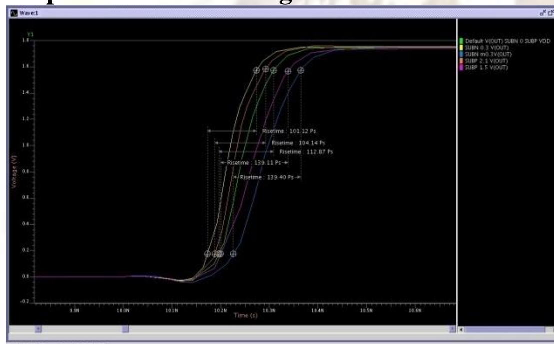
N Pre-buffer Rise

Simulation Waveform of Output Buffer

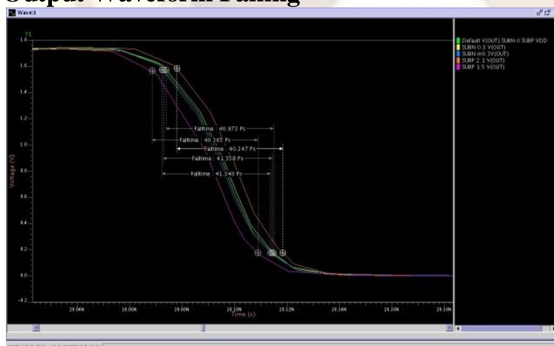
Output Waveform Pulse:



Output Waveform Rising



Output Waveform Falling



CONCLUSION:

Due to change in Substrate Voltage Slope of the output Curve changesIncrease inSubstrate Bias Voltage □ Decrease in Rise (tr) and Fall (tf) time of output waveform. The Complete design of the compensated circuit for an I/O buffer is presented with the cost of area and process mask generation time. The system will work at hundreds of MHz and presents same quality of output signal and hence reduces the noise encounters due to change in process design.

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