Srinivas Dasam, Dr. B.V.Sanker Ram, A Lakshmisudha / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 6, November- December 2012, pp.130-135

Using Passive Front-ends on Diode-clamped multilevel converters for Voltage control

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Abstract

This paper presents a novel closed-loop control approach capable of guaranteeing the balance of the dc-link capacitor voltages of multilevel three-phase diode-clamped dc–ac converters with passive front-ends for high modulation indices for all operating conditions of the converters without the need for additional hardware. There are three different phase duty-ratio perturbation schemes proposed in this paper. A four-level three-phase diode-clamped dc–ac converter operated with a virtual-vector-based modulation is compared through simulations. The most straightforward and useful perturbation scheme requiring the sensing of all dc-link capacitor voltages is tested experimentally in the same four-level converter. With the help of the demonstrated results the dc-link capacitor voltage balance is guaranteed for all converter operating conditions.

Keywords – Voltage, Diode, Multilevel converter

I. INTRODUCTION

MULTILEVEL techniques [1], [2] have opened a door for advances in the electrical energy conversion technology. For a given semiconductor technology, these techniques allow a higher power rating per converter, a higher efficiency, and a lower harmonic distortion, compared to the conventional two level converter. Multilevel converters are typically considered for high power applications, because they allow operating at higher dc-link voltage levels avoiding the problems of the series interconnection of devices. But they can also be interesting for medium or even low power/voltage applications, since they allow operating with lower voltage-rated devices, with potentially better performance/economical features [3], [4]. There are three basic multilevel converter topologies: diodeclamped, flying capacitor, and cascaded H-bridge with separate dc sources. Among these topologies, diode-clamped converters are especially interesting because of their simplicity (see Fig. 1):

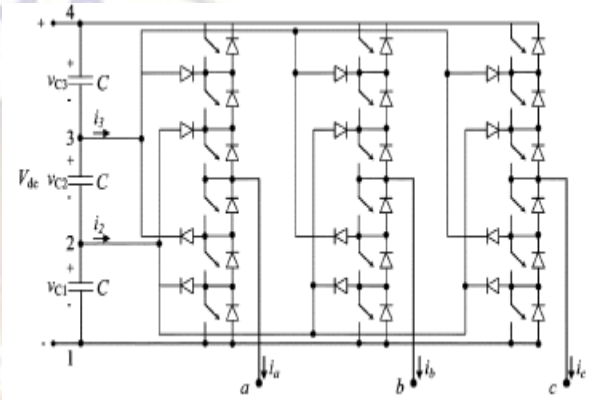

Fig.1: Four-level three-phase diode-clamped dc–ac converter.

$$m < \frac{2}{\pi \cdot |\cos(\varphi)|} = \frac{0.637}{|\cos(\varphi)|}. \quad (1)$$

In the case of a three-phase linear load with phase impedance angle , the region for balanced operation is defined by

$$m < \frac{\sqrt{3}}{\pi \cdot |\cos(\varphi)|} = \frac{0.551}{|\cos(\varphi)|}. \quad (2)$$

These boundaries for balanced operation are depicted in Fig. 2. [7] and [10] corroborate these limits in the particular case of a four-level three-phase converter using a closed-loop control tied to a conventional nearest-three space vector

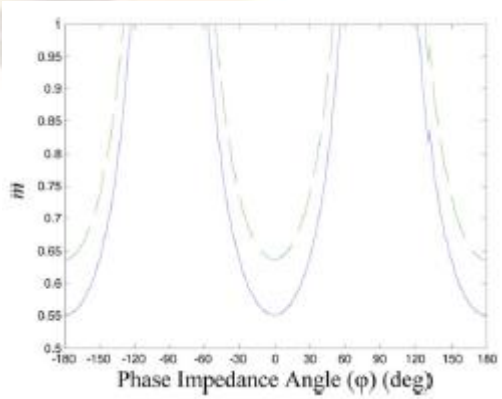

Fig.2: Boundaries for balanced dc-link capacitor voltage operation using conventional PWMs

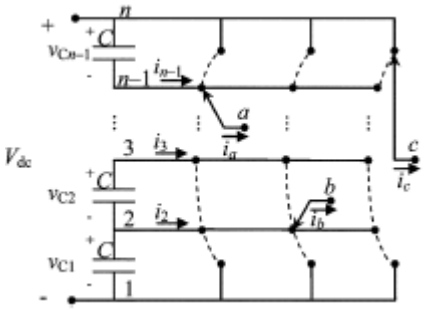

Fig.3: Functional schematic of a n-level three-phase converter

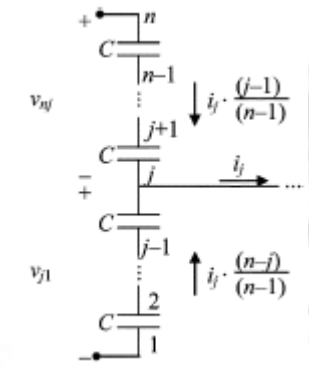

Fig.4: Distribution of current i through the dc-link capacitors.

II. BALANCING CONCEPT

a) Balancing Principle

Fig. 3 presents a functional schematic of a -level three-phase converter; the dc-link capacitor voltage balance condition can be formulated as

$$v_{C1} = v_{C2} = \cdots = v_{Cn-1}. \quad (3)$$

This causes a variation of the partial dc-link voltages and

$$dv_{nj} = -dv_{j1} = \frac{(n-j)\cdot(j-1)}{C\cdot(n-1)}\cdot i_j \cdot dt. \quad (4)$$

$$\frac{v_{j1}}{(j-1)} = \frac{v_{nj}}{(n-j)}. \quad (5)$$

Hence, meeting (5) for all inner dc-link points guarantees the dc-link capacitor voltage balance.

b) Balancing Control

Fig. 5 shows the proposed balancing control structure, consisting of n-2 control loops. The n-1 sensed dc-link capacitor voltages are used to compute the n-2 unbalance values corresponding to each inner dc-link point.

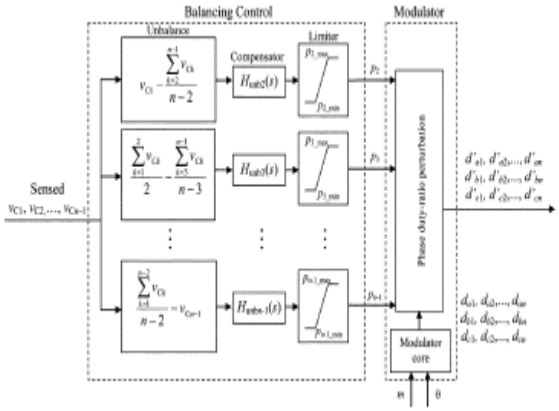

Fig.5: Balancing control structure

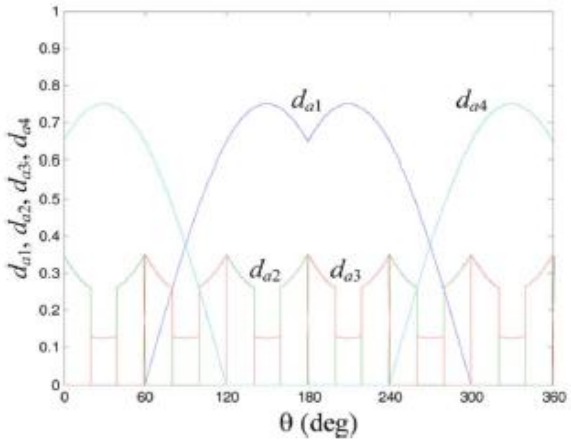

Fig.6: Phase a duty-ratio pattern without perturbation (m = 0.75)

b. (i) Perturbation Scheme A

In perturbation scheme A (PSA) each phase is perturbed independently from the others. The equations describing this perturbation scheme for phase are

$$\text{sign}(w) = 1, \quad w \geq 0$$
$$\text{sign}(w) = -1, \quad w < 0$$
$$d'_{xn} = d_{xn} - \left[\frac{(j-1)}{(n-1)}\right]\cdot p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{xj} = d_{xj} + p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{x1} = d_{x1} - \left[\frac{(n-j)}{(n-1)}\right]\cdot p_j \cdot \text{sign}(p_j \cdot i_x).$$

b. (ii) Perturbation Scheme B

In perturbation scheme B (PSB) only two duty ratios per phase need to be perturbed. Let us designate as the phase carrying the highest absolute value of current; and the other two phases.

$$d'_{xn} = d_{xn}$$
$$d'_{xj} = d_{xj} + p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{x1} = d_{x1} - p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{yn} = d_{yn} + \left[\frac{(j-1)}{(n-j)}\right] \cdot p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{yj} = d_{yj} - \left[\frac{(j-1)}{(n-j)}\right] \cdot p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{y1} = d_{y1}$$
$$d'_{zn} = d_{zn} + \left[\frac{(j-1)}{(n-j)}\right] \cdot p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{zj} = d_{zj} - \left[\frac{(j-1)}{(n-j)}\right] \cdot p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{z1} = d_{z1}.$$

For $j > (n+1)/2$ the equations are

$$d'_{xn} = d_{xn} - p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{xj} = d_{xj} + p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{x1} = d_{x1}$$
$$d'_{yn} = d_{yn}$$
$$d'_{yj} = d_{yj} - \left[\frac{(n-j)}{(j-1)}\right] \cdot p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{y1} = d_{y1} + \left[\frac{(n-j)}{(j-1)}\right] \cdot p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{zn} = d_{zn}$$
$$d'_{zj} = d_{zj} - \left[\frac{(n-j)}{(j-1)}\right] \cdot p_j \cdot \text{sign}(p_j \cdot i_x)$$
$$d'_{z1} = d_{z1} + \left[\frac{(n-j)}{(j-1)}\right] \cdot p_j \cdot \text{sign}(p_j \cdot i_x).$$

b. (i) Perturbation Scheme C

An algorithm describing this perturbation scheme for phase, assuming, is

$$v_{a1} = v_{C1} \cdot d_{a2} + (v_{C1} + v_{C2}) \cdot d_{a3} + \cdots + (v_{C1} + v_{C2} + \cdots + v_{Cn-1}) \cdot d_{an}$$
$$v_{b1} = v_{C1} \cdot d_{b2} + (v_{C1} + v_{C2}) \cdot d_{b3} + \cdots + (v_{C1} + v_{C2} + \cdots + v_{Cn-1}) \cdot d_{bn}$$
$$v_{c1} = v_{C1} \cdot d_{c2} + (v_{C1} + v_{C2}) \cdot d_{c3} + \cdots + (v_{C1} + v_{C2} + \cdots + v_{Cn-1}) \cdot$$
$$v_{ac} = v_{a1} - v_{c1}$$
$$v_{bc} = v_{b1} - v_{c1}$$
$$pow = i_a \cdot v_{ac} + i_b \cdot v_{bc}$$

if $(p_j \cdot pow \geq 0)$ {
  if $\left(d_{xn} > \frac{|p_j|}{n-j}\right)$ {
    $d'_{xn} = d_{xn} - \frac{p_j|}{n-j}$
    $d'_{x1} = d_{x1}$
  } **else** {
    $d'_{xn} = 0$
    $d'_{x1} = d_{x1} + \left[\frac{|p_j|}{n-j} - d_{xn}\right] \cdot \left[\frac{n-j}{j-1}\right]$
  }
} **else** {
  if $\left(d_{x1} > \frac{p_j|}{(j-1)}\right)$ {
    $d'_{x1} = d_{x1} - \frac{p_j}{j-1}$
    $d'_{xn} = d_{xn}$
  } **else** {
    $d'_{x1} = 0$
    $d'_{xn} = d_{xn} + \left[\frac{|p_j|}{j-1} - d_{x1}\right] \cdot \left[\frac{j-1}{n-j}\right]$
  }
}

$$d'_{xj} = (d_{x1} + d_{xj} + d_{xn}) - d'_{x1} - d'_{xn}.$$

III. RESULTS

Fig. 7 presents the results for a transient with an initial unbalance in the dc-link capacitor voltages. The control parameters are

$$H_{unb2}(s) = H_{unb3}(s) = \frac{(s + 2\pi \cdot 0.1)}{s \cdot (s + 2\pi \cdot 100)}$$
$$[p_{2\text{-min}}, p_{2\text{-max}}] = [p_{3\text{-min}}, p_{3\text{-max}}] = [-0.1, 0.1].$$

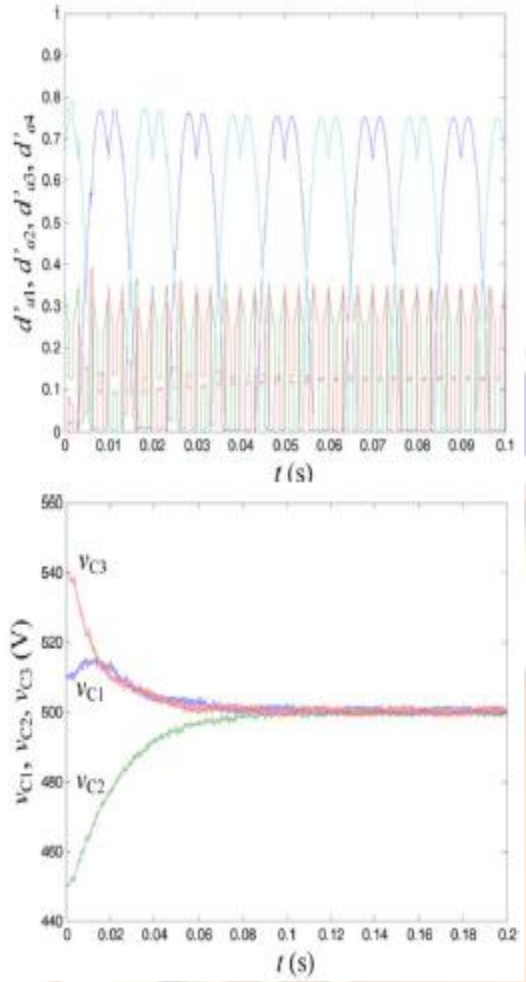

Fig.7(a): Simulation result for PSA_1

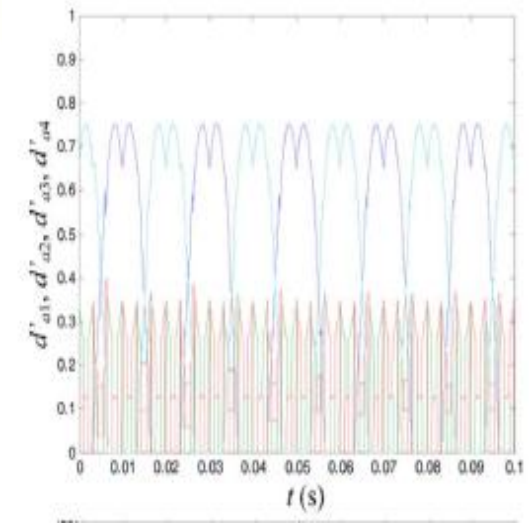

Fig.7(b): Simulation result for PSA_2

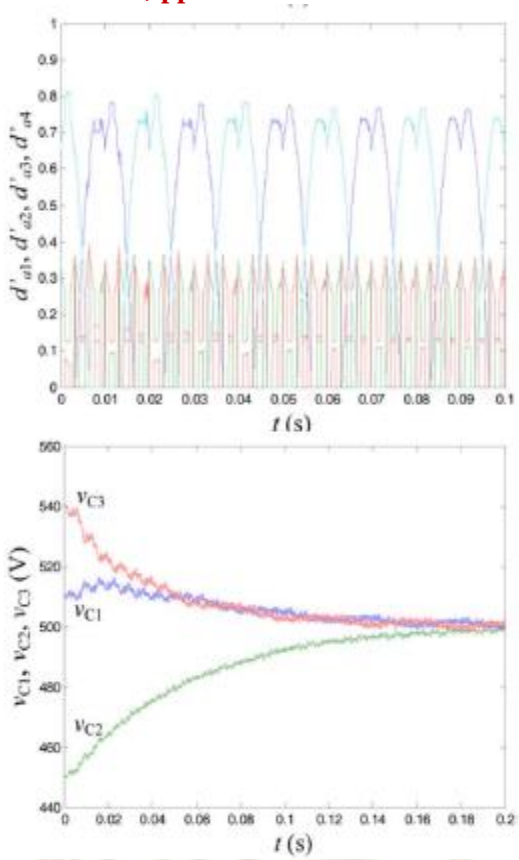

Fig.7(c): Simulation result for PSA_3

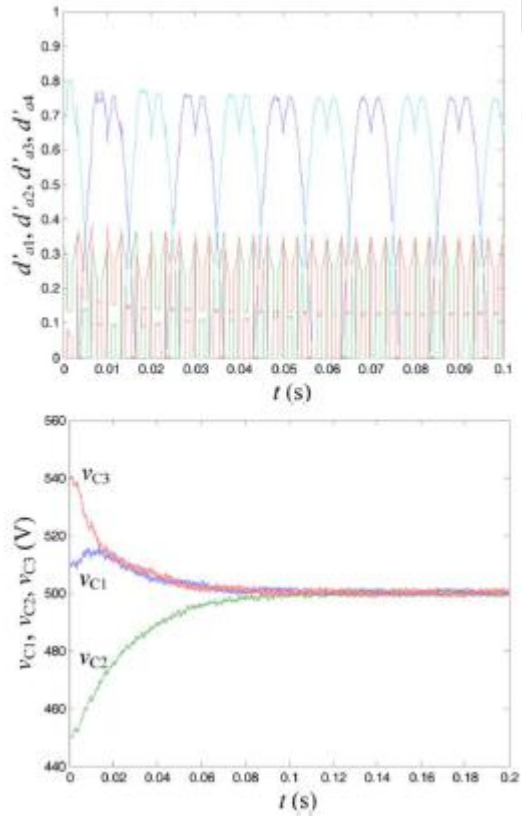

Fig.7(d): Simulation result for PSA_4

Experimental results have been obtained with the same system configuration as in the previous

Section. A resistor has been connected in parallel with each dc-link capacitor. The three resistors have nominal values 10 k , 5 k , and 10 k , respectively, in order to produce an initial dc-link voltage unbalance.

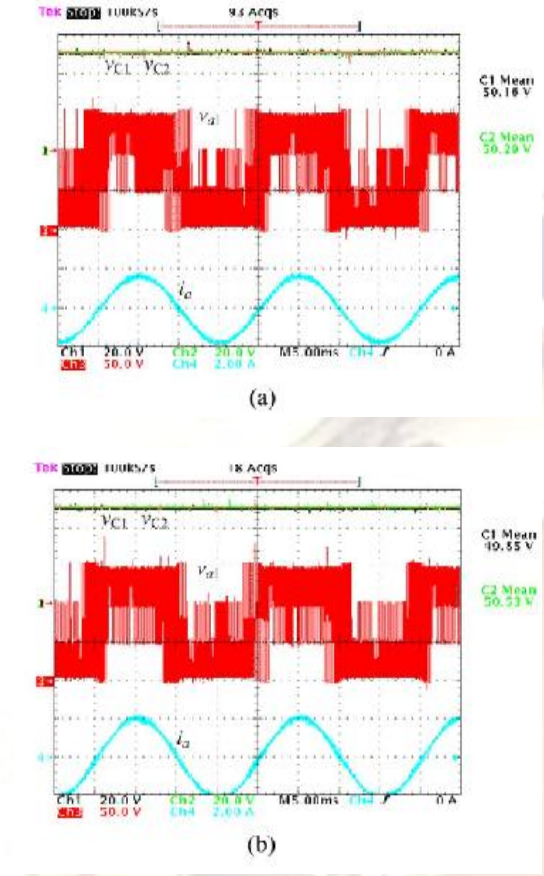

Fig.8: Experimental results in steady-state for dc-link voltages

CONCLUSION

A novel control approach (patent pending) for the balancing of the dc-link capacitor voltages of diode clamped multilevel converters with any number of levels, any number of legs, and passive front-ends is presented in this paper. A set of command signals P(i) are generated from the sensed dc-link capacitor voltages and are used to perturb the appropriate phase duty-ratios in order to recover the balance. Among the three different duty-ratio perturbation schemes which have been discussed and compared PSC performs the best in three-phase systems and does not require sensing the phase currents in unidirectional power flow applications. Comparing with the traditional control methods (selection of the proper redundant switching state in NTV PWMs, for example), the control method proposed here has the advantage of guaranteeing dc-link capacitor voltage balance for all possible values of the modulation index and for any load (linear, nonlinear, balanced, unbalanced), while traditional control methods are bounded by (1) and (2) (see Fig. 2). The increase in balanced operating range is obtained at an expense of an increase of switching transitions per switching cycle and a higher output voltage distortion, when the control is applied to conventional core modulation strategies such as the NTV PWM. However, applying to core modulations such as VV PWMs, does not increases the number of switching transitions and output voltage distortion, and prevents the unbalance due to non ideal operating conditions (unequal device behavior, load neutral-to-ground leakage currents, etc.). Consequently, the proposed control solution enables the practical use of diode-clamped multilevel converters with passive front-ends under the full range of operating conditions especially, for high modulation indices.

References

[1] G. Sinha and T. A. Lipo, "A four-level inverter based drive with a passive front-end," IEEE Trans. Power Electron., vol. 15, no. 2, pp.285–294, Mar. 2000.

[2] M. Marchesoni and P. Tenca, "Theoretical and practical limits in multilevelMPC inverters with passive front ends," in Proc. Eur. Conf. Power Electron. Appl., 2001, [CD ROM].

[3] J. Pou, P. Rodriguez, J. Zaragoza, V. Sala, C. Jaén, and D. Boroyevich, "Enhancement of carrier-based modulation strategies for multilevel converters," in Proc. IEEE Power Electron. Spec. Conf., 2005, pp. 2534–2539.

[4] B. P. McGrath, T. Meynard, G. Gateau, and D. G. Holmes, "Optimal modulation of flying capacitor and stacked multicell converters using a state machine decoder," IEEE Trans. Power Electron., vol. 22, no. 2, pp. 508–516, Mar. 2007.

[5] Z. Du, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," IEEE Trans. Power Electron., vol. 21, no. 2, pp. 459–469, Mar. 2006.

[6] M. S. A. Dahidah, V. G. Agelidis, and M. V. Rao, "On abolishing symmetry requirements in the formulation of a five-level selective harmonic elimination pulse-width modulation technique," IEEE Trans. Power Electron., vol. 21, no. 6, pp. 1833–1837, Nov. 2006.

[7] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," IEEE Trans. Ind. Appl., vol. 41, no. 3, pp. 855–865, May/ Jun. 2005.

[8] C. Newton and M. Sumner, "Neutral point control for multi-level inverters: Theory, design and operational limitations," in

Proc. IEEE Ind. Appl. Soc. Annu. Meeting, 1997, pp. 1336–1343.

[9] G. S. Perantzakis, F. H. Xepapas, and S. N. Manias, "A novel fourlevel voltage source inverter—Influence of switching strategies on the distribution of power losses," IEEE Trans. Power Electron., vol. 22, no. 1, pp. 149–159, Jan. 2007.

[10] Z. Cheng and B.Wu, "A novel switching sequence design for five-level NPC/H-bridge inverters with improved output voltage spectrum and minimized device switching frequency," IEEE Trans. Power Electron., vol. 22, no. 6, pp. 2138–2145, Nov. 2007.

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