Vaddi Ramesh, U. Haribabu / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 6, November- December 2012, pp.1129-1135

Simulate The Implementation Of Interleved Boost Converter With Zero Voltage Transition

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ABSTRACT

This paper proposes a novel soft-switching interleaved Boost converter composed of two shunted elementary boost conversion units and an auxiliary inductor. This converter is able to turn on both the active power switches at zero voltage to reduce their switching losses and evidently raise the conversion efficiency. Since the two parallel-operated elementary boost units are identical, operation analysis and design for the converter module becomes quite simple. A laboratory test circuit is built, and the circuit operation shows satisfactory agreement with the theoretical analysis. The experimental results show that this converter module performs very well with the output efficiency as high as 95%.

Keywords: Interleaved boost converter, Quasi resonant converter, Soft switching, ZerocureentSwitching(ZCS), ZerovoltageSwitching(ZVS),

I. INTRODUCTION

Boost converters are popularly employed in equipments for different applications. For high-power-factor requirements, boost converters are the most popular candidates, especially for applications with dc bus voltage much higher than line input. Boost converters are usually applied as pre regulators or even integrated with the latter-stage circuits or rectifiers into single-stage circuits. Most renewable power sources, such as photovoltaic power systems and fuel cells, have quite low-voltage output and require series connection or a voltage booster to provide enough voltage output. Several soft-switching techniques, gaining the features of zero-voltage switching (ZVS) or zero-current switching (ZCS) for dc/dc converters, have been proposed to substantially reduce switching losses, and hence, attain high efficiency at increased frequencies. There aremany resonant or quasi-resonant converters with the advantages of ZVS or ZCS presented earlier. The main problem with these kinds of converters is that the voltage stresses on the power switches are too high in the resonant converters, especially for the high-input dc-voltage applications. Passive snubbers achieving ZVS are attractive, since no extra active switches are needed,

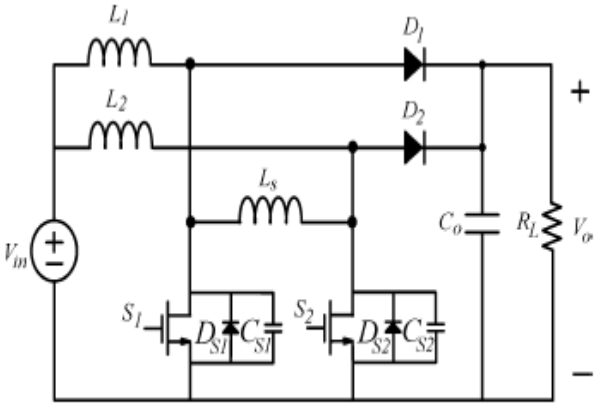


Fig. 1. Proposed interleaved boost converter.

and therefore, feature a simpler control scheme and lower cost. However, the circuit topology is complicated and not easy to analyze. Auxiliary active snubbers are also developed to reduce switching losses. These snubbers have additional circuits to gate the auxiliary switch and synchronize with the main switch. Besides, they have an important role in restraining the switching loss in the auxiliary switch. Converters with interleaved operation are fascinating techniques now a days. Interleaved boost converters are applied as power-factor-correction front ends. An interleaved converter with a coupled winding is proposed to a provide a lossless clamp. Additional active switches are also appended to provide soft-switching characteristics. These converters are able to provide higher output power and lower output ripple. This paper proposes a soft-switching interleaved boost converter composed of two shunted elementary boost conversion units and an auxiliary inductor. This converter is able to turn on both the active power switches at zero voltage to reduce their switching losses and evidently raise the conversion efficiency. Since the two parallel-operated boost units are identical, operation analysis and design for the converter module becomes quite simple.

II.CIRCUIT CONFIGURATION

The voltage source V_{in} , via the two Fig. 1 shows the proposed soft-switching converter module. Inductor L1 , MOSFET active switch S1, and diode D1 comprise one step-up conversion unit, while the components with subscript “2” form the

other.D_{sx} and C_{sx} are the intrinsic antiparallel diode and output capacitance of MOSFET S_x , respectively.
paralleled converters, replenishes output capacitor C_o and the load. Inductor

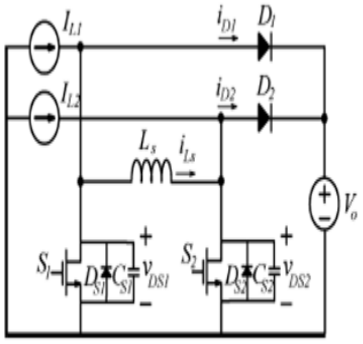


Fig. 2. Simplified circuit diagram.

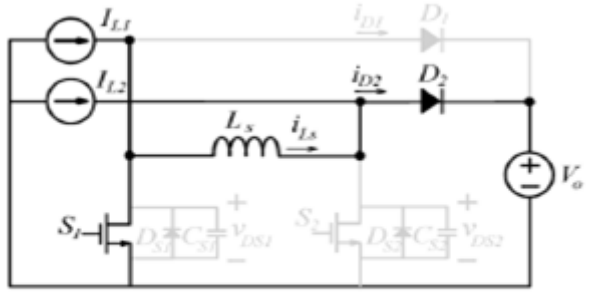
L_S is shunted with the two active MOSFET switches to release the electric charge stored within the output capacitor C_{sx} prior to the turn-ON of S_x to fulfill zero-voltage turn- ON (ZVS), and therefore, raises the converter efficiency. To simplify the analysis,L1,L2, and C_0 are replaced by current and voltage sources.

III CIRCUT OPERATION ANALYSIS

Before analysis on the circuit, the following assumptions are presumed.
1) The output capacitor C_0 is large enough to reasonably neglect the output voltage ripple.
2) The forward voltage drops on MOSFET S_1,S_2, and diodes D_1, and D_2, are neglected.
3) InductorsL_1, and L_2 have large inductance, and their currents are identical constants, i.e.,I_{L1}=I_{L2}=I_L .
4) Output capacitances of switches C_{S1}, and C_{S2} have the same values, i.e.,C_{S1}=C_{S2}=CS.

The two active switches S_1 and S_2 are operated with pulse width-modulation (PWM) control signals. They are gated with identical frequencies and duty ratios. The rising edges of the two gating signals are separated apart for half a switching cycle. The operation of the converter can be divided into eight modes, and the equivalent circuits and theoretical waveforms are illustrated in Figs. 3 and 4.

Mode-1



(a)

Prior to this mode, the gating signal for switch S_2 has already transmitted to low state and the voltage V_{DS2} rises toV_0 at t_0 . At the beginning of this mode, current flowing through S_2 completely commutates to D_2 to supply the load. Current I_{S1} returns from negative value toward zero;I_{L1} flows through L_S. Due to the zero voltage on V_{DS1} , the voltage across inductor L_S is V_0, i.e. i_{LS}, will decrease linearly at the rate of V_0/L_S. Meanwhile, the current flowing through S_1 ramps up linearly. As i_{LS} drops to zero, current i_{s1} contains only I_{L1}, while i_{D2} equals I_{L2}. Current i_{LS} will reverse its direction and flow through S_1 together with I_{L1}. As i_{LS} increases in negative direction,i_{D2} consistently reduces to zero. At this instant,i_{LS} equals $-I_{L2}$, diode D_2 turns OFF , andthus this mode comes to an end. Despite the minor deviation of i_{S1} from zero and I_{LS} from I_{L1}, currents i_{LS} ,is_1,i_{D2} and the duration of this mode t_{01} can be approximated as

$$i_{Ls}(t) = I_L - \frac{V_o}{L_S}t \quad (1)$$

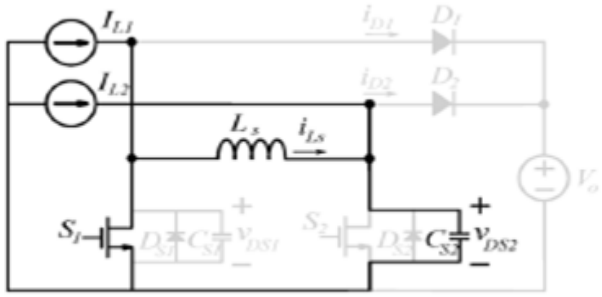
$$i_{S1}(t) = \frac{V_o}{L_S}t \quad (2)$$

$$i_{D2}(t) = 2I_L - \frac{V_o}{L_S}t \quad (3)$$

$$t_{01} = \left(\frac{3}{4} - D_{\text{eff}}\right)T_S - \frac{\sin^{-1}(V_o/(V_o + 2I_L/\omega C_S))}{\omega} \quad (4)$$

where D_{eff} is the effective duty ratio to be explained later and $\omega = 1/\sqrt{L_S C_S}$.

Mode II



(b)

Whereas diode D_2 stops conducting, capacitor C_{S2} is not clamped at V_0 anymore. The current flowing through L_S and i_{LS} continues increasing and commences to discharge C_{S2}. This mode will terminate as voltage across switch S_2,v_{DS2}, drops to zero. Voltage v_{DS2} and current i_{LS} can be equated as

$$v_{DS2}(t) = V_o \cos(\omega t) \quad (5)$$

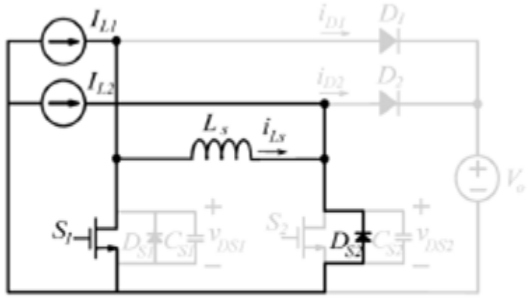
$$i_{Ls}(t) = -V_o \omega C_S \sin(\omega t) - I_L \quad (6)$$

$$t_{12} = \frac{\pi}{2\omega}. \quad (7)$$

Mode III {$t_2 < t < t_3$,}

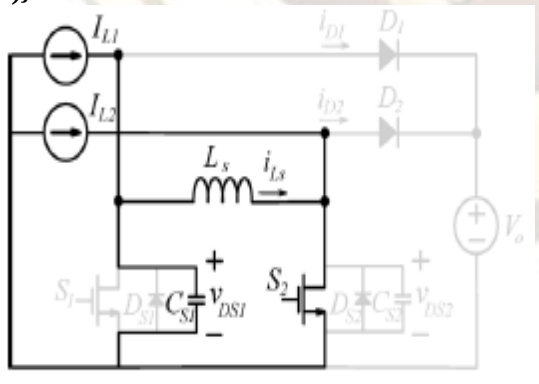
At $t=t_2$, voltage v_{DS2} decreases to zero. After this instant, D_{S2}, the antiparallel diode of S_2, begins to conduct current. The negative directional inductor current i_{LS} freewheels through S_1 and D_{S2} , and holds at a magnitude that equals $i_{LS2(t2)}$, a little higher than I_L. During this mode, the voltage on switch S_2 is clamped to zero, and it is adequate to gate S_2 at zero-voltage turn- ON

$$t_{23} = \left(D_{\text{eff}} - \frac{1}{2}\right) T_S. \quad (8)$$



(c)

D. Mode IV {$t_3 < t < t_4$ **, Referring to Fig. 3*(d)*}**



(d)

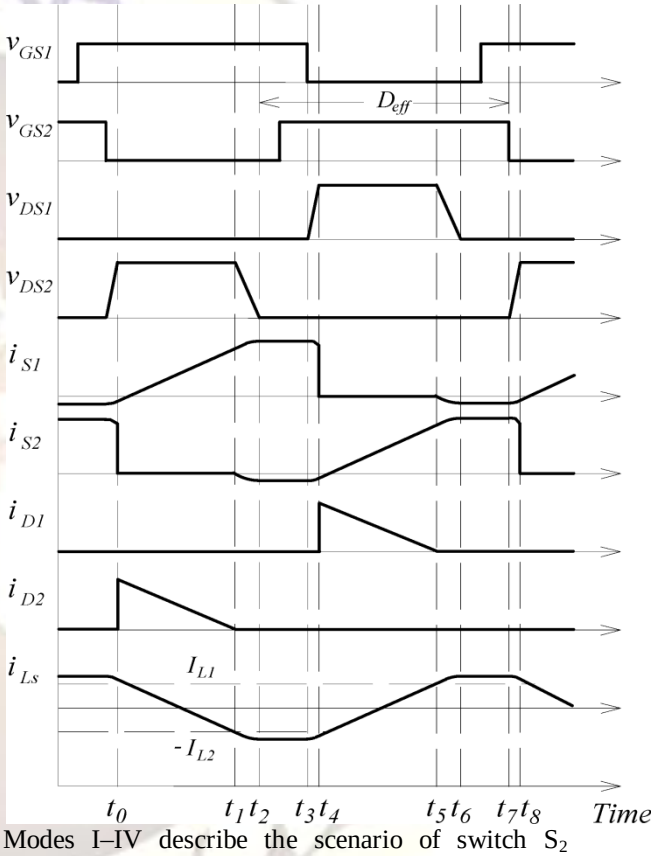
The switch S_1 turns OFF at $t=t_3$. Current i_{LS} begins to. Charge the capacitor C_{S1}. The charging current includes I_{L1} and i_{LS} . Since the capacitor C_{S1} retrieves a little electric charge, i_{LS} decreases a little and resonates toward $-I_{L2}$. In fact i_{LS}, will not equal $-I_{L2}$ at t_4 even with a slightly higher magnitude. However, by ignoring the little discrepancy, the voltage on switch S_1 and current through L_S can be approximated as

$$v_{DS1}(t) = \left(V_o + \frac{2I_L}{\omega C_S}\right) \sin(\omega t) \quad (9)$$

$$i_{Ls}(t) = I_L - (V_o \omega C_S + 2I_L) \cos(\omega t) \quad (10)$$

$$t_{34} = \frac{\sin^{-1}\left(V_o/(V_o + 2I_L/\omega C_S)\right)}{\omega}. \quad (11)$$

While the capacitor voltage v_{CS1} ramps to V_0,D_1 will be forward-biased, and thus this mode will come to an end.



Modes I–IV describe the scenario of switch S_2 between off-state proceeding to ZVS turn-ON . Operations from modes V–VIII are the counterparts for switch S_1. Due to the similarity, they are omitted here.

IV. CIRCUIT DESIGN

The proposed circuit is focused on higher power demand applications. The inductors L_1 and L_2 are likely to operate under continuous conduction mode (CCM); therefore, the peak inductor current can be alleviated along with less conduction losses on active switches. Under CCM operation, the inductances of L_1 and L_2 are related only to the current ripple specification. What dominates the output power range and ZVS operation is the inductance of L_S.

A. Considerations on Inductor L_S

As the description in mode II, prior to the turn-ON of switch S_2, i_{LS} will discharge C_{S2}, the output capacitor of switch S_2, and therefore, surpass I_{L2} . In order to turn ON S_2 at ZVS condition, switch S_1 has to keep conducting current so as to i_{LS} allow to flow through antiparallel diode D_{S2}. While D_{S2} clamps the switch voltage at zero, the gating signal v_{GS2} can comfortably impose on S_2. This means that v_{GS2} should shift to high state before v_{GS1} goes low. Therefore, for ZVS and symmetrical operations of both switches, the duty ratios of both switches should be greater than 0.5. Whereas v_{DS1} or v_{DS2} is zero, it looks like the switch S_1 or S_2 is turned ON. Taking S_2, for example, modes III–VII constitute the effective switch turn-ON time. Defining the effective duty ratio D_{eff}, the voltage across L_2 and V_{L2} holds at V_{in} for duration of D_{eff} T_S ; while ignoring the tiny period of modes II and VIII, V_{L2} is (V_{in} - V_O) for (1 - D_{eff})T_S. Applying the voltage–second balance principle on inductor L_2, we can obtain

$$V_o = \frac{1}{1 - D_{\text{eff}}} V_{\text{in}}. \tag{12}$$

As for the design L_S of , it can be noted that current i_{LS} will drop from I_{L1} down to $-I_{L2}$ approximately during modes I and II. The current swing span should be a little more than $2I_L$ to discharge C_{S2}, and therefore, reduces v_{DS2} to zero before turning ON . Consequently, (13) can be formulated to estimate the current variation ratio

$$\frac{V_o}{L_S} = \frac{2I_L}{(1 - D_{\text{eff}})T_s} = \frac{I_{\text{in}}}{(1 - D_{\text{eff}})T_s} \tag{13}$$

Where T_S is the switching period and I_{in} is the input current. Assuming that the converter efficiency is, the input and load current are related as follows:

$$I_o = \eta(1 - D_{\text{eff}})I_{\text{in}}. \tag{14}$$

Therefore

$$L_S = \frac{\eta V_o T_s (1 - D_{\text{eff}})^2}{I_o}. \tag{15}$$

B. Considerations on Output Regulation

Combining (13) and (15), we can rewrite the relationship between input voltage V_{in} and output voltage V_0 as

$$V_o = \frac{\eta T_s}{I_o L_s} V_{\text{in}}^2 = \sqrt{\frac{\eta R T_s}{L_s}} V_{\text{in}}. \tag{16}$$

For normal operations of a converter, the output voltage V_0 is expected to be constant. Therefore, for a fixed L_S value, switching period T_S should be modulated to cope with the variations of load current I_0 or input voltage V_{in}. This indicates that this converter will be operated under adaptable

TABLE 1

CIRCUIT PARAMERTER

parameter	Value
Inductors L1 and L2	600µ H
Inductors Ls	200µ H
Capacitor Co	3000 µF
Switching frequency fs	60 kHz
Input voltage vin	85v
Output voltage vo	3o8v
Out power po	3.9kw
MOSFETs S1,S2	IXFH16F84
Diodes D1,D2	IN4007

frequency to provide constant output voltage. Similarly, the input current I_{in} with respect to output current I_0
can be depicted as

$$I_{\text{in}} = \frac{1}{\eta}\sqrt{\frac{V_o I_o T_s}{L_s}}. \tag{17}$$

And the output power P_0 is

$$P_o = \frac{T_s}{L_s} V_{\text{in}}^2 = \eta^2 \frac{L_s}{T_S} I_{\text{in}}^2. \tag{18}$$

C.Considerations on Input Current Ripple

The current ripples on each of the boost inductor I_L can be denoted as

$$\Delta I_L = \frac{D_{\text{eff}} T_S}{L} V_{\text{in}}. \tag{19}$$

Due to the interleaved operation, the input current is the summation of two boost inductor currents. Observing Fig. 5, the input current ripple can be illustrated as (20)

$$\Delta I_{\text{in}} = \frac{(2D_{\text{eff}} - 1)T_S}{L} V_{\text{in}}. \tag{20}$$

Under certain input current ripple requirement, inductance inductorL_1andL_2canbeobtained

D. Considerations Output Voltage Ripple

Since the load and output capacitor receive the current summation from diodes D_1 and D_2, the frequency of the output ripple current becomes twice as high as the switch frequency. Therefore, the output ripple voltage can be reduced. The output ripple voltage can be estimated by evaluating the joint contributions from the capacitance and the equivalent series resistance (ESR)

$$\Delta V_C = \frac{I_o D_{\text{eff}}^2 T_S}{2C_o} = \frac{V_o D_{\text{eff}}^2 T_S}{2RC_o} \tag{21}$$

$$\Delta V_{\text{ESR}} = I_{\text{in}} \times \text{ESR} \tag{22}$$

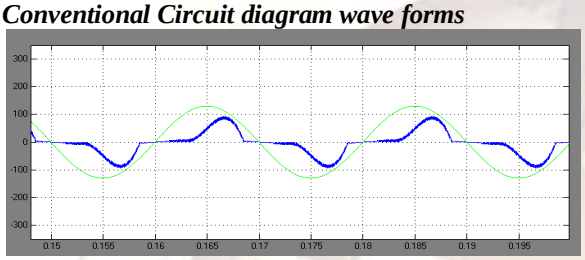
$$\Delta V_o \cong \sqrt{\Delta V_C^2 + \Delta V_{\text{ESR}}^2}. \tag{23}$$

TABLE :2
COMPARISONS ON CALCULATED AND MEASURED PARAMETERS

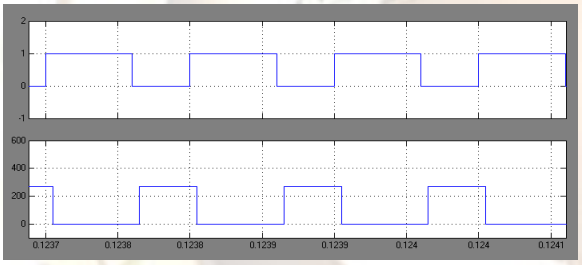
Parameter	Calculated value	Measured value
Effective duty ratio Deff	0.6	0.5
Inductor ripple current ΔIin	7.28A	4.75A
Input ripple current ΔIL	1.32A	0.5A
Output ripple voltage ΔV0	2.144V	1V

IV.I .SIMULATION RESULTS:

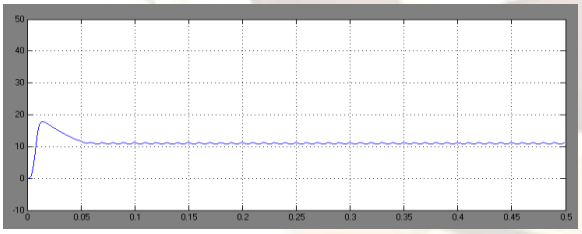
Conventional Circuit diagram wave forms



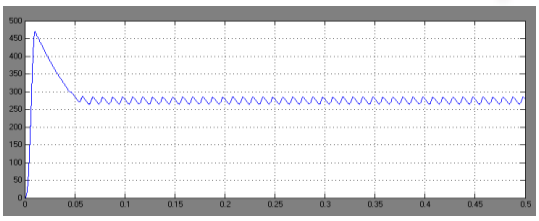
(vin:120v current:30A time:150msec)
Fig:1. Input voltage and current



vgs:1v vds:280v time:123msec)
Fig:2.Voltage vgs andvds triggeringpulsewaveform

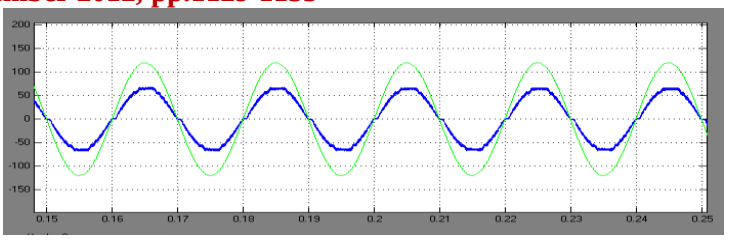


(Cureent:19A time:0.5msec)
Fig 3:Output current

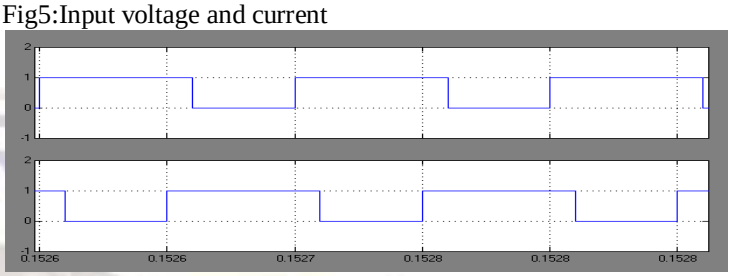


(voltage:470v time:0.5msec)
Fig4:Output voltage

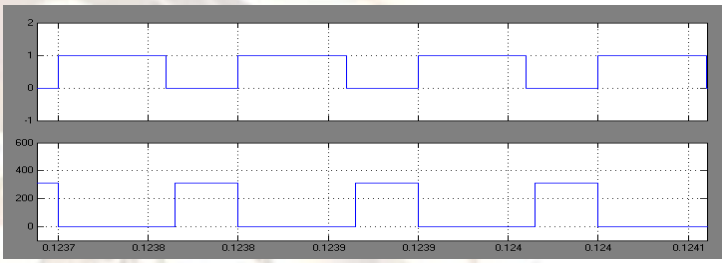
Proposed interleaved boost converter circuit diagram wave form



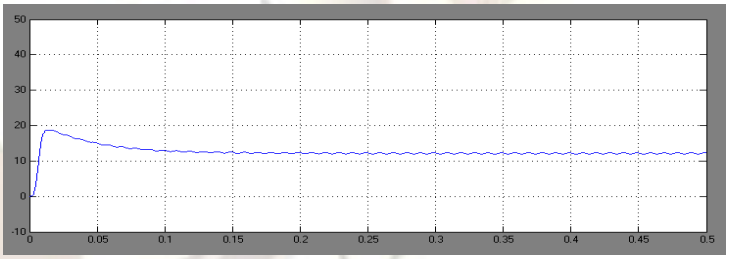
(vin:120v current:30A time:15sec)
Fig5:Input voltage and current



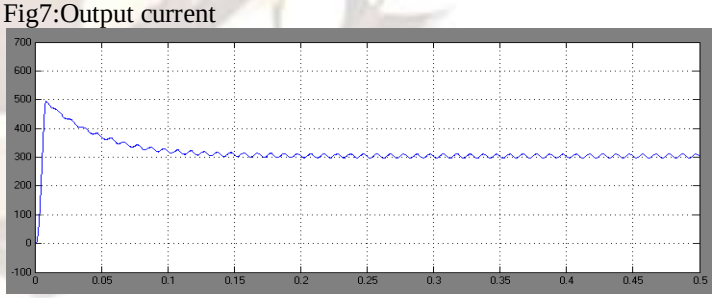
(voltage vg1:1v vg2:1v time:152msec)
Fig6:Vg1andvg2Triggering pulses wave form



Vgs and Vds across S1



(current:19A time:0.5msec)
Fig7:Output current

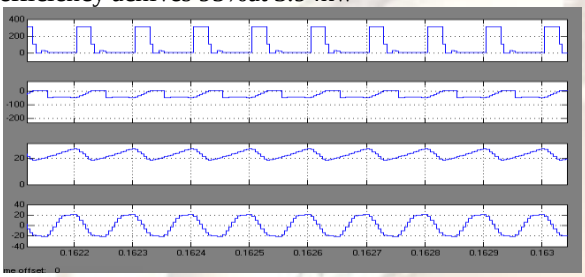


(voltage:480v time:0.5msec)
Fig8:Output voltage

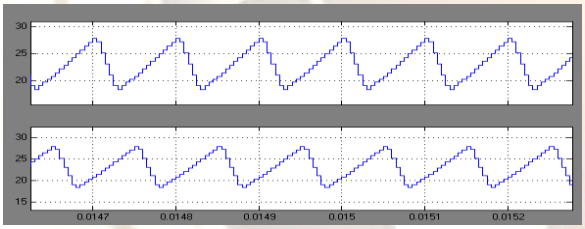
IV.II EXPERIMENTAL RESULT

An experimental circuit is built to verify the fesibility of th is circuit topology .The parametersare listsed Table1
Figs.9 and 10 illsutrate the expermental wavforms. Fig.9 shoews vgs and vds of each switch. Fig.6The gatingSingal is imposed on the switch after its

voltage falls down to zerofig.10depictsrelationships between current iL1,IL2 where this ripple current of iL1 is significant.IL1 flowes thoughswtich s1 during its turn on period fig:11 shows the current ripples clearly input current ripple ΔIin is smaller than Δ IL1 and ΔIL2. The ration of ΔIin/Iin is less than 10%tTable2 lists some comparison between measured results from experimental and calculated results from theoretical equcations.the measuredresults do not inculed the parasitics resonant peaks.the control unit of this is a peripheralinterfance control micro controller.the swtiching frequency is modulatedas depicted in provide output voltage regulation under output power shift.the cricuit is operated at
different power output and input voltage fig15:The result is presented the best conventional voltage is320v and proposed output voltage370v the circuit efficiency achives 95%at 3.94kw



(vg1,vg2:20v vds1,vs2:350v time;162msec)
Fig9:vlotage vgs and vds of each switch



(voltage:28v current:0.5A time:14.2msec)
Fig10:current relationship between iL1,iL2

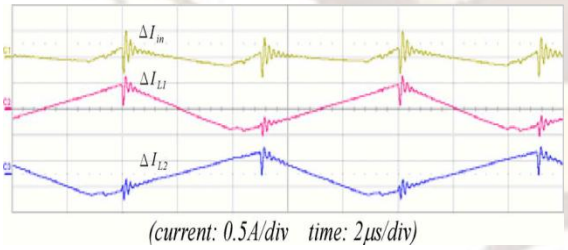
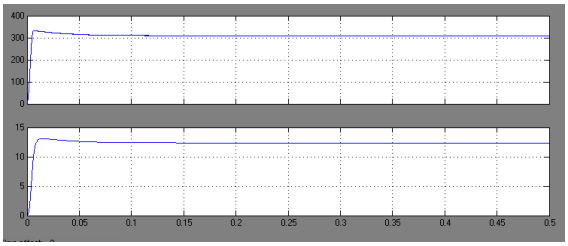


Fig:11Current ripple ΔIin, ΔIL1 and ΔIL2



(voltage:350v cureent:1.5A time:0.5msec)
Fig12: output voltage output current io when power fluctuates between3.9kw

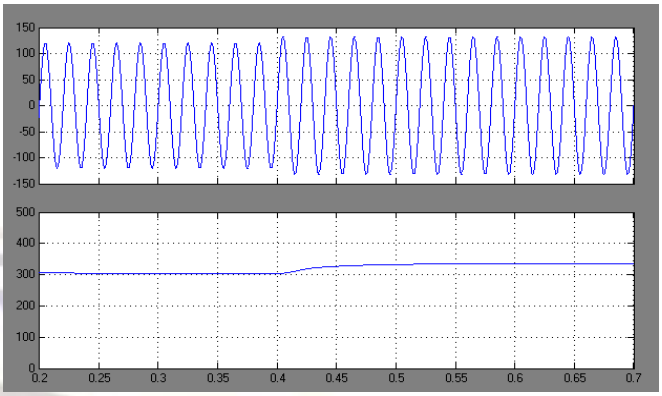


Fig13:open loop input and output wave form
(ac inputvoltage=125v,dc output voltage=320v time:20msec)

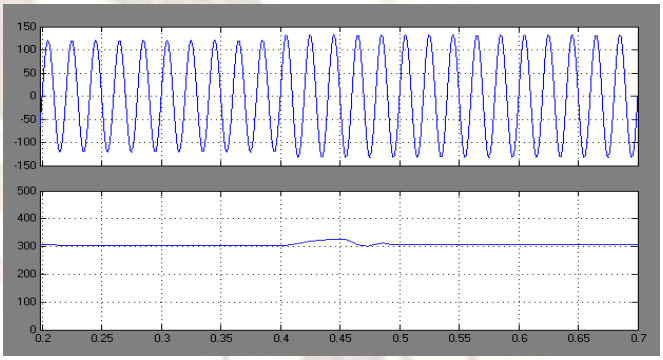


Fig14:closed loop input and output wave form
(ac inputvoltage =125v,dcoutputvolatge=320v time:20msec)

IV.III . INPUT AND OUTPUT CHARACTERISTICS

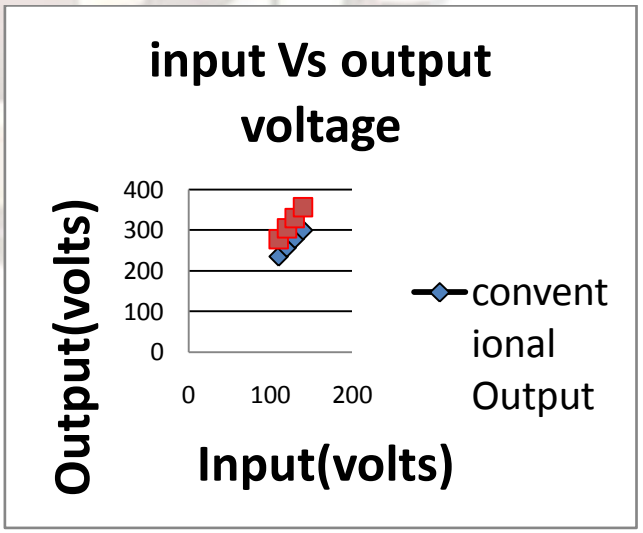
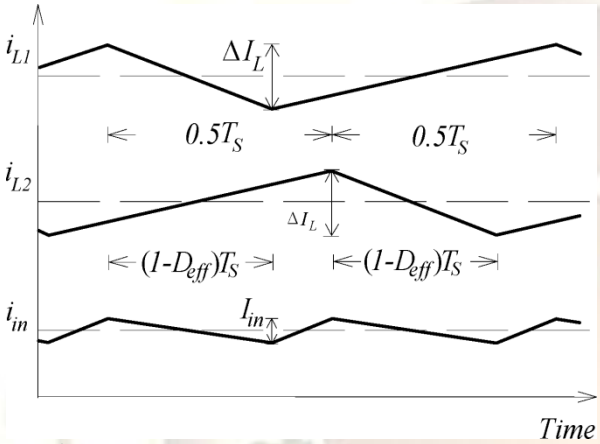


Fig15:different output and input voltage

V.CONCLUSION

This paper has proposed a dual boost converter with zero voltage turn-on. It inherits the merits of interleaved converters, i.e., low output voltage ripple. The detail analysis has presented the design and control equations. Inductor determines the performance of the converter. The converter can be controlled by varying switching frequency to deal with the fluctuation of input voltage and output load. In a laboratory testing circuit, the results is presented in conventional output voltage is 320v and proposed output voltage 370vthe circuit efficiency achieves 95% at 3.94k W output due to its ZVS characteristics.

IV.IV FUTURE SCOPE THE PROJECT



- **3-stage interleaved boost converter with 120 degree shift can be done in future ripple can be reduced**
- **Closed loop can be done with ANN controlling**

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