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Digital Multiple Beam Forming with Parallel Array Processing for Phased Array RADARs

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Abstract

Beam forming is a signal processing technique used in antenna arrays for directional signal transmission or reception. Phased array radar is very important in modern radar development, and multiple digital beam forming technology is the most significant technology in phased array radar. Digital multiple beam forming on each antenna element about large phased array radar is impossible in processor based digital processing units, because it needs simultaneous processing many A/D channels. In this project we resolve this problem by using a multi array based beam forming technique with multiplexed signal processing unit on FPGA. The conventional techniques of completely duplicated hardware and also dynamic reconfiguration[1] does not yield the real time parallel beam processing. The proposed technique employs multiplexed signal processing unit which is time shared for various beam formers. This technique provides simultaneous beams without any compromise on functionality.

Keywords—**Numerically Controlled Oscillator(NCO), Digtial Down coventer(DDC)**

I. INTRODUCTION

A phased array radar is an array of antennas in which the relative phases of the respective signals feeding the antennas are varied in such a way that the effective radiation pattern of the array is reinforced in a desired direction and suppressed in undesired directions. An antenna array is a group of multiple active antennas coupled to a common source or load to produce a directive radiation pattern. Usually, the spatial relationship of the individual antennas also contributes to the directivity of the antenna array. Use of the term "active antennas" is intended to describe elements whose energy output is modified due to the presence of a source of energy in the element (other than the mere signal energy which passes through the circuit) or an element in which the energy output from a source of energy is controlled by the signal input. One common application of this is with a standard multiband television antenna, which has multiple elements coupled together. Phased array transmission was originally developed in 1905 by Nobel Laureate Karl Ferdinand Braun who demonstrated enhanced transmission of radio waves in one direction. During World War II, Nobel Laureate Luis Alvarez used phased array transmission in a rapidly-steer able radar system for "ground-controlled approach", a system to aid in the landing of aero planes in Britain. At the same time GEMA in Germany built the PESA Mammut. It was later adapted for radio astronomy leading to Nobel Prizes for Physics for Antony Hewish and Martin Ryle after several large phased arrays were developed at the University of Cambridge. The design is also used in radar, and is generalized in interferometric radio antennas. In 2007 DARPA researchers announced a 16 element phased array integrated with all necessary circuits to send at 30–50 GHz on a single silicon chip for military purposes. The relative amplitudes of constructive and destructive interference effects among the signals radiated by the individual antennas determine the effective radiation pattern of the array. A phased array may be used to point a fixed radiation pattern, or to scan rapidly in azimuth or elevation. Simultaneous electrical scanning in both azimuth and elevation was first demonstrated in a phased array antenna at Hughes Aircraft Company, Culver City, CA, in 1957 “When phased arrays are used in sonar, it is called beam forming”. The phased array is used for instance in optical communication as a wavelength-selective splitter.

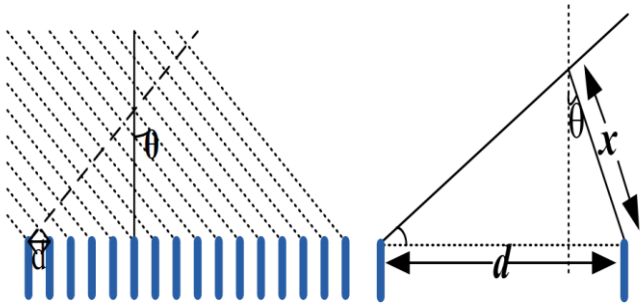

Figure 1. A linear array of antennas with a plane wave with angle of arrival *θ*. Antennas in the array are spaced at distance d

There are two main different types of phased arrays, also called” beam formers”.
1. Time domain beam formers
2. Frequency domain beam formers.

A time domain beam former works, as the name says, by doing time-based operations. The basic operation is called "delay and sum". It delays the incoming signal from each array element by a certain amount of time, and then adds them together. Sometimes a multiplication with a window across the array is done to increase the main lobe/side lobe ratio, and to insert zeroes in the characteristic.

There are two different types of frequency domain beam formers.

1. The first type separates the different frequency components that are present in the received signal into different frequency bins (using either an FFT or a filter bank). When different delay and sum beam formers are applied to each frequency bin, it is possible to point the main lobe to different directions for different frequencies. This can be an advantage for communication links.
2. The other type of frequency domain beam formers makes use of so called “Spatial Frequency”. This means that an FFT is taken across the different array elements, not in time. The output of the N point FFT is N channels, which are evenly divided in space. This approach makes a simple implementation of several beam formers at the same time possible, but this approach is not flexible, because the different directions are fixed.

Beam forming is a signal processing technique which is used in” sensor arrays for directional signal transmission or reception”. This is achieved by combining elements in the array in such a way that signals at particular angles experience constructive interference while others experience destructive interference. Beam forming can be used at both the transmitting and receiving ends in order to achieve spatial selectivity. The improvement compared with Omni directional reception/transmission is known as the receive/transmit gain(or loss).

Digital Beam Forming (DBF) is a combination between “the antenna technology” and “the digital technology”. Workers in Sonar and Radar systems first developed the early ideas of digital beam forming. This coupled with the development of aperture synthesis techniques in radio astronomy lead to the development of the modern dipolar arrays.

Digital beam forming is based on the conversion of the RF signal at each antenna elements into two streams of binary baseband signals representing” cos and sin channels”. These two digital baseband signals can be used to recover both the amplitudes and phases of the signals received at each element of the array. The process of digital beam forming implies weighting by a complex weighting function and then adding together to form the desired output. The key to this technology is the accurate translation of the analog signal into the digital regime. Close matching of several receivers is not achieved in hardware, but rather by applying a calibration process. It is expected that more and more of receiver functions will be implemented using software. Eventually one would expect that the receiver would be built using software rather than hardware.

An antenna can be considered to be a device that converts spatio temporal signals into strictly temporal signals, thereby making them available to a wide variety of signal processing techniques. From a conceptual point of view, its sampled outputs represent all of the data arriving at the antenna aperture. No information is destroyed, at least not until the processing begins and any compromises that are made in the processing stages can be noted and estimates made of the divergence of the actual system from the ideal.

Digital beam forming networks:

1. An element space beam former.
2. Beam space digital beam former.

An element-space beam forming, where the data signals from the array elements are directly multiplied by a set of weights to form the desired beam. Rather than directly weighting the outputs from the array elements, they can be first processed by a multiple –beam former to form a suite of orthogonal beams. The output of each beam can then be weighted and the result combined to produce a desired output. This process is often referred to as the beam-space beam forming.

II. BLOCK DIAGRAM

In order to receive radio signals an antenna must be used. However, since the antenna will pick up thousands of radio signals at a time, a radio tuner is necessary to tune in to a particular frequency (or frequency range).This is typically done via a resonator – in its simplest form, a circuit with a capacitor and an inductor forming a tuned circuit. The resonator amplifies oscillations within a particular frequency band, while reducing oscillations at other frequencies outside the band.

FPGAs are well suited for serial Analog to Digital (A/D) converters. This is mainly because serial interface consumes less communication lines while the FPGA is fast enough to accommodate the high speed serial data. A/D converter is a high speed serial interface that interfaces easily to FPGAs. The A/D interface adapter (AD1_PMOD) is implemented within the FPGA. Inside the FPGA, this adapter facilitates parallel data acquisition. Sampling is initiated at the rising edge of a clock applied at the line sample.

The below fig.2 shows the main block diagram of the digital multiple beam forming which is explained clearly.

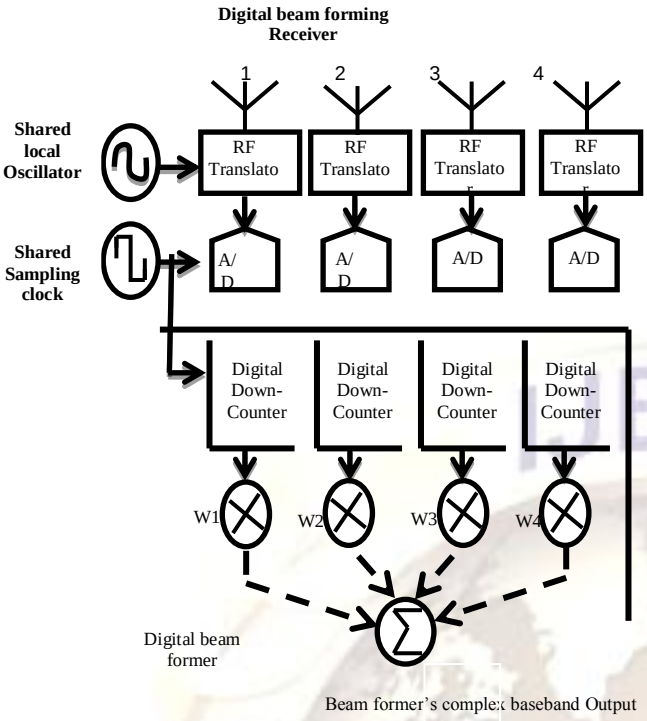

Figure2: Digital Beam Forming

Digital Down-Counter:

The Digital Down-Counter consists of sub modules of

1. Oscillator (NCO)
2. Multiplier
3. Low Pass Filter
4. Decimator

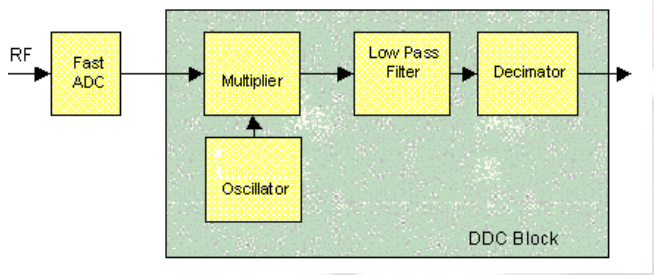

Figure.3 Digital down Counter

The principle of Digital Down-Counter which is taking the input from RF Translator that is given to the input of Fast ADC .The output of Fast ADC block which is given to the DDC block. The DDC (Digital Down-Counter) consists of NCO (Numerically Controlled Oscillator), Multiplier, low pass filter and Decimator.

1. Oscillator (NCO):

The NCO main purpose is to generation the carrier signals (cosine).The main advantage is ROM based techniques will be used for area optimization.

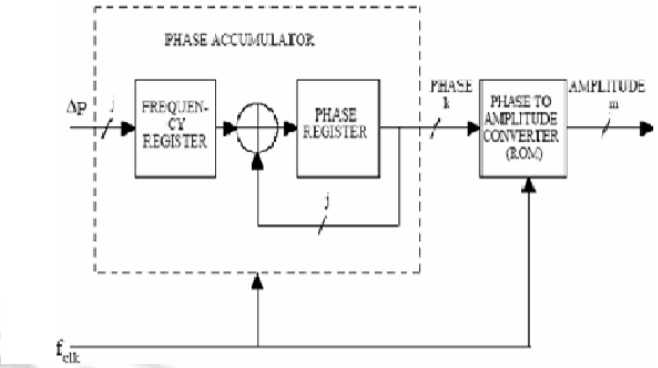

Figure.4 NCO (Oscillator)

PHASE ACCUMULATOR MODULE:

The phase accumulator consists of phase increment register, adder and phase register. The phase increment register stores the instantaneous phase increment values resulting from frequency modulation control block. This is fed to an 8 bit adder as one of its input. The other input for adder is phase register output. The phase register holds the instantaneous phase for each clock pulse. The accumulated phase also is represented by 8 bits, which limits the maximum phase by 11111111, and addition by 1 to maximum value causes the phase to become 00000000 this is expected and desired since the Look up Tables are programmed to consider 255 as highest phase value and phase increment by one results next cycle of waveform. Since 8 bits are used to represent the 0O to 360O the increment in digital phase value by one cause effective increment of 1.40625O (results by dividing 360O with 256 maximum possible combinations of 8 bits). This also implies that outputs can't have more that 256 samples for one cycle.

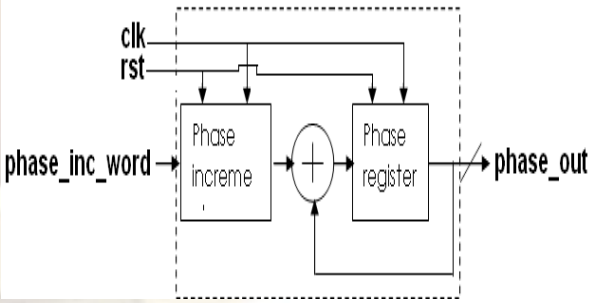

Figure.5 phase accumulator

The output of phase accumulator when the phase increment value is 0000001000000000. It can be observed that the resulting phase value after each clock pulse is four added to the previous phase value. In the following figure initial phase is 0 and further with clock pulses resulting in 4, 8, 12, and 16 ...The output of phase accumulator is added with multiplier output. That output is given to NCO block.

All the blocks are connected with common clock and reset signals. The delta phase value decides the phase increment for each clock pulse. Hence decides the resulting signal frequency. The Frequency modulating instantaneous value is added to the delta phase value which causes instantaneous change in frequency. Due to the digital nature of the modulator only at each clock tick the modulating signal value shall affect the resulting frequency. If the modulating signal is analog then an Analog Digital converter must be used to digitize the modulating signal which can be used in NCO.

The phase accumulator produces accumulated phase value for each clock pulse. In case if the DDS is used for phase modulation then instantaneous phase modulating signal value is added to the phase output of phase accumulator. This resulting phase value is given to the four Look Up Tables. Each Look Up Table is configured to produce a specific waveform. The logic used to generate the Look Up Tables is discussed in the further sections. The outputs of four Look Up Tables are given to the input lines a 4 to 1 Multiplexer. This multiplexer connects one of the inputs to the output depending on the select lines. The output of Multiplexer consists the 8 amplitude bits which is the final output in case required modulation schemes are FM or PM. In case of Amplitude modulation, the output of Multiplexer is multiplied with instantaneous modulating signal. In three modulation schemes if modulating signal is analog in nature then an appropriate Analog to Digital converter is required to convert into 8 bit digital output. The basic blocks in NCO can be identified as PIPO registers, adders, Look Up Tables and other combinational circuits. The following sections presents the implementation details and results obtained for all these blocks. The ModelSim tool from Mentor Graphics is used, for simulation and functional verification of NCO.

VHDL has been used as design entry method for all these blocks. Xilinx ISE (Integrated Software Environment) XST (Xilinx Synthesis Tool) is used as a synthesis tool to implement the design on Spartan-3E FPGA. Chipscope pro is used for analyzing the implemented design.

1. PIPO n bit generic register:

The Parallel in Parallel Out shift register cells are required in phase accumulator block to hold frequency and phase values. Synchronization is required between the phase increment register and phase register. This is achieved by connecting a common clock signal. Generic is used in VHDL implementation which allows to instantiate the PIPO component any bit size.

2. N bit generic adder:

The N-bit generic adder is implemented in VHDL with simple ripple carry adder logic. The adder is tested with inputs A=011001, B=000101 and output observed is Z = 011110.

2. Multiplier:

Here, The output generated by NCO as carrier signal which is multiplied with the ADC outputs. This output is given to next module as low pass filter.

3. Low Pass Filter:

A low-pass filter is an electronic filter that passes low-frequency signals but attenuates (reduces the amplitude of) signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies from filter to filter. It is sometimes called a high-cut filter, or treble cut filter when used in audio applications. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass.

4. Decimator :(Filtering & Decimation):

There are two main classes of DDC – wideband and narrowband, differentiated by their decimation ratios. As a rough guide, if the decimation ratio is less than 32, consider the DDC wideband; if 32 or more, the DDC is narrowband. The filtering we will perform is different for narrowband or wideband, so is tackled separately. However, the decimators can be treated identically for wideband or narrowband systems. Note also that in some systems it may make sense to combine wideband and narrowband DDCs. For example, in a GSM system which uses 8 carriers, a wideband DDC could be used to shift the carriers down to a moderate frequency. This could be done using a simple oscillator – no complex components. 8 narrowband DDCs could then be used to select the individual carriers.

Filtering for Wideband DDCs:

With a wideband signal, we are typically reducing the sampling rate by a small amount, and the data output rate is large. Note that the output rate of a wideband DDC should be checked as part of our overall system design. In some systems that data rate will be significant, and could saturate a DSP processor – if that is meant to be receiving it. The main challenge of a wideband receiver is getting enough processing to filter the signal. All the processing is performed at a fairly high rate, often 20-40MHz. Because of this, the filters tend to be very gate-intensive; a single wideband channel will typically consume more of an FPGA than several narrowband channels. Each design has different requirements. However, the following is a rough guide to implementing the filter. The filter is best implemented as an FIR, and in fact the best approach is to use a multi-rate FIR. This may sound complex, but in fact a multi-rate FIR is simply an efficient way of implementing large filters with decimation.

Imagine we need to implement a large filter at a high sampling rate, before decimating the signal.

However, suppose we split the filter. The first filter can perform enough filtering to allow us to perform some decimation. The second filter is now operating at a much reduced sampling rate. Typically by splitting the filter in this way we can reduce the number of taps in the filter, and reduce the sampling rate that some of these taps operate it. Both reduce the amount of FPGA resource we require to build the filter. Immediately after this filter, decimate the signal by 2, and implement a larger filter. Again, the filter's bandwidth should match the DDC output bandwidth. This will improve the response of the first filter. One can afford to have more taps in this stage, as the sampling rate is lower. For higher decimation ratios (e.g. 8 and up), one can afford to use a third stage filter. This can have significantly more taps than the first two, as each multiplier here can implement at least 4x as many taps as in the first stage. Again, one will want to experiment with the layout of the filters to see what gives best performance.

Designing the Filters:

There can be several tools by which the filter coefficients can be finalized for implementing the required FIR filters. In this project the MATLAB's filter design analysis tool (FDA) will be used for designing. An FIR filter is one whose impulse response is of finite duration. In this filter, the current output (y_n) is calculated solely from the current and previous input values (x_n, x_{n-1}, x_{n-2},...). This type of filter is also said to be non-recursive.

The difference equation, which defines how the input signal is related to the output signal

$$y(n) = b_0 x(n) + b_1 x(n-1) + \cdots + b_P x(n-P)$$

Where P is the filter order, x(n) is the input signal, y(n) is the output signal and b_i are the filter coefficients. The previous equation can also be expressed as

$$y(n) = \sum_{i=0}^{P} b_i x(n-i)$$

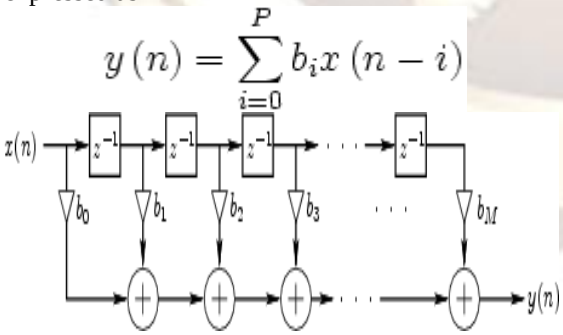

Figure6. Finite Impulse Response Digital Filters

The transfer function allows us to judge whether or not a system is BIBO stable. To be specific the BIBO stability criterion requires all poles of the transfer function to have an absolute value smaller than one. In other words all poles must be located within a unit circle in the *z*-plane.

Filter Design:

To design a filter means to select the coefficients such that the system has specific characteristics. The required characteristics are stated in filter specifications. Most of the time filter specifications refer to the frequency response of the filter. There are different methods to find the coefficients from the specifications:

1. Window design method
2. Weighted least squares design
3. Minimax design
4. In practice the equiripple design is often used

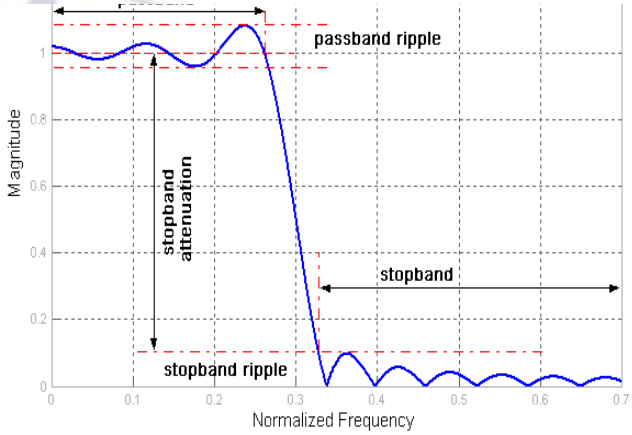

Figure 7.lowpass

In this project equiripple based low pass FIR filter is designed.

SPECIFICATIONS:

The below table1 gives the specifications of the project like input signal type, sampling rate, DDC filter size etc.

TABLE 1 : Beam forming specifications

Parameter	Value	Comments
Input signal type	Band pass signal	Coming from typical superhytrodyne receiver
Input signal frequency range	1.5-3.5 MHz	2 MHz BW and 2.5 Mhz IF frequency value
Sampling rate	10 MHz	
DDC filter size	16 taps	
DDC decimation	4	DDC output sampling rate 2.5 Msps
NCO values: COS	1 0 -1 0	As fo=fs/4
NCO value : -SIN	0 -1 0 1	As fo=fs/4
Number of array elements	16	Linear array as shown in below figure.
Element spacing	3 meters	d as shown in below figure

III. SIMULATION RESULTS

The Digital beam forming receiver of phased array radar using all digital blocks using VHDL coding. In this, we are using the modelsim 6.6b software for simulation results purpose.

The below fig.8 & fig.9 shows the simulation results of single and multiple digital beam forming which will shows the maximum gain in desired direction and minimum gain in the unwanted direction.

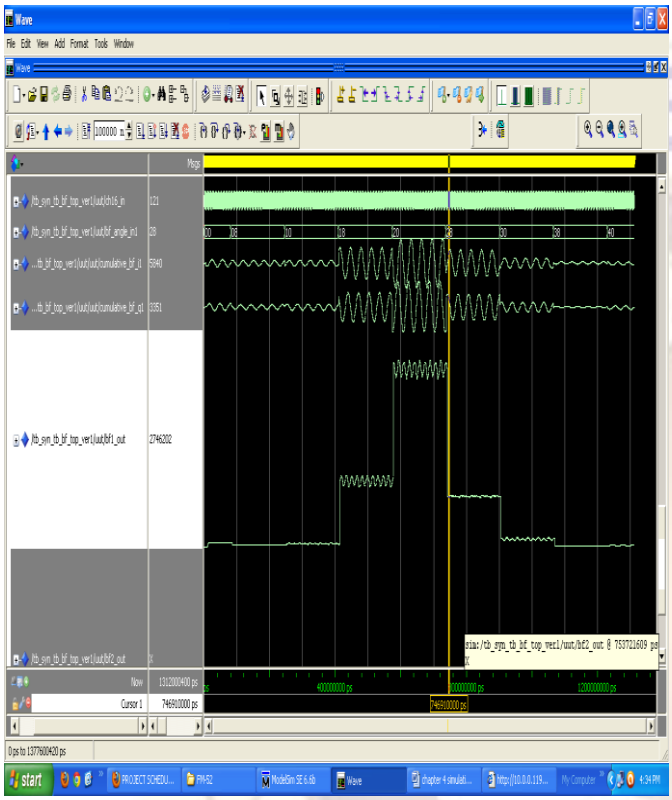

Figure8 A Digital single beam forming

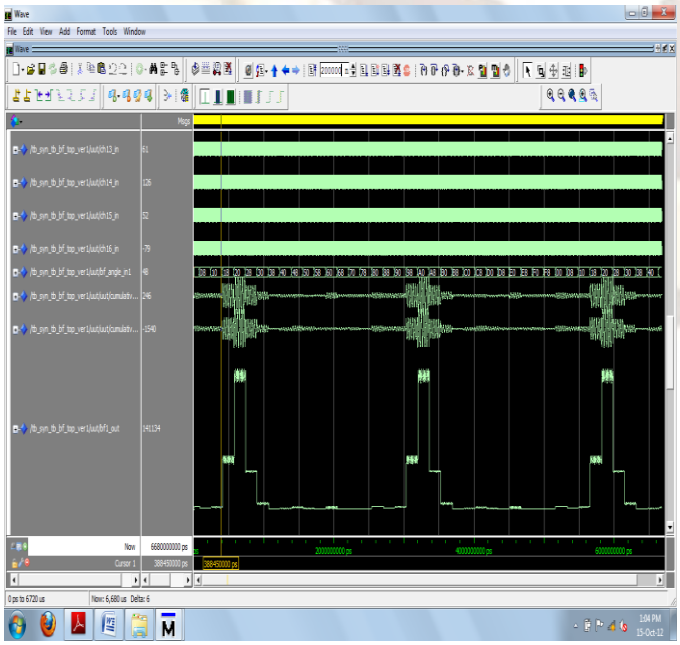

Figure 9 Digital Multiple beam forming

IV. CONCLUSION

This project has explored the design and implementation of a low-cost digital beamforming platform. The board inputs and FPGA beamforming circuits have been tested to verify system operation. The proposed technique employs multiplexed signal processing unit which is time shared for various beam formers. This technique provides simultaneous beams without any compromise on functionality. The low cost of the system facilitates its easy integration into phased array radar systems.

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