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A Novel Sequence Generator Replacing LFSR For Hardwired BIST Of SRAM

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ABSTRACT
This paper has emphasis on the novel sequence generation for the hardwired built in self test (BIST) of static random access memory (SRAM). It reduces the testing time of SRAM by generating all the pattern sequence in less time. BIST is a design technique that allows a circuit to test itself. Linear feedback shift register (LFSR) was used for the sequence generation in the BIST but novel sequence generator is better than LFSR for BIST of SRAM. The novel designing of the sequence generator has done with the help of synchronous up and down counter. The up and down counter has used here is of 4 bits and the corresponding addresses are also of 4 bits but there is a unique transition take place. The switching between the sequence of the up and down counter generates the sequence which is fulfilling the requirement for the BIST purpose. This requires very little hardware overhead so the area is reduced which on the other hand reduced cost as well as power. The necessary sequences which have required for detecting the faults such stuck at/open faults, transition faults, etc. It can be detected easily with the help of this sequence generator.

The large number of sequences can be generated with the help of cascading the smaller module. It is more efficient than LFSR. The whole designing has done in the 180 nm technology in Cadence's spectre, virtuoso & assura tool.

Keywords – BIST, LFSR, SRAM, sequence generator, and counter.

I. INTRODUCTION
A LFSR is a shift register whose input is the exclusive-or of some of its outputs. The outputs that influence the input are called taps.[1] A maximal LFSR produces an n-sequence, unless it contains all zeros. The tap sequence of a LFSR can be represented as a polynomial mod 2 - called the feedback polynomial. [2] LFSR's can be implemented in hardware. The designing of the shift register is done by the help of D flip-flop. A 4bit LFSR generates the sequence of 0000, 0001, 0010, 0011…up to 1111. This sequence has the transition from 0-1 and 1-0 of the bits.

The problem in using the LFSR in the BIST design was that the extra sequences which are generated by the LFSR which consumes the power and lowered the speed of the testing this simultaneously degrade the performance of peripherals used for testing. [3] In the testing of memory the transition of the 1 to 0 and 0 to 1 is needed which is generated by the sequence generator properly but on the other hand the LFSR generates the various sequences which are not needed for the detection purpose.

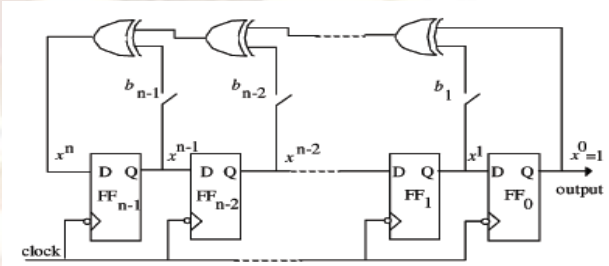

Figure 1. Simplified circuit of a generic n-bit LFSR.

Hardware implementation of the PRBGs is almost always made up of the well-known linear-feedback shift register (LFSR) [5], whose generic circuit is reported in Figure 1. Simplified circuit of a generic n-bit LFSR are useful in many areas of digital design and science.[2] LFSR is the most common used topology to implement PRBG. It is obtained with an array of FFs with a linear feedback performed by several XOR gates. They are based on a rather complex mathematical theory [6]. A 3-stage LFSR is characterized by its feedback polynomial [4]-[11]

$$P(x) = 1 + x2 + x3 \ldots \text{(i)}$$

Various works has been done on the architecture design of the LFSR. The work which has done in this paper is novel. This sequence generator is the replacement of the LFSR in hardwired SRAM BIST. This will give a new direction for the fast and synchronized sequence generation for the BIST applications. This paper describes how the sequence generation is done by this novel circuit.

II. SEQUENCE GENERATOR
The sequence generated by the sequence generator is done by also gives this transition of bits. The sequences which are generated by this sequence

generator are as follows 0000, 1111, 0001, 1110, 0010, 1101, 0011,1100,0100,1011, 0101, 1010, 0110, 1001, 0111 and 1000.

The sequence generator is formed by the help of up and down counter, the sequence switches from the up counter sequence to down counter sequence with the help of a switching circuit. Switching from the up counter sequence to down counter is done by the conventional circuit. The conventional circuits are used here so the delay is less which corresponds to the increases in the speed. As soon as the input will change the output will also change accordingly. So the fast sequence generation can be done easily. On the other hand a huge testing sequence are not required because the needed transition from 1-0 & 0-1 is got by small numbers of sequences hence it produce chance to decrease the testing time of the SRAM.

It is useful for a huge number of inputs because by the help of the cascading we can generate the necessary transitions for the testing purpose.

III. PARTS OF SEQUENCE GENERATOR

There has a combination of up and down Counter. The designing of the up counter (4bit) is done by the help of the JK flip flop and NAND gate for resetting. The resetting of the up counter is needed because there is only need to count 0 to 7. Similarly, the down counter (4bit) is done by the help of the JK flip flop and AND gate for resetting. The presetting of the down counter is needed because there is only need to count F to 8.

In this way the counter has been designed which has a control signal. It controls the up and down counter by switching the up and down counter alternatively. That means when the control signal is high the up counter's output goes to the output and when the control signal is low the down counter's output goes to the output. By the help of this procedure only the bit sequence of 0, F, 1, E, 2, D, 3, C, 4, B, 5, A, 6, 9, 7, 8 can be achieved.

The sequences can be generated for 8 bit counter by cascading the resultant 4 bit counter results. For 8bit the sequence is as follows 00, FF, 11, EE, 22, DD, 33, CC, 44, BB, 55, AA, 66, 99, 88, 77.

IV DESIGN OF CIRCUITS

IV.I SCHEMATIC DESIGN OF CIRCUITS

IV.I.I UP COUNTER

The up counter designing deals with the integration of the JK flip-flop and the 4 bit NAND gate for resetting purpose. In this circuit only one input pin and four output pins they are Q_0, Q_1, Q_2 & Q_4. The below shown diagram give the detailed view of the circuit of the up counter.

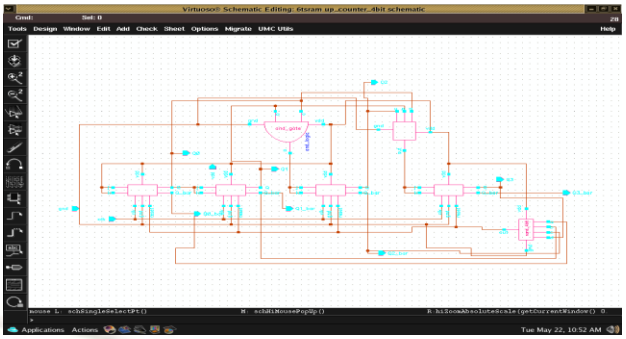

FIG. IV.I.I schematic design of up counter

IV.I.II DOWN COUNTER

The down counter designing deals with the integration of the JK flip-flop and the 4 bit AND gate for presetting purpose. In this circuit only one input pin and four output pins they are Q_0, Q_1, Q_2 & Q_4. The below shown diagram give the detailed view of the circuit of the up counter.

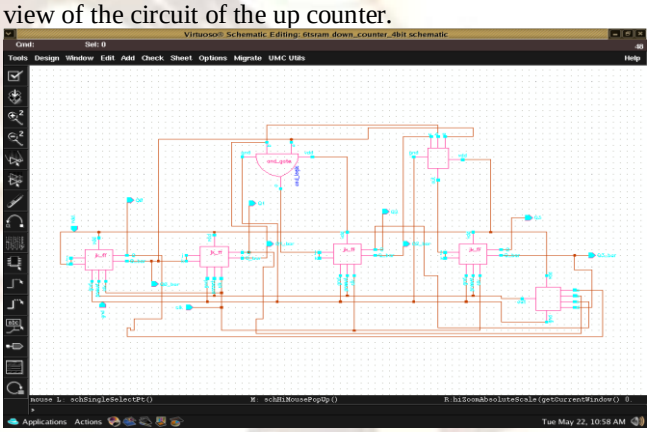

FIG. IV.I.II schematic design of down counter

IV.I.III SEQUENCE GENERATOR

The design of the sequence generator has done by the help of alternating turning on the up counter and down counter with the help of the switching circuit, as shown below.

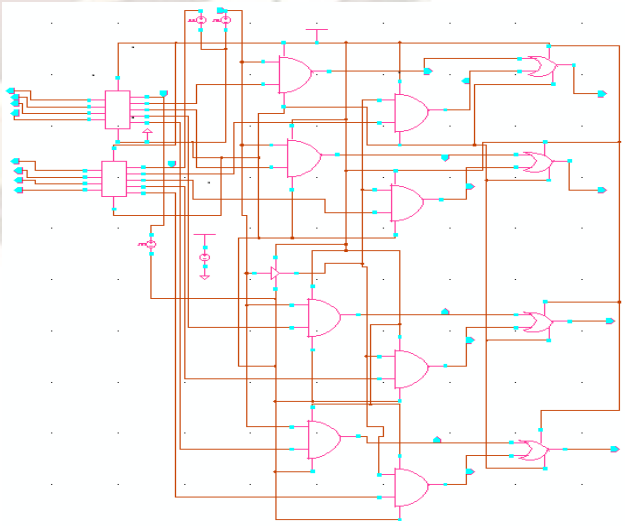

FIG. IV.I.III schematic design of sequence generator

IV.II TEST BENCH OF CIRCUITS

The test bench shows the biasing of the circuits and it is useful for taking the simulated responses of the circuit.

IV.II.I UP COUNTER

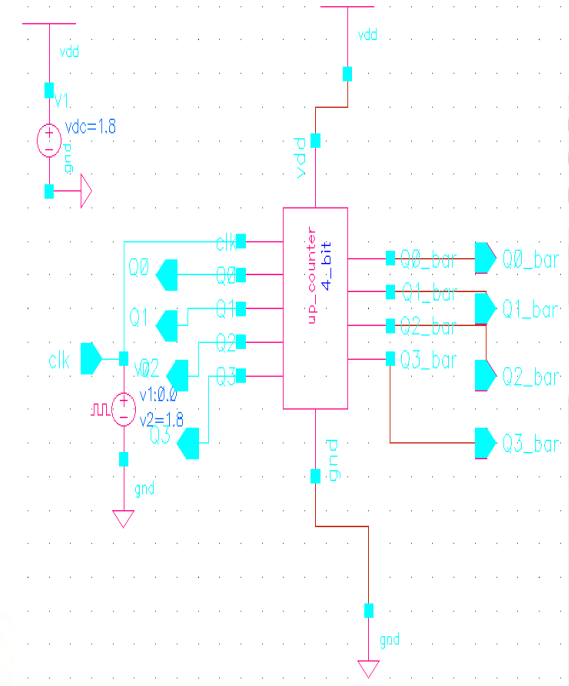

FIG. IV.II.I Test Bench of up counter circuit

IV.II.II DOWN COUNTER

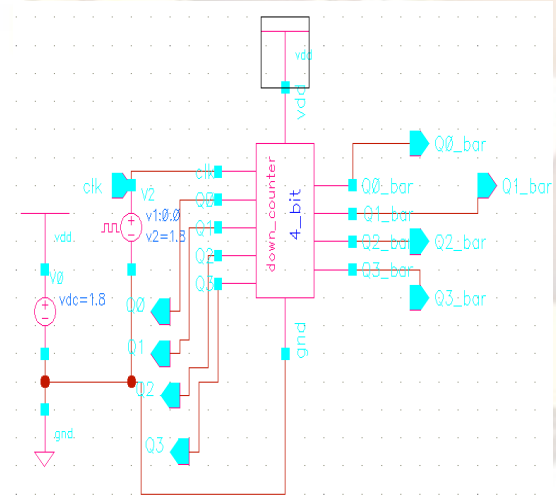

FIG. IV.II.II Test Bench of down counter circuit

IV.II.III SEQUENCE GENERATOR

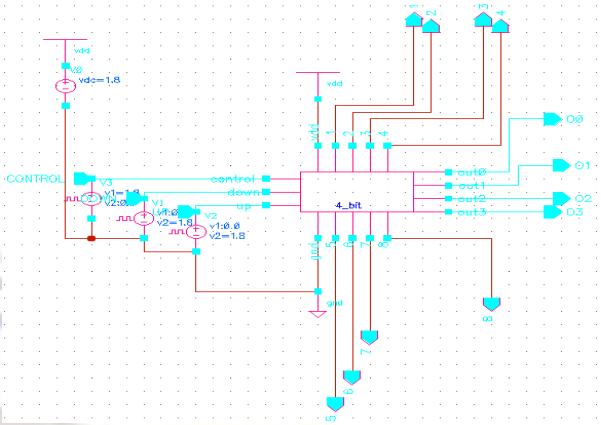

FIG. IV.II.III Test Bench of sequence generator

IV.III LAYOUT OF CIRCUITS

The layout of the blocks and the pattern sequence are as follows.

IV.III.I UPCOUNTER

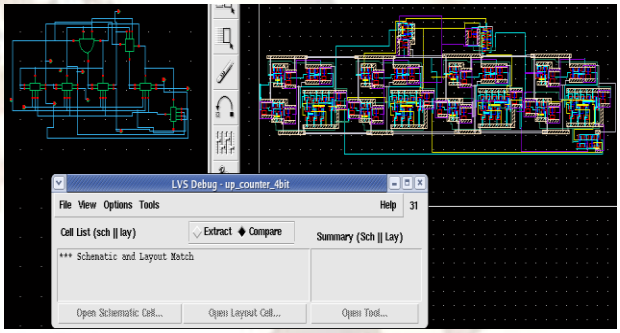

FIG. IV.III.I Layout of up counter

IV.III.II DOWN COUNTER

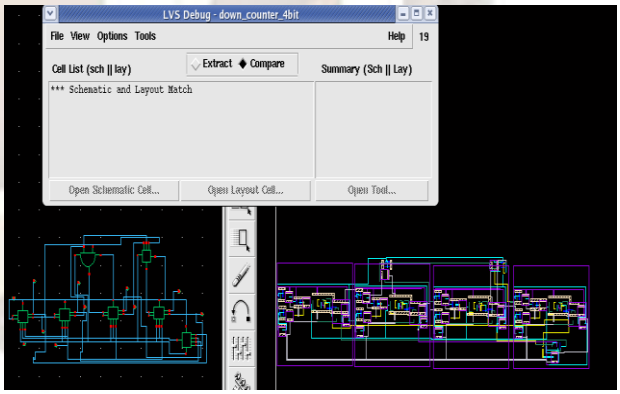

FIG. IV.III.II Layout of down counter

IV.III.III SEQUENCE GENERATOR

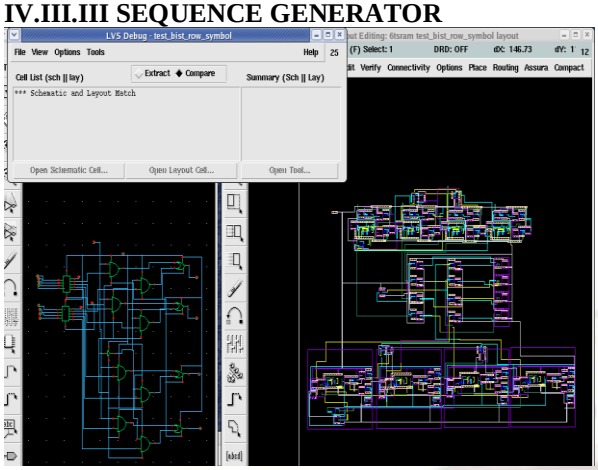

FIG. IV.III.III Layout of sequence generator

V. SIMULATION AND RESULTS

V.I UP COUNTER

The simulation of the up and down counters is as follows

FIG. V.I Simulated Result of up counter

V.II DOWN COUNTER

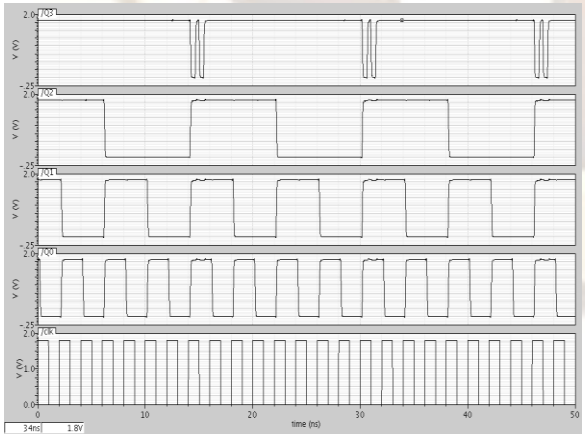

FIG. V.II Simulated Result of down counter

V.III SEQUENCE GENERATOR

The whole sequence generator is designed by the help of the counters. The sequences of the address are shown below. The 4bit output of the counter is given in which it can be seen that the sequence follows as 0, F, 1, E, 2, D, 3, C, 4, B, 5, A, 6, 9, 8, 7 respectively. The simulation results of the sequence generator are as follows

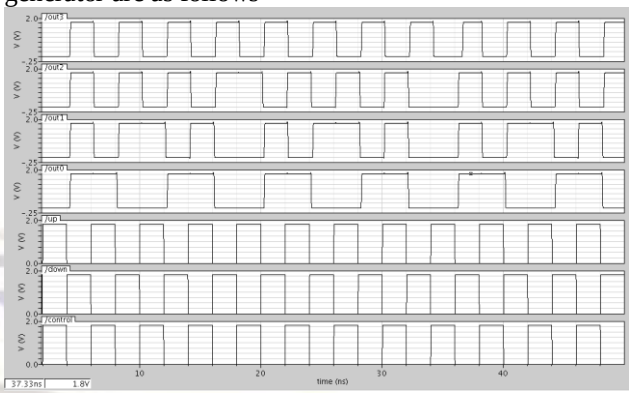

FIG. V.I Simulated Result of Sequence Generator

VI. TABULATED RESULTS

The below results shows the power and area which is calculated by spectre and virtuoso tools respectively.

S. No.	Component	Power	Area
1	Up-Counter	255µW	0.0085mm^2
2	Down-Counter	292µW	0.024mm^2
3	Sequence Generator	440µW	0.0556mm^2

VII. CONCLUSION

The sequence generator has comparatively lower power and area with respect to LFSR. The testing time of SRAM is reduced by the help of this sequence generator because all the pattern sequence which has required for testing are generated in less duration of time. As we say that for 8 address the LFSR generates 2^8 sequences but the pattern generator used by cascading. It can produce 16 sequences which is sufficient for testing. The power and area of whole BIST circuit is given as 440µW and 0.0556mm^2.

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