A Perspective of Gate-Leakage Reduction in Deep Sub-Micron Ics

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ABSTRACT

Before the CMOS process is scaled into deep sub-micron process, dynamic energy loss has always dominated power dissipation, while leakage power is little. The aggressive scaling of device dimensions and threshold voltage has significantly increased leakage current exponentially, thus the MOS devices will no longer be totally turned-off anymore. The power dissipation caused by leakage current can't be neglected anymore, which attracts extensive attentions. Based on the fact that PMOS transistors have an order of magnitude smaller gate leakage than NMOS ones, it is used for designing circuit for reducing gate leakage power. Series of iterative steps are carried out to find the design perspective effect in different technologies.

Keywords: ***ECB, Gate leakage, HVB, PDCVSL, PCPL.***

I. INTRODUCTION

With the substantial growth in portable computing and wireless communication in the last few years, power dissipation has become a critical issue. Problems with heat removal and cooling are worsening because the magnitude of power dissipated per unit area is growing with scaling. Years ago, portable battery-powered applications were characterized by low computational requirement. Nowadays, these applications require the computational performance similar to as non-portable ones. It is important to extend the battery life as much as possible. For these reasons power dissipation becomes a challenge for circuit designers and a critical factor in the future of microelectronics. There are three components of power dissipation in digital CMOS Circuits, namely dynamic, short circuit and leakage power dissipation.

Dynamic switching power dissipation is caused by charging capacitances in the circuit during each low-to-high output transition, by the load capacitance. The dynamic switching power dissipation was the dominant factor compared with other components of power dissipation in digital CMOS circuits for technologies up to 0.18µm, where it is about 90% of total circuit dissipation.

With the technology scaling, supply voltage needs to be reduce due to dynamic power and reliability issues. However, it requires the scaling of the device threshold voltage (*Vth*) to maintain a reasonable gate over drive . The *Vth* reduction, result in an exponential increase in the subthreshold current. Moreover, to control the short channel effects (SCEs) and to maintain the transistor drive strength at low supply voltage, oxide thickness needs to be also scaled down. The aggressive scaling of oxide thickness results in a high tunneling current through the transistor gate insulator. Furthermore, scaled devices require the use of the higher substrate doping density. It causes significantly leakage current through these drain- and source-to substrate junctions under high reversed bias.

Leakage current Mechanism

For nanometer devices, leakage current is dominated by subthreshold leakage, gate-oxide tunneling leakage and reverse-bias pn-junction leakage. Those three major leakage current mechanisms are illustrated in fig1.

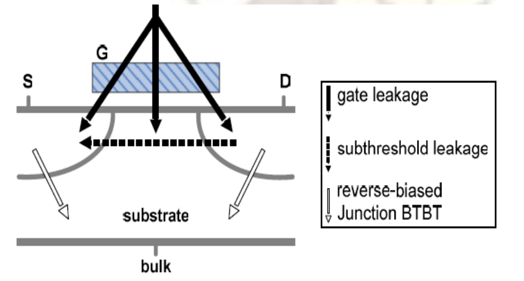

Fig1: Major leakage mechanisms in MOS transistor.

Subthreshold Current

Supply voltage has been scaled down to keep dynamic power consumption under control. To maintain a high drive current capability, the threshold voltage (*Vth*) has to be scaled too. However, the *Vth* scaling results in increasing subthreshold leakage currents. Subthreshold current occurs between drain and source when transistor is operating in weak inversion region, i.e., the gate voltage is lower than the *Vth*. The drain-to-source current is composed by drift current and diffusion current. The drift current is the dominant mechanism in strong inversion regime, when the gate-to-source voltage exceeds the *Vth*. In weak inversion, the minority carrier concentration is almost zero, and the channel has no horizontal electric field, but a small longitudinal electric field appears due the drain-to-source voltage. In this situation, the carries move by diffusion between the source and the drain of MOS Transistor. Therefore, the subthreshold current is dominated by diffusion current and it depends exponentially on both gate-to-source and threshold voltage.

Gate Oxide Tunneling Current

As mentioned before, the aggressive device scaling in nanometer regime increases short channel effects such as DIBL and *Vth* roll-off. To control the short channel effects, oxide thickness must also become thinner in each technology generation. Aggressive scaling of the oxide thickness, in turn, gives rise to high electric field, resulting in a high direct-tunneling current through transistor gate insulator. The tunneling of electrons (or holes) from the bulk and source/drain overlap region through the gate oxide potential barrier into the gate (or vice-versa) is referred as gate oxide tunneling current. This phenomenon is related with the MOS capacitance concept. There are three major gate leakage mechanisms in a MOS structure. The first one is the electron conduction-band tunneling (ECB), where electrons tunneling from conduction band of the substrate to the conduction band of the gate (or vice versa). The second one is the electron valence-band tunneling (EVB). In this case, electrons tunneling from the valence band of the substrate to the conduct band of the gate. The last one is known as hole valence-band (HVB) tunneling, where holes tunneling from the valence band of the substrate to the valence band of the gate (Or vice- versa). Reduction of gate oxide thickness results in an increase in the field across the oxide. The high electric field coupled with low oxide thickness results in tunneling of electrons from inverted channel to gate (or vice versa) or from gate to source/drain overlap region (or vice versa) . There are two types of different tunneling, namely direct tunneling and Fowler-Nordheim (FN) tunneling. The gate leakage of micro device comes mostly from direct tunneling. In scaled devices (with oxide thickness <3 nm), the tunneling mechanism occurs through the trapezoidal energy barrier and known as the direct tunneling. The direct tunneling occurs when the potential drop across the oxide ΦOX is less than the SiO2-Si conduction band energy difference ΦOX.

Reverse Biased Leakage current

The MOS transistor has two pn junctions – drain and source to well junctions. These junctions are typically reverse biased, causing a pn junction leakage current. This current is a function of junction area and doping concentration. When ‘n’ and ‘p’ regions are heavily doped, band-to-band tunneling (BTBT) leakage dominates the reverse biased pn junction leakage mechanism. A high electric field across a reverse biased pn junction causes a current flow through the junction due to tunneling of electrons from the valence band of the p-region to the conduction band of the n-region as shown in fig2.

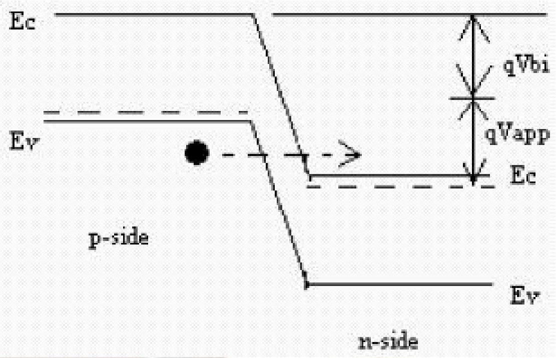

Fig2: BTBT in reverse-biased pn junction.

Logical families targeted to reduce static power are DCVSL (differential cascade voltage switch logic), CPL(complementary pass transistor logic).

Complementary Pass transistor logic (CPL)

Complementary Pass transistor logic (CPL) was developed by Hitachi. It allows primary inputs to drive gate terminals as well as source-drain terminals of NMOS. The promise of this approach is fewer numbers of transistors are required to implement a given function. Since circuits are differential complementary data inputs and outputs are available which eliminates the need for inverters. The design is very modular, all gates use the same topology only the inputs are permuted which makes the design of cell library very simple. The disadvantage of this family is that it suffers from voltage drop problems due at the node which requires additional circuits to compensate the voltage drop

The complexity of CMOS pass-gate logic can be reduced by dropping the PMOS transistors and using only NMOS pass transistors (named CPL) In this case, CMOS inverters (or other means) must be used periodically to recover the full V_{DD} level since the NMOS pass transistors will provide a V_{OH} of VDD – V_{Tn} in some cases. The CPL circuit requires complementary inputs and generates complementary outputs to pass on to the next CPL stage. A AND/NAND implementation in CPL is shown in fig 3

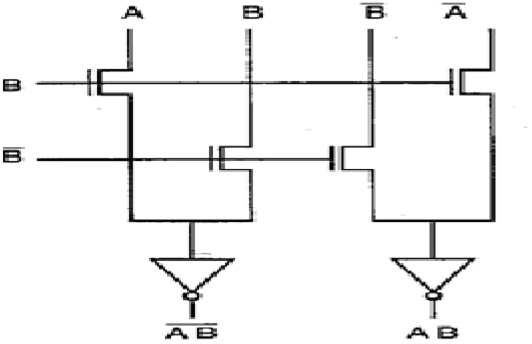

Fig 3: CPL AND/NAND logic

DCVSL (Differential cascade voltage switch logic)

Cascade Voltage Switch Logic (CVSL) was developed in IBM as an improvement over the use of pseudo NMOS. It comes in two forms: single output and differential output (or Double rail). The later form of the logic is also called DCVSL (Differential Cascade Voltage Switch Logic). DCVSL is made of two N type switching networks, one implementing out and the other outbar, and of two P type transistors, connected in a cross-coupled combination to *Vdd*, used as pull-up devices. The advantage of DCVS logic is that both polarities of the output are represented, and thus inversion operation is not necessary. This eliminates the need for the inverter and makes this type of logic inherently faster.

One problem of DCVSL is that since PMOS transistors are the only pull-up devices, there may be a time window during which both the PMOS and the NMOS are ON. This situation will create a current from *Vdd* to ground node causing current spikes and additional delay. The block diagram is shown in fig4

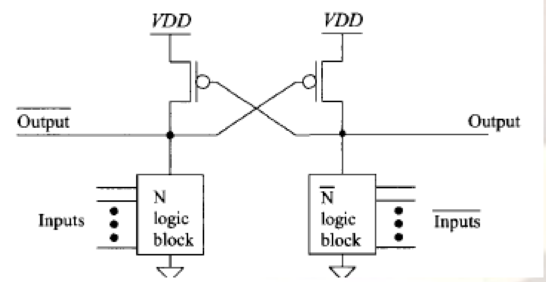

Fig4: Block diagram of DCVSL

P-Type Circuits for reducing leakage current P-CPL and P-DCVSL

There are three major mechanisms for direct tunneling in MOS devices, namely electron tunneling from the conduction band (ECB), electron tunneling from the valence band (EVB), And hole tunneling from the valance band (HVB). In NMOS, ECB controls the gate to channel tunneling current in inversion, whereas gate to body tunneling is controlled by EVB in depletion-inversion and ECB in accumulation. In Pchannel MOSs, HVB controls the gate to channel leakage in inversion, whereas gate-to-body leakage is controlled by EVB in depletion-inversion and ECB in accumulation. Since the barrier height for HVB (4.5eV) is considerably higher than the barrier height for ECB (3.1eV), the tunneling current associated with HVB is much less than the current associated with ECB. This results in a lower gate leakage current in PMOS than NMOS. Based on this fact, the circuits consist mostly of PMOS transistors can reduce gate leakage power. P-DCVSL and P-CPL inverter is shown in figure 5 and 6 respectively.

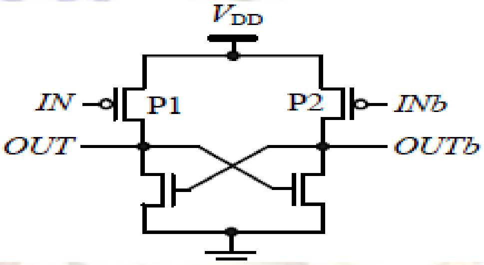

Fig5: P-Type DCVSL Inverter circuit

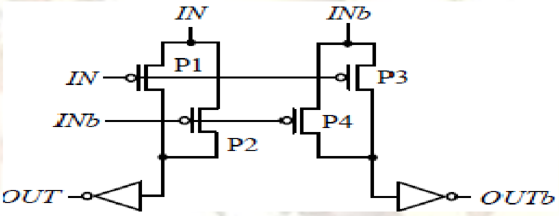

Fig6: P-Type CPL inverter.

II. PERFORMANCE TEST RESULTS

Technology	Power(uW)	Static Power(uW)	Delay(ns)	PDP
90nm	221.832	2.928	1.998	443.20
45nm	80.898	0.669	2.101	54.120
32nm	37.571	0.462	2.204	17.533

Table 1: Performance comparison of PDCVSL full adder at 200MHZ

Technology	Power(uW)	Static Power(uW)	Delay(ns)	PDP
90nm	509.84	815.61	2.606	1019.68
45nm	169.87	291.63	2.486	420.134
32nm	64.40	107.201	3.109	202.219

Table 2: Performance comparison of PCPL full adder at 200MHZ

At 45nm, P-CPL can save 55% and 35%, and P-DCVSL can save 40% and 11% of static power consumption and total power respectively. At speed, because of using PMOS topology, P-type full adders have a slightly large delay. However, PDP of the PCPL full adder is the smallest among all full adders, since its static power consumption is reduced greatly.

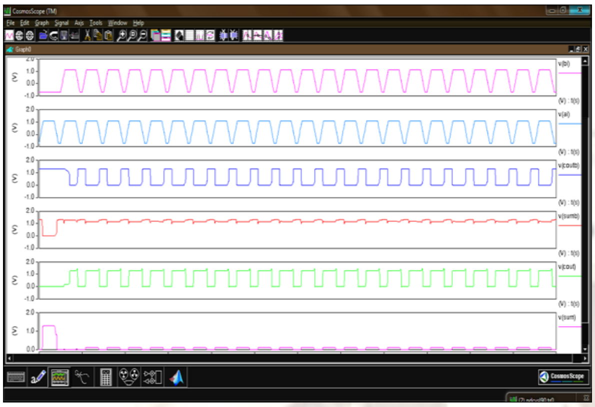

Fig7: Waveform of PDCVSL full adder in 90nm

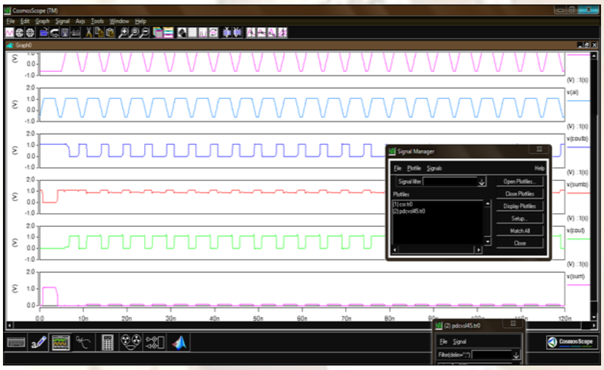

Fig8: Waveform of PDCVSL full adder in 45nm

Fig9: Waveform of PDCVSL full adder in 32nm

Fig10: Waveform of PCPL full adder in 90nm

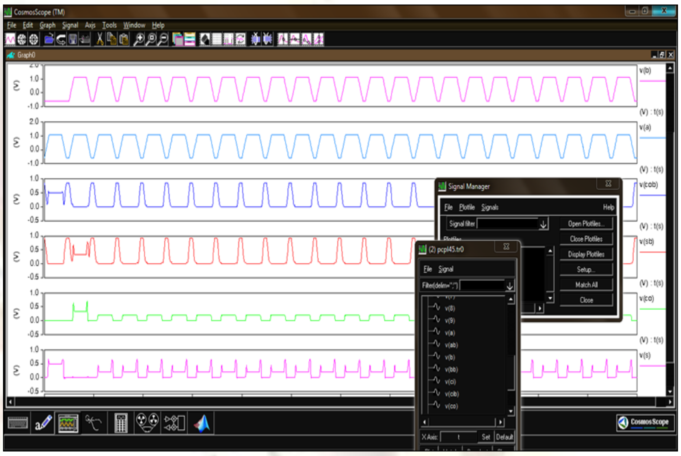

Fig11: Waveform of PCPL full adder in 45nm

Fig12: Waveform of PCPL full adder in 32nm

III. CONCLUSION

Based on the characteristic that the PMOS has low leakage current, P-type complementary pass-transistor logic (P-CPL) and P-type differential cascade voltage switch logic (PDCVSL) achieves considerable energy savings over the CMOS implementation. Although there is a little performance penalty, the static power can be reduced considerably. This design idea could provide a significance reference for reducing gate leakage in deep sub-micron ICs in the coming years.

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