

An Improvement Of Transient Current Response Of Load Transformers For The Series Voltage Sag Compensator

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ABSTRACT

Power quality is one of major concerns in the present era. According to Survey results it shows that 92% of interruption at industrial facilities are caused due to voltage sag related. The DVR (Dynamic voltage restorer) is a series connected device whose function is to protect a sensitive industrial load from voltage sags. The voltage sag compensator, based on a transformer-coupled is connected in series to voltage source inverter, is among the most cost-effective solution against voltage sags. To mitigate the problems caused by poor quality of power supply, series compensators are used. Transformers are often installed in front of critical loads for electrical isolation purposes. When voltage sags happen, the transformers are exposed to the disfigured voltages and a DC offset will occur in its flux linkage. When the compensator restores the load voltage, the flux linkage will be driven to the level of magnetic saturation and severe inrush current occurs. The compensator is likely to be interrupted because of its own over-current protection, and eventually the compensation fails, and the critical loads are interrupted by the voltage sag. This paper proposes an improvement of transient current response using inrush current mitigation technique of load transformer together with a state feedback controller for the voltage sag compensator. The operation principles of the proposed method are specifically presented, and experiments are provided to validate the proposed approach.

Keywords: DVR, Flux Linkage, inrush current, load transformer, power quality, series compensator, voltagesag

I. INTRODUCTION

Power quality and reliability are essential for operation of industrial process which involve in critical sensitive loads. The Power quality in the distribution system can be improved by using a custom power device DVR for voltage disturbances such as voltage sags, harmonics, and unbalanced voltage.[1] The DVR (Dynamic voltage restorer) is a series connected device whose function is to protect sensitive industrial load from voltage sags.

A voltage sag as defined by IEEE Standard 1159-1995, IEEE Recommended Practice for Monitoring Electric Power Quality, is a decrease in RMS voltage at the power frequency for durations from 0.5 cycles to 1 minute, reported as the remaining voltage. The measurement of a voltage sag is stated as a percentage of the nominal voltage, it is a measurement of the remaining voltage and is stated as a sag to a percentage value. Thus a voltage sag to 60% is equivalent to 60% of nominal voltage, or 288 volts for a nominal 480 Volt system [2][3]. Voltage sags are caused due to short circuits, starting large motors, sudden changes of load, and energization of transformers are the main causes of voltage sags [4]. Voltage sags often interrupt critical loads and results in substantial productivity losses. The DVR is a voltage sag compensator based on a voltage source inverter (VSI). The voltage sag compensators have been one of the most cost-effective voltage sag ride-through solutions.

Several closed-loop control techniques have been proposed for voltage source inverter-based sag compensators [5-7]. Transients can be currents or voltages which occur momentarily and fleetingly in response to a stimulus or change in the equilibrium of a circuit. Transients frequently occur when power is applied to or removed from a circuit, because of expanding or collapsing magnetic fields in inductors or the charging or discharging of capacitors. In this paper, the inrush issue of load transformers under the operation of the sag compensator is presented. An improvement of transient current response along with inrush mitigation technique is proposed and implemented in a synchronous reference frame with a sag compensator controller. The proposed technique can be integrated with the conventional closed-loop control on load voltages.

The new integrated control can successfully reduce inrush current of load transformers and improve the disturbance rejection capability and the robustness of the sag compensator system. Laboratory test results are presented to validate the proposed technique.

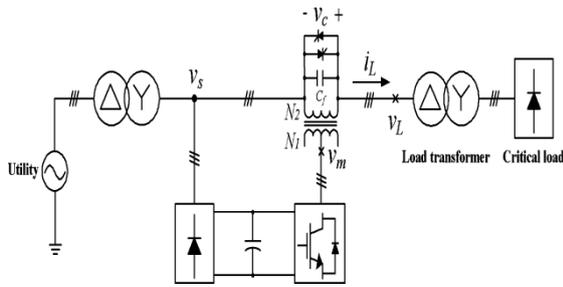


Fig. 1. Simplified one-line diagram of the offline series voltage compensator.

As shown in Fig. 1, the voltage sag compensator consists of a three phase voltage source inverter (VSI) and a coupling transformer for serial connection [8-10]. When the grid is normal, the compensator is bypassed by the thyristors for high operating efficiency. When voltage sags occur, the voltage sag compensator injects the required compensation voltage through the coupling transformer to protect sensitive loads from being interrupted by sags. However, certain detection time (typically within 4ms) is required by the sag compensator controller to identify the sag event [11]. And the load transformer is exposed to the deformed voltage from the sag occurrence to the moment when the compensator restores the load voltage. Albeit its short duration, the deformed voltage causes magnetic flux linkage deviation inside the load transformer, and magnetic saturation may easily occur when the compensator restores the load voltage, thus results in inrush current. The inrush current could trigger the over-current protection of the compensator and lead to compensation failure. Thus this paper proposes inrush mitigation technique by correcting the flux linkage offsets of the load transformer. And this technique can be seamlessly integrated with the state feedback controller of the compensator.

II. DYNAMIC VOLTAGE RESTORER

Dynamic Voltage Restorer (DVR) is a recently proposed seriesconnected solid state device that injects voltage into the system in order to regulate the load-side voltage. The DVR was first installed in 1966 [12]. It is normally installed in a distribution system between the supply and the critical load feeder [13]. Its primary function is to boost up the load-side voltage in the event of a disturbance in order to avoid any power disruption to that load [14,15]. There are various circuit topologies and control schemes that can be used to implement a DVR. In addition to voltage sags and swells compensation, a DVR can also perform other tasks such as: line voltage harmonics compensation, reduction of transients in voltage and fault current limitations. The general configuration of a DVR consists of an injection / booster transformer, a

harmonic filter, a voltage source converter (VSC), DC charging circuit and a control and protection system as shown in Fig. 2. In most sag correction techniques, the DVR is required to inject active power into the distribution line during the period of compensation. Hence, the capacity of the energy storage unit can become a limiting factor in the disturbance compensation process especially for sags of long duration.

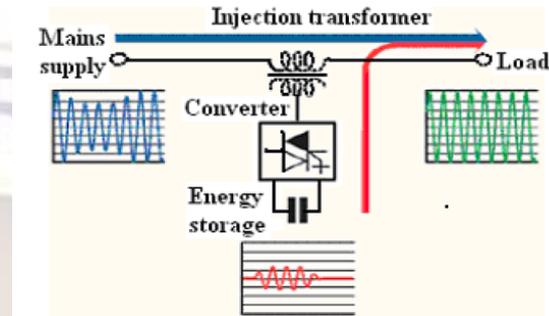


Fig.2 Principle of DVR

III. SYSTEM CONFIGURATION OF THE PROPOSED COMPENSATOR

The leakage inductor of coupling transformer L_f and capacitor C_f is recognized as the low pass filter to suppress Pulse width modulation [PWM] ripples of the inverter output voltage v_m . Figure 3 shows the equivalent circuit of series voltage sag compensator and its dynamic equation can be expressed as (1) and (2).

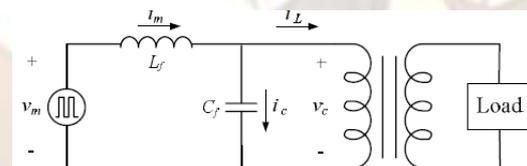


Fig. 3 Per-phase equivalent circuit of series voltage sag compensator

$$L_f \frac{d}{dt} \begin{bmatrix} i_{ma} \\ i_{mb} \\ i_{mc} \end{bmatrix} = \begin{bmatrix} v_{ma} \\ v_{mb} \\ v_{mc} \end{bmatrix} - \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} \quad (1)$$

$$C_f \frac{d}{dt} \begin{bmatrix} v_{ca} \\ v_{cb} \\ v_{cc} \end{bmatrix} = \begin{bmatrix} i_{ma} \\ i_{mb} \\ i_{mc} \end{bmatrix} - \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (2)$$

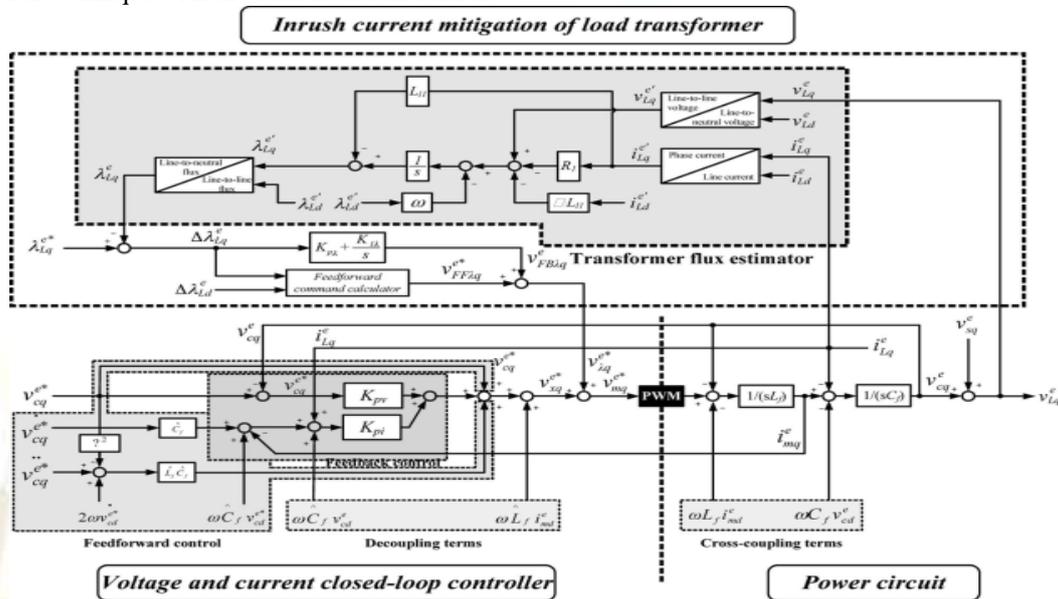
Where $[v_{ma} v_{mb} v_{mc}]^T$ is the inverter output voltage, $[v_{ca} v_{cb} v_{cc}]^T$ is the compensation voltage, $[i_{ma} i_{mb} i_{mc}]^T$ is the filter inductor current, and $[i_{La} i_{Lb} i_{Lc}]^T$ is the load current. Equation (1) and (2) are transferred into the synchronous reference frame as (3) and (4).

$$\frac{d}{dt} \begin{bmatrix} i_{mq}^e \\ i_{md}^e \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \begin{bmatrix} i_{mq}^e \\ i_{md}^e \end{bmatrix} + \frac{1}{L_f} \begin{bmatrix} v_{mq}^e \\ v_{md}^e \end{bmatrix} - \frac{1}{L_f} \begin{bmatrix} v_{cq}^e \\ v_{cd}^e \end{bmatrix} \quad (3)$$

$$\frac{d}{dt} \begin{bmatrix} v_{cq}^e \\ v_{cd}^e \end{bmatrix} = \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \begin{bmatrix} v_{cq}^e \\ v_{cd}^e \end{bmatrix} + \frac{1}{C_f} \begin{bmatrix} i_{mq}^e \\ i_{md}^e \end{bmatrix} - \frac{1}{C_f} \begin{bmatrix} i_{Lq}^e \\ i_{Ld}^e \end{bmatrix} \quad (4)$$

current control. The voltage control is implemented by a proportional regulator with voltage command v_{cq}^{e*} respectively produced by the voltage sag scheme.

Fig. 4. Block diagram of the proposed inrush current mitigation technique with the state feedback control.



Where superscript “e” indicates the synchronous reference frame representation of this variable and ω is the angular frequency of the utility grid. Equation (3) and (4) show the cross-coupling terms between compensation voltage and filter inductor current.

IV. THE PROPOSED CONTROL METHOD

The block diagram of the proposed control method is shown in the Figure 4. Note that the d-axis controller is not shown for simplicity. The block diagram consists of the full state feedback controller [16] and the proposed inrush current mitigation technique. Detailed explanations are given in the following sections.

4.1 The full state feedback scheme

The state feedback scheme includes feedback control, feedforward control and decoupling control.

4.1.1 Feedback control

The feedback control is utilized to improve the preciseness of compensation voltage, the disturbance rejection capability and the robustness against parameter variations. As in Fig. 4, the capacitor voltage v_{cq}^e is the voltage control in the outer loop and the inductor current i_{mq}^e is the inner

4.1.2 Feed-forward control

To improve the dynamic response of the voltage sag compensator, the feed forward control is added to the voltage control loop to compensate the load voltage immediately when voltage sag occurs. The feed-forward voltage command can be calculated by combining the compensation voltage and the voltage drop across the filter inductor which is produced by the filter capacitor current.

4.1.3 Decoupling control

Since cross coupling terms derived from the synchronous reference frame transformation and the external disturbances exists in the physical model of voltage sag compensator, the control block utilizes the decoupling control to improve the accuracy and the disturbance rejection ability. Figure 4 shows the decoupling terms is produced by measuring the load current, filter capacitor voltage and the filter inductor current. The cross coupling terms in physical model can be eliminated completely.

4.2. Inrush Current Mitigation Technique

4.2.1 Flux linkage DC offset

The flux linkage is estimated by the measured line voltage. Figure 5 shows a single winding of the delta/ye three-phase load transformer which is installed in downstream of

voltage sag compensator. The fluxlinkage of the phase a-b winding is expressed as
 $\lambda_{Lab}(t) = \int v_{Lab}(t) dt$ (5)

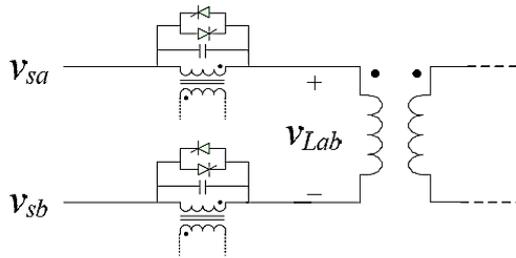


Fig. 5. Connection diagram of the proposed system and delta/ye load transformer.

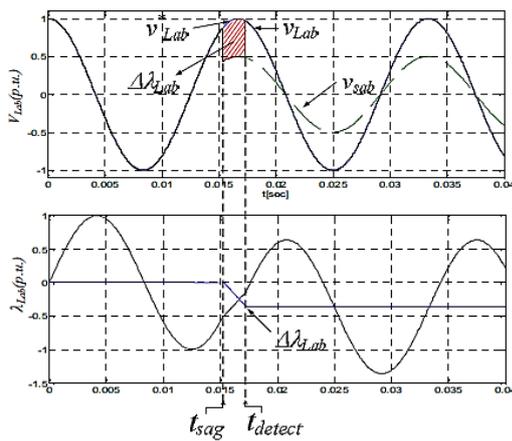


Fig.6. Transformer voltage and corresponding transient flux linkage.

As shown in Figure 6, the line-to-line voltage across the transformer winding and the resulting flux linkage from the sag occurrence to completion of voltage compensation. When voltage sags occurs ($t=t_{sag}$), the controller detects the sagged voltage and injects the required compensation voltage at $t=t_{detect}$. The flux linkage during the voltage compensation process can be express as following:

$$\lambda_{Lab}(t) = \lambda_{Lab}(t)|_{t=t_{sag}} + \int_{sag}^{detect} v_{Lab}(t) dt + \int_{detect} v_{Lab}^*(t) dt \quad (6)$$

This equation can be re-written as

$$\lambda_{Lab}(t) = \lambda_{Lab}(t)|_{t=t_{sag}} - \int_{sag} v_{Lab}^*(t) dt + \int_{sag}^{detect} (v_{Lab}(t) - v_{Lab}^*(t)) dt + \int_{detect} v_{Lab}^*(t) dt \quad (7)$$

Assume the pre-fault load voltage is

$$v_{Lab}^*(t) = \hat{V}_{Lab}^* \sin(\omega t + \Phi_{Lab}^*)$$

Where \hat{V}_{Lab}^* is the magnitude is the magnitude of load voltage, ω is the grid frequency, and Φ_{Lab}^* is the phase angle. Thus, after the voltage compensation is completed, the flux linkage can be expressed as

$$\lambda_{Lab}(t) = \Delta\lambda_{Lab}(t)|_{t=t_{detect}} + \frac{\hat{V}_{Lab}^*}{\omega} \sin(\omega t + \Phi_{Lab}^* - \frac{\pi}{2}) \quad (8)$$

Where

$$\Delta\lambda_{Lab}(t)|_{t=t_{detect}} = \lambda_{Lab}(t)|_{t=t_{sag}} - \lambda_{Lab}^*(t)|_{t=t_{sag}} + \int_{sag}^{detect} (v_{Lab}(t) - v_{Lab}^*(t)) dt \quad (9)$$

for $t_{sag} \leq t < t_{detect}$

Equation (9) states that the sagged voltages cause the flux linkage DC offset $\Delta\lambda_{Lab}$ on the transformer windings, and its magnitude is dependent on the depth and the duration of sags. Severe voltage sag event can drive the DC offset exceeding the magnetic saturation knee and causes high inrush current. In practical saturation, the magnetic saturation knee is usually put on 1.10-1.15 p.u. of state-study flux linkage.

4.2.2 Design the flux linkage estimator

The Figure 7 shows the model of a single transformer under no load, where R_1 is the equivalent resistor of copper loss, L_{l1} is the equivalent leakage inductance, R_c is the equivalent resistor of core losses, and L_m is the magnetic inductance.

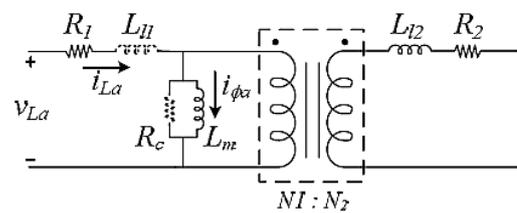


Fig. 7. Equivalent per phase circuit model of the transformer

This dynamics of the transformer equivalent circuit in Fig. 7 can be expressed as

$$\begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} = L_m \frac{d}{dt} \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} + R_1 \begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (10)$$

Note that the leakage inductances and the core losses are neglected for simplifications. This equation can be re-written as

$$\begin{bmatrix} v_{La} \\ v_{Lb} \\ v_{Lc} \end{bmatrix} = \frac{d}{dt} \begin{bmatrix} \lambda_{La} \\ \lambda_{Lb} \\ \lambda_{Lc} \end{bmatrix} + \frac{R_1}{L_m} \begin{bmatrix} \lambda_{La} \\ \lambda_{Lb} \\ \lambda_{Lc} \end{bmatrix} \quad (11)$$

Where $[\lambda_{La}\lambda_{Lb}\lambda_{Lc}]^T=L_m[i_{La}i_{Lb}i_{Lc}]^T$

The dynamics of the transformer flux linkages can be transformed into the synchronous reference frame as

$$\begin{bmatrix} \lambda_{Lq}^e \\ \lambda_{Ld}^e \end{bmatrix} = \int \left(\begin{bmatrix} v_{Lq}^e \\ v_{Ld}^e \end{bmatrix} + \begin{bmatrix} 0 & -\omega \\ \omega & 0 \end{bmatrix} \begin{bmatrix} \lambda_{Lq}^e \\ \lambda_{Ld}^e \end{bmatrix} - \zeta \begin{bmatrix} \lambda_{Lq}^e \\ \lambda_{Ld}^e \end{bmatrix} \right) dt \quad (12)$$

where the damping ratio, $\zeta=R_1/L_m$, decides the transient of the flux linkage. Figure 8 shows the flux linkage estimator under the synchronous reference frame derived from the equation (12).

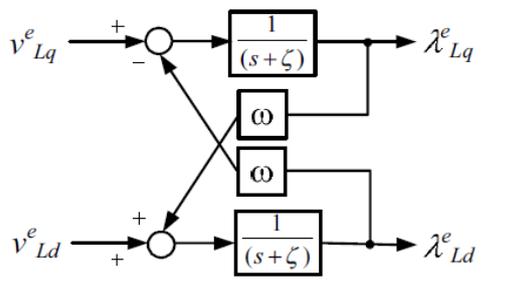


Fig. 8.The flux linkage estimator under the synchronous reference frame.

As shown in Fig. 8, the flux linkage estimator is applied to the proposed inrush mitigation technique. The proposed inrush mitigation method includes feedback control and feedforward control.

In the feedback control loop, the flux linkage λ_{Lq}^e is generated by integrating the load voltage v_{Lq}^e . The deviation of the flux linkage can be calculated by the difference between λ_{Lq}^{e*} and the flux linkage λ_{Lq}^e . The error is regulated by a proportional-integral (PI) regulator.

To speed up the dynamics response of the inrush current mitigation, the error between the estimated flux linkage DC offset and the flux linkage command ($\Delta\lambda_{Lq}^e = \lambda_{Lq}^{e*} - \lambda_{Lq}^e$) is utilized as a feedforward control term. The command is multiplied by a proportional gain K_{pt} ($=1/\Delta T$) to accelerate the DC offset compensation during the compensator start transient. The control gain K_{pt} is selected according to the tolerant of inrush current and the time requirement of flux linkage DC offset compensation.

The summation $v_{\lambda q}^{e*}$ of feedback and

feedforward command is added to the sag compensation voltage command v_{mq}^{e*} to establish the overall command voltage of the voltage sag compensator. Thus, the proposed control method leads the voltage sag compensator to perform an excellent load voltage tracking and prevent the inrush current occurs on the load-side transformer.

V. LABORATORY TEST RESULTS

A prototype voltage sag compensator with inrush current mitigation technique is implemented in laboratory. The one-line diagram is as given in Fig. 1. The system parameters of testbench and controller are given as follows:

- ❖ Source: 220V, 60Hz;
- ❖ Loads: non-linear load ($R=140\Omega$, $L=2.0mH$, $C=3300\mu F$);
- ❖ Voltage sag compensator: a conventional three-phase inverter switching at 10kHz, the leakage inductance of the coupling transformer $L_f=0.32mH$, and filter capacitor $C_f=4.0\mu F$.
- ❖ Load transformer: 3kVA, 220V/220V (Delta/Wye connection)

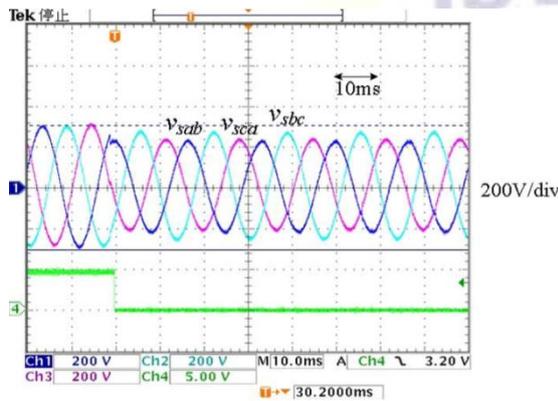
TABLE I
The parameters of the control gains

K_{pv}	K_{pi}	K_{pt}	$K_{p\lambda}$	$K_{I\lambda}$
0.2	3.2	167	304	200

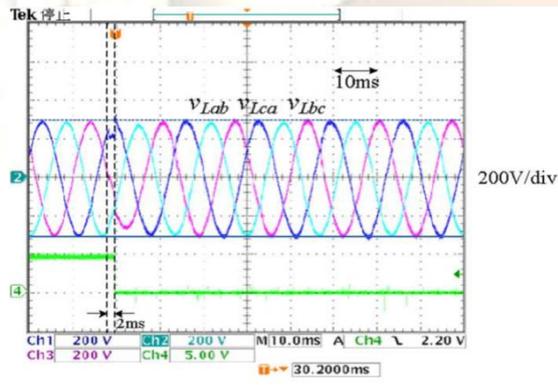
The Figure 9 shows that asymmetrical fault is introduced in utility line, and the experimental results of voltage sag compensator without the inrush current mitigation technique. The controller detects the voltage sag in 4.0ms after the fault occurs, and injects the required compensation voltage immediately to maintain load voltage in normal value as shown in Fig. 9(b). The transformer flux linkage DC offsets caused by the voltage sag can be clearly observed in Fig. 9(c), which results in a significant inrush current of peak value 14A as shown in Fig. 9(d). Figure 9(e) shows the transformer flux linkage under the synchronous reference frame (λ_{Ld}^e). The voltage compensation process causes the flux linkage λ_{Ld}^e oscillate and naturally decays to the normal state by core losses of the transformer and the power consumption of the load.

Under the same asymmetrical fault, Fig. 10 shows the experimental waveforms when the inrush current mitigation technique is utilized in compensation process. Figure 10(a) and (b) illustrate proposed inrush current mitigation technique can achieve fast voltage compensation and without any flux linkage DC offset during the transient compared with Fig. 9(b) and (c). Therefore, the inrush current caused by the voltage sag can be

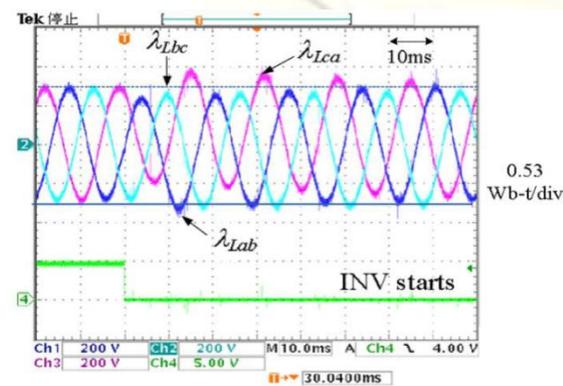
avoided completely compared to Fig. 9(d). Furthermore, Fig. 10(a) also shows that the inrush current mitigation technique generates an extra voltage to correct the trace of transient flux linkage when the compensation is initiated compared to Fig. 9(c). The magnitude of the extra voltage is usually dependent on proportion gain K_λ . Figure 10(d) shows the tracking performance of proposed inrush current mitigation technique. The P-I regulator proposed method can be recognized as a virtual damper. A large number of $K_{P\lambda}$ can accelerate the flux linkage λ_{Ld}^e to track the flux linkage command λ_{Ld}^{e*} . However, it may cause a high current in the start transient.



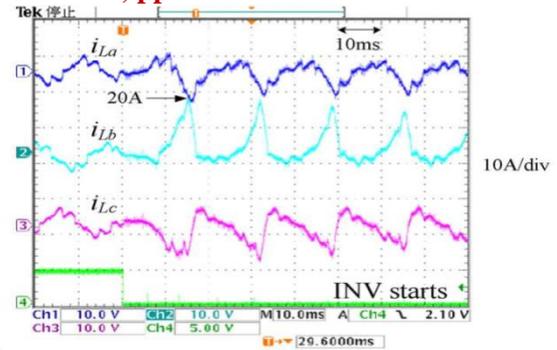
(a) Source voltage v_s



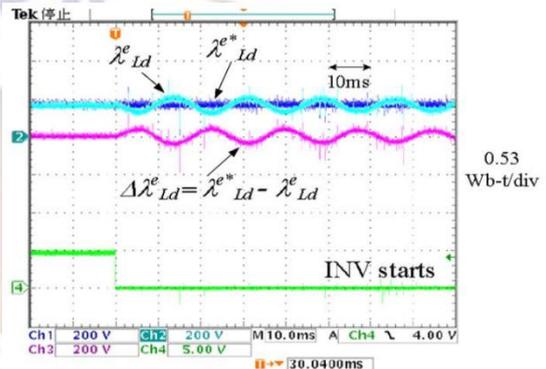
(b) Load voltage v_{L-L}



(c) Flux linkage of the load transformer λ_{L-L}

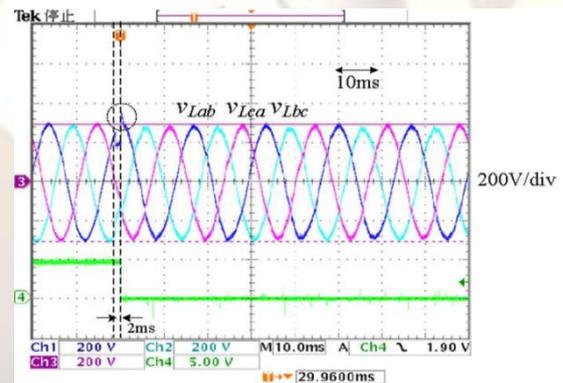


(d) Load current i_L

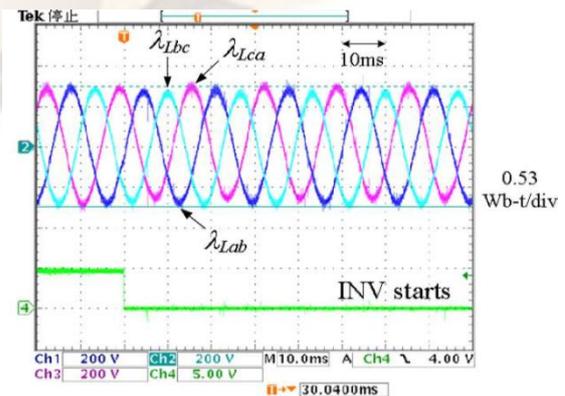


(e) Flux linkage of d axis λ_{Ld}^e

Fig. 9. Experimental waveforms without the inrush current mitigation technique



(a) Load voltage v_{L-L}



(b) Flux linkage of the load transformer λ_{L-L}

VI. THE DISTURBANCE REJECTION CAPABILITY

The stationary referenced frame control design [17] causes a steady-state tracking error on the load voltage. Moreover, the control gain limitation constricts the compensator capability about disturbance rejection [7]. The synchronous reference frame implementation of the proposed state feedback controller can effectively enhance the disturbance rejection capability compared to the stationary frame feedback controller design [16]. The proposed inrush current mitigation technique utilizes a flux linkage closed-loop control, and this feature elevates even further the disturbance rejection characteristics of the sag compensator for the fundamental frequency load current.

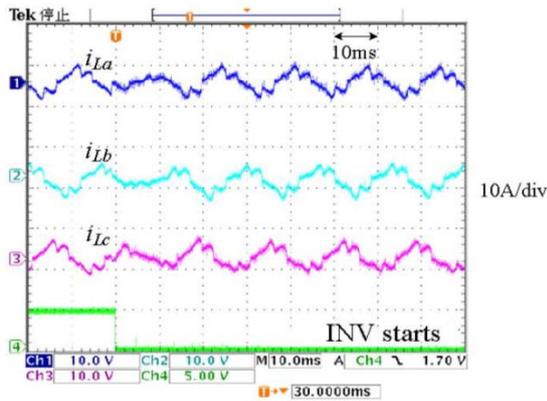
The disturbance rejection capability can be characterized by the transfer function between the compensator output voltage and the load current. Equation (11) and (12) show the disturbance rejection capability of the compensator under the conventional voltage-current state feedback controller and the proposed inrush current mitigation technique integrated with state feedback controller respectively.

$$\left| \frac{i_{Ld}^e(s)}{v_{eq}^e(s)} \right| = \frac{L_f C_f s^3 + K_{pi} C_f s^2 + (K_{pv} K_{pi} + 1)s + K_N K_{pi}}{L_f s^2} \quad (11)$$

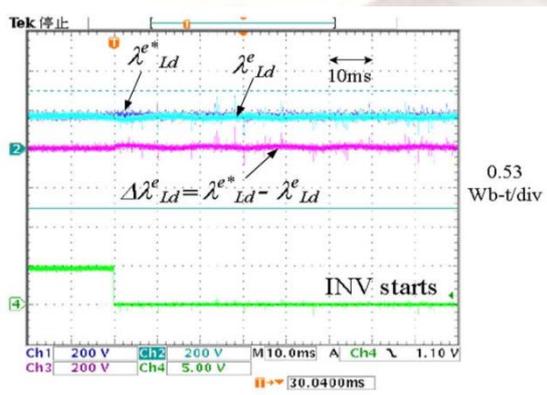
$$\left| \frac{i_{Ld}^e(s)}{v_{eq}^e(s)} \right| = \frac{L_f C_f s^4 + K_{pi} C_f s^3 + (K_{pv} K_{pi} + 1)s^2 + K_{pi} s + K_N}{L_f s^3} \quad (12)$$

Note that three assumptions are made for simplicity, namely 1) cross-coupling terms in physical model has been decoupled by the controllers, 2) and the utility voltage is a voltage stiff, 3) the parameter of proportion gain is selected as $K_{p\lambda} = K_{iv} K_{pi}$.

Figure 12 illustrates a Bode diagram of the both the transfer functions. The figure shows that the system is very critical in shaping the Bode diagram of this disturbance rejection transfer function if the inrush current mitigation technique is integrated with controllers. This advantage benefits the power quality of the compensator output voltage. Analysis of the experimental results shows that the total harmonic distortion (THD) of load voltage without inrush current mitigation is 5.49% and with inrush current mitigation is 5.16%. The TABLE II summarizes the relationship between the error of fundamental component of load voltage and control gain $K_{D\lambda}$. The rejection ratio of the fundamental frequency can be increased by selecting a high control gain $K_{D\lambda}$.



(c). Load current i_L



(d). Flux linkage of d axis λ_{Ld}^e

Fig.10. Experimental waveforms with the inrush current mitigation technique

Figure 11 makes a comparison between the proportion gain $K_{p\lambda}$ and flux linkage tracking error ($\lambda_{Ld}^{e*} - \lambda_{Ld}^e$). As the figure shows that the tracking error approaches steady state very quickly as a high $K_{p\lambda}$ is selected as control gain. Moreover, the higher $K_{p\lambda}$ can benefit the disturbance rejection capability in the range between fundamental frequency and middle frequency. More details will be discussed in the next section.

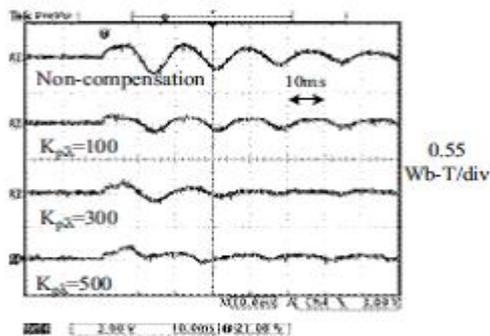


Fig. 11. The flux linkage tracking error between λ_{Ld}^{e*} and λ_{Ld}^e under different control gain $K_{p\lambda}$

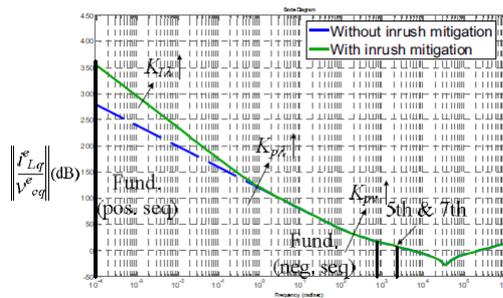


Fig. 12. Comparison between conventional voltage-current state feedback controller and the proposed inrush current mitigation technique integrated with state feedback controller in disturbance rejection capability.

TABLE II

K_D gain	Error of fundamental component of load voltage
Without inrush compensation	2.53%
$K_D=100$	1.18%
$K_D=300$	0.91%
$K_D=1000$	0.88%

VII. CONCLUSION

This paper proposes an improvement of transient current response with inrush current mitigation technique incorporating with the full state feedback controller to prevent the inrush current during the voltage compensation process. The controller includes a voltage control, a current control and a flux linkage control. The proposed control method is based on the synchronous reference frame which enables voltage sag compensator to achieve fast voltage injection and prevent the inrush current. When voltage sag occurs, the controller can track the transient flux linkage and calculate a required compensation voltage in real-time for fast compensation and elimination of flux linkage DC offset caused by voltage sags. The effectiveness of the proposed flux linkage compensation mechanism is validated by laboratory test results. The disturbance rejection characteristics of the proposed method are also examined in the frequency domain for better understanding of the control gains selection and its effect. It shows that the proposed control method provides a high disturbance rejection capability for voltage sag compensator compared with conventional voltage-current state feedback control method. The proposed method can be easily integrated with the existing voltage sag compensation control system without using any extra sensors.

REFERENCES

- [1] Amit Kumar Jena, Bhupen Mohapatra, Kalandi Pradhan, "Modeling and Simulation of a Dynamic Voltage Restorer (DVR)", Project Report, Bachelor of Technology in Electrical Engineering, Department of Electrical Engineering, National Institute of Technology, Rourkela, Odisha-769008
- [2] Roger C. Dugan. Electrical Power Systems Quality. Editorial McGraw-Hill, 1996.
- [3] Ministerio de Economía. Real Decreto 1955/2000 por el que se regulan las actividades de transporte, distribución, comercialización, suministro y procedimientos de autorización de instalaciones de energía eléctrica. BOE, Diciembre 2000.
- [4] Facts Controllers In Power Transmission and Distribution by Padiyar, K.R. , ISBN: 978-81-224- 2142-2: June, 2007.
- [5] J. G. Nielsen, M. Newman, H. Nielsen, and F. Blaabjerg, "Control and testing of a dynamic voltage restorer (DVR) at medium voltage level," IEEE Trans. Power Electron., vol. 19, no. 3, pp. 806–813, May 2004.
- [6] M. Vilathgamuwa, A.A.D. Ranjith Perera, S.S. Choi, "Performance improvement of the dynamic voltage restorer with closed-loop load voltage and current-mode control," IEEE Trans. Power Electron., Vol. 17, on 5, pp. 824 – 834, September 2002.
- [7] M. J. Ryan, W. E. Brumsickle, and R. D. Lorenz, "Control topology options for single-phase UPS inverters," Industry Applications, IEEE Transactions on, vol. 33, pp. 493-501, 1997.
- [8] W. E. Brumsickle, R. S. Schneider, G. A. Luckjiff, D. M. Divan, M. F. McGranaghan, "Dynamic sag correctors: cost-effective industrial power line conditioning", IEEE Transactions on Industry Applications, vol.37, pp. 212-217, Jan.-Feb. 2001.
- [9] D. M. Vilathgamuwa, A. A. D. R. Perera, S. S. Choi, "Voltage sag compensation with energy optimized dynamic voltage restorer", IEEE Transactions on Power Delivery, vol.18, pp.928-936, July 2003.
- [10] Chi-Jen Huang, Shyh-Jier Huang, Fu-Sheng Pai, "Design of dynamic voltage restorer with disturbance-filtering enhancement", IEEE Transactions on Power Electronics, vol.18, pp.1202-1210, Sept. 2003.

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- [11] P.T. Cheng; C. -C. Huang; C. – C. Pan; S. Bhattacharya, “Design and implementation of a series voltage sag compensator under practical utility conditions”, IEEE Trans. Ind. Applicat., Vol. 39, pp. 844-853, May-June 2003.
- [12] B.H. Li, S.S. Choi, D.W. Vilathgamuwa, 2001, “Design Considerations on the line-side filter used in the Dynamic Voltage Restorer,” IEE Proc. Generat. Trans. Distribut., 148(1), pp. 1-7.
- [13] Rosh Omar, NasrudinAbd Rahim, MarizanSulaiman, 2010, “New Control Technique Applied in Dynamic Voltage Restorer for Voltage Sag Mitigation,” American Journal of Engineering and Applied Sciences, 3(1), pp. 858-864.
- [14] K. Chan, 1998, “Technical and Performance Aspects of aDynamic Voltage Restorer,” Proceeding of the IEE Half Day Colloquium on Dynamic Voltage Restorers – Replacing Those Missing Cycles, IEEE Xplore Glasgow, UK, pp. 5/1-525.
- [15] R. Buxton, 1998, “Protection from Voltage Dips with the Dynamic Voltage Restorer,” Proceeding of the IEE Half Day Colloquium on Dynamic Voltage Restorers – Replacing Those Missing Cycles, IEEE Xplore Glasgow, UK, pp. 3/1-3/6.
- [16] P. T. Cheng, C. L. Ni, J. M. Chen, ”Design of a state feedback controller for series voltage sag compensators,” Power Conversion Conference, pp. 398-403, April 2007.
- [17] L. Yun Wei, F. Blaabjerg, D. M. Vilathgamuwa, and A. P. C. L. Poh Chiang Loh, "Design and Comparison of High Performance Stationary-Frame Controllers for DVR Implementation," Power Electronics, IEEETransactions on, vol. 22, pp. 602-612, 2007.
- [18] M. H. Rashid, Power Electronics-Circuits, Devices and Applications, 3rd ed. India: Prentice-Hall of India, Aug. 2006.