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A Closed Loop for Soft Switched PWM ZVS Full Bridge DC - DC Converter

S.P.Narasimha Prasad.
Dept of EEE, SVPCET.
AP-517583, India.

K.Vijaya Bhaskar.
Dept of EEE, SVPCET.
AP-517583, India.

Abstract: -

This paper propose soft switched PWM ZVS full bridge DC to DC converter. The control of the proposed converter can be implemented either with the phase-shift or pulse width modulated technique. This converter is effectively reduces the switching losses, stress and elector magnetic interference. The input DC voltage 48V is step down to 12V level. The simulation results and analytical results are compared. The PWM ZVS FB converter proto type will operate at 20 KHz at a 48V DC. The open loop and closed loop of the circuit is simulated by using MAT LAB software.

Index Terms-DC-DC converter, Full Bridge (FB), Zero voltage switching (ZVS)

I. INTRODUCTION

The continuing success of square-wave PWM topology in switching converter can be attributed to its ease of operation. The harmonics can easily be eliminated by power filter and it has a capability in allowing continuous and linear control of the frequency and fundamental component of the output voltage. But with the demands for higher power densities, the switching frequencies are approaching 1 MHz range. At these frequencies, square wave converters' switching losses become very high leading to excessive heat dissipation. Even if the increased switching frequency does not cause unacceptable switching losses, the oscillations caused by converter parasitic elements may cause high current and voltage stresses, which are almost unpredictable, depending on circuit layout. Suitable snubber circuits must therefore be adopted, which affect power density and converter reliability. The zero-voltage transition approach, as well as the active-clamp snubber approach, leads to zero-voltage switching of the transistors and zero-current switching of the diodes. These approaches have been successful in substantially improving the efficiencies of transformer-isolated converters.

The Zero-voltage switching (ZVS) phase shift modulated full bridge (PSM-FB) DC/DC converter with MOSFET switches has been proposed in [1],[2]. Low component count and zero full load switching losses enable this topology to achieve low cost, high power density, high efficiency, and low EMI, so for medium to high power DC/DC applications it is a good choice.

The phase-shifted PWM full bridge (FB) converter incorporates the leakage inductance of the transformer to achieve zero-voltage switching, but only achieves it near the full load condition.

Several new techniques for high frequency DC-DC conversion are there to reduce component stresses and switching losses while achieving high power density and improved performance. Among them, the full-bridge (FB) zero-voltage-switched (ZVS) converter is one of the most attractive techniques which are shown in Fig. 1. It is the most widely used soft-switched circuit in high-power applications, [1]–[3]. This constant-frequency converter employs phase-shift (PS) control and features ZVS of the primary switches with relatively small circulating energy. However, full ZVS operation can only be achieved with a limited load and input-voltage range, unless a relatively large inductance is provided in series with the primary winding of the transformer either by an increased leakage inductance of the transformer and/or by an additional external inductor. This increased inductance has a detrimental effect on the performance of the converter since it causes an increased loss of the duty cycle on the secondary side, as well as severe voltage ringing across the secondary-side output rectifiers due to the resonance between the inductance and the junction capacitance of the rectifier. The secondary-side ringing can be suppressed by an active snubber described in [2]. For implementations with an external primary inductor, the ringing can also be effectively controlled by employing primary-side clamp diodes D and D_1 shown in Fig. 1, as proposed in [2]. While the snubber approaches in [1] and [2] offer practical and efficient solutions to the secondary-side ringing problem, they do not offer any improvement of the secondary side duty-cycle loss.

Several techniques have been proposed to extend the ZVS range of FB ZVS converters without the loss of duty cycle and secondary-side ringing [4]–[7]. Generally, these circuits utilize energy stored in the inductive components of an auxiliary circuit to achieve ZVS for all primary switches in an extended load and input voltage

range. Ideally, the auxiliary circuit needs to provide very little energy, if any, at full load because the full-load current stores enough energy in the converter's inductive components to achieve complete ZVS for all switches. As the load current decreases, the energy provided by the auxiliary circuit must increase to maintain ZVS, with the maximum energy required at no load. The energy stored for ZVS is independent of load as described in [4] and [5]. Adaptive energy storage in the auxiliary circuit has been introduced in [6] and [7]. However, these converters have to use large inductors so, high circulating energy that is needed1 to achieve no-load ZVS and that is due to a relatively large inductor employed to assist ZVS.

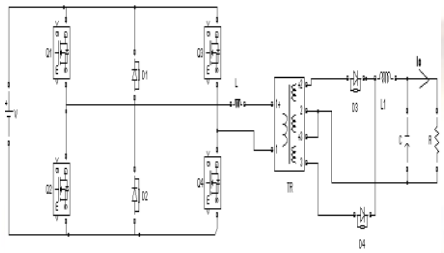

Fig.1 PWM Full Bridge Converter

In this paper, a FB ZVS converter with adaptive energy storage that offers ZVS of the primary switches over a wide load range with greatly reduced no-load circulating energy and with significantly reduced secondary-side duty cycle loss is introduced with PWM control. ZVS full bridge DC to DC converter with ZVS over the entire range is given by[8].High power density multi-kilowatt DC to DC converter with galvanic isolation is given by [9]. The literature [1] to [9] does not deal with the modeling and simulation of closed loop controlled PWM ZVS full bridge converter. This works aims to develop circuit model for ZVS full bridge converter.

II. PWM ZVS FB CONVERTER WITH AUXILIARY TRANSFORMER.

Fig. 2 shows the FB ZVS converter circuit diagram that provides ZVS for the bridge switches over a wide range of load current. It employs low-power auxiliary transformer TRA to extend the ZVS range. The primary of auxiliary transformer TRA is connected to the center tap of power transformer TR and the ground through blocking capacitor C_1, where as its secondary is connected in series with the primary winding of power transformer TR and inductor L_p .Auxiliary transformer TRA is only used to adaptively store a relatively small amount of energy into primary inductor that is required for ZVS. Finally, two diodes are connected from the node connecting the primary of the power transformer and the secondary of the auxiliary transformer to the positive and negative (ground) rails of the bridge to provide a path for the current through primary inductor, L_p which is used to store ZVS energy. When the load voltage is regulated, as the load current and/or input voltage decreases, the duty cycle of each PWM switch, i.e., switches Q_3 and Q_4 decreases so that the volt-second product on the windings of power transformer TR also decreases. At the same time, the volt-second product on the windings of auxiliary transformer TRA increases, which proportionally increases the energy stored in the primary inductor. Due to the adaptive nature of the energy available for ZVS stored in the primary inductor, which increases as the load current and/or input voltage decreases, the proposed circuit can achieve ZVS in a very wide range of load current, including no load, with minimal circulating energy.

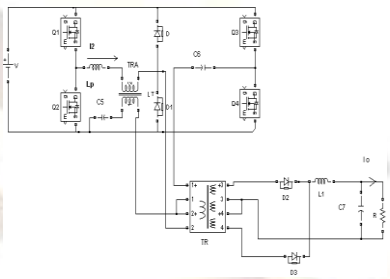

Fig.2 FB ZVS converter with auxiliary transformer

In the modified circuit, since the ZVS energy stored in the primary inductor is dependent on its inductance value and the volt-second product of the secondary of auxiliary transformer TRA, the size of the primary inductor can be minimized by properly selecting the turns ratio of auxiliary transformer TRA. As a result, the size of the primary inductor is very much reduced compared to that of the conventional PS FB converter shown in Fig.1. In addition, since the auxiliary transformer does not need to store energy, its size can be small. Finally, because the energy used to create the ZVS condition at light loads is not stored in the leakage inductances of transformer TR, the transformer's leakage inductances can also be minimized. As a result of the reduced total primary inductance, i.e., the inductance of the primary inductor used for ZVS energy storage and the leakage inductance of the power transformer, the proposed converter exhibits a relatively small duty-cycle loss, which minimizes both the conduction loss of the primary switches and the voltage stress on the components on the secondary side of the transformer, which improves the conversion efficiency. Moreover, because of the reduced total primary inductance, the secondary- side parasitic ringing is also reduced and is effectively controlled by primary side diodes D and D_1.

III. OPERATIONAL PRINCIPLE

The circuit diagram of the modified converter is shown in Fig.2.The primary side consists of four switches, two diodes, one inductor, and one capacitor. It employs low power auxiliary transformer TRA to extend the ZVS range. At light loads energy used to create ZVS is not stored in the leakage inductance of the transformer TR .So; the transformer's leakage inductance can be minimized. Energy stored in primary inductor depends on volt-second product of the secondary of auxiliary transformer TRA and inductance value. So by selecting proper turn ratio of auxiliary transformer TRA, the size of the primary inductor can be minimized. Auxiliary transformer is not used to store energy. So, its size can be small. Several assumptions are made as follows.

1) Capacitance of capacitor C_5 is large enough so that the capacitor can be modeled as a constant voltage source.
2) The inductance of output filter L_1 is large enough so that during a switching cycle the output filter can be modeled as a constant current source.
3) The leakage inductance of auxiliary transformer TRA and the magnetizing inductances of both transformers are neglected.
4) The resistance of each conducting switch is zero; where as the resistance of each non-conducting switch is infinite.
5) Current through primary side of auxiliary transformer TRA is zero.

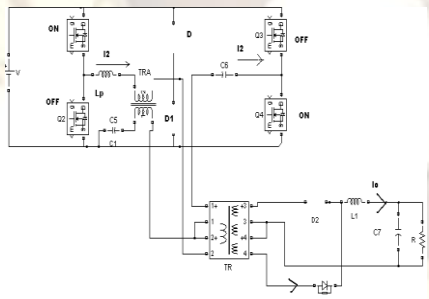

Fig 3(a).The circuit diagram at (t_0 to t_1)

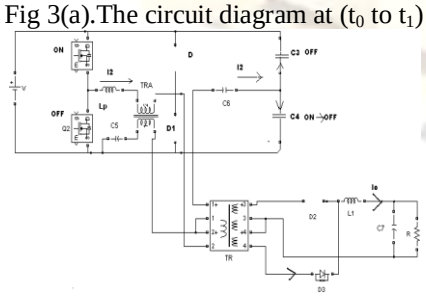

Fig 3(b).The circuit diagram at (t1 to t2)

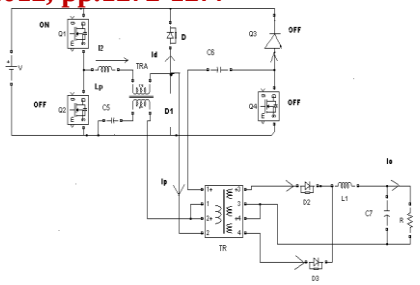

Fig 3(c).The circuit diagram at (t_2 to t_3)

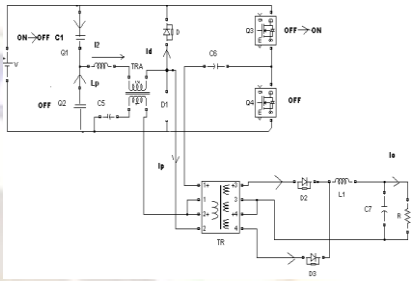

Fig 3(d).The circuit diagram at (t_3 to t_4)

As shown in Fig.3(a), at $t=t_0$, load current flows through rectifier D_3 and the lower secondary of power transformer TR. when diagonal switches Q_1 and Q_2 are conducting. Since during this topological stage diodes D and D_1 are reverse biased, the reflected primary current is flowing through closed switch Q_1, primary inductor L_p winding N_2 of auxiliary transformer TRA, primary winding N_p of transformer TR, and closed switch Q_4. Since the impendence of the primary inductor L_p and winding N_2 of auxiliary transformer TRA are very small compare to primary referred filter inductor L_o .Let V_o be the primary referred output DC voltage.

Slope of the primary current is given by $(V_{DC} - V_o)/L_o$. Centre tap of primary voltage is given by $V_P/2 = V/2$ because impendence of primary inductor L_p and winding N_2 of TRA are small. At $t=t_1$ as shown in Fig. 3(b), switch Q_4 is turned off, primary current starts charging output capacitance C_4 of switch Q_4 and discharges output capacitance C_3 of switch Q_3. The total required energy to charge C_4 and discharge C_3 is provided not only from the stored energy of L_p, but also from the stored energy of the output filter inductor. Since the stored energy in the output filter inductor is significantly larger than the required energy to charge C_4 and discharge C_3, these capacitors are assumed to be charged and discharged linearly. Voltage across switch Q_4 increases towards V and voltage across switch Q_3 decreases towards zero. Primary winding voltage of auxiliary transformer increases from zero to V/2 and secondary winding of auxiliary transformer increases from zero to $V/2^* n_i$ where n_i is the auxiliary transformer turn ratio. Diode D starts conducting because of increasing secondary voltage of auxiliary

transformer. After voltage across Q_3 reaches zero diode across Q_3 starts conducting at $t=t_2$ as shown in Fig. 4(c).

When the voltage across switch Q_3 becomes zero, voltage across the power transformer also becomes zero since the primary of the transformer is shorted by the simultaneous conduction of the body diode of Q_3 and diode D. As a result, the secondary windings are also shorted so that rectifiers D_2 and D_3 can conduct the load current simultaneously. However, because of the leakage inductance of transformer TR, load current Io is still carried by the lower secondary through rectifier D_3 since no voltage is available to commutate the current from the lower secondary and D_3 to the upper secondary and D_2 if ideal components are assumed. With real components this commutation voltage exists, but is too small to commutate a significant amount of current from the lower to the upper secondary so that even with real components the majority of the current is still found in the lower secondary and its corresponding rectifier D_3. So, during this stage when switches Q_1 and Q_3 are conducting, primary current stays nearly unchanged.

During this stage, diode D is conducting and voltage V_2 is applied directly across primary inductor L_p, Which increases current I_2 until Q_1 is turned off at $t=t_3$ as shown in Fig 4(d).Current $I_2(t)$ in the interval of t_2 to t_3 can be given as

$$I_2(t) = I_p + I_d(t) = I_o/n + \{(V/2)*n_i*Lp(t-t_2)\} \quad (1)$$

Where $I_d(t)$ is the current across diode D.
n=turn ratio of power transformer.

During this stage, the voltage across switch Q_3 is kept zero due to D. So switch Q_3 is turned on with ZVS. After Q_1 is turned off, current I_2 begins charging output capacitance C_1 of switch Q_1 and discharging capacitance C_2 of switch Q_2.The total energy required to charge C_1 and discharge C_2 is supplied from the stored energy in the primary inductor L_p. To achieve ZVS energy stored in the primary inductor (ELP) must be higher than total energy required to charge C_1 and discharge C_2.

$$E_{LP} \geq CV^2 \quad (2)$$

Where $C_1=C_2=C$
Using equation (1)

$$E_{LP} = \left(\frac{1}{2} L_P \frac{Io}{n} + \frac{v(1-d)^2}{2} \right) \quad (3)$$

Where, f_s is the switching frequency.
From equation (2) and (3)

$$\left(\frac{1}{2} L_P \frac{Io}{n} + \frac{v(1-d)^2}{4niL_Pfs} \right) \geq 2CV^2 \quad (4)$$

Where, D is the duty cycle of the converter.

Then primary current continue to flow through anti-parallel diode of switch Q_2 so that Q_2 can be turned on with ZVS. In this stage Voltage V_{s1} across switch Q_1, which is in opposition to voltage V_2, is increasing and current I_d starts decreasing. When I_d becomes zero Diode D stops conducting so that primary current starts decreasing. Load current I_o also begins to commutate from the lower secondary and D_3 to upper secondary and D_2. When the commutation of the load current from the lower to upper secondary is completed, the primary current commutation from the positive to negative direction is also finished.

The circuit stays with diagonal switches Q_2 and Q_3 turned on until the switch Q_3 is turned off. Second half of the switching period is exactly the same as the first half of the switching period.

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IV. SIMULATION RESULTS.

The ZVS DC to DC converter is simulated using Matlab Simulink are presented here.

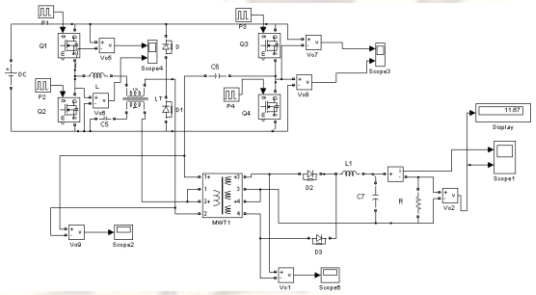

Fig.4 Simulink Model of ZVS DC to DC converter

Simulink model of DC to DC converter is shown in Fig 4. Driving pulses are shown in Fig. 5.DC input voltage is shown in Fig 6.Output voltage across Q_1 & Q_2 is shown in Fig 7.Voltage across Q_3 & Q_4 are shown in Fig 8. .Secondary voltage is shown in Fig 9. DC output current and voltage are shown in Fig. 10. DC output voltage is 12V and the current is 1A. It can be seen that the DC output is free from ripple.

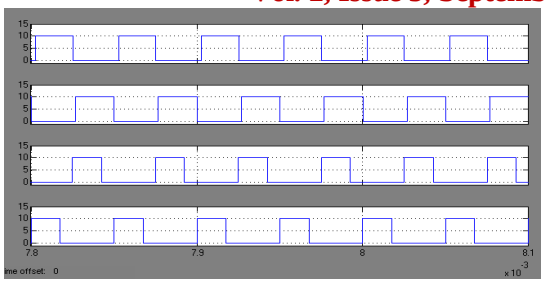

Fig.5 Driving Pulses

For constant-frequency, variable duty cycle control of the proposed converter, switches Q_1 and Q_2 always operate with approximately 50% duty cycle, whereas switches Q_3 and Q_4 have a duty cycle in the range from 0% to 50% as shown in Fig 5.

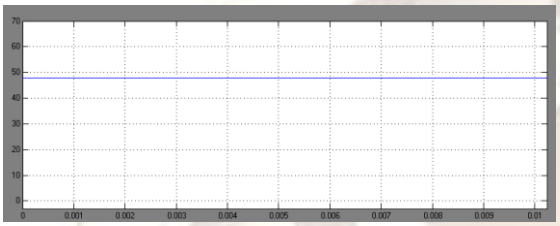

Fig.6 DC Input Voltage

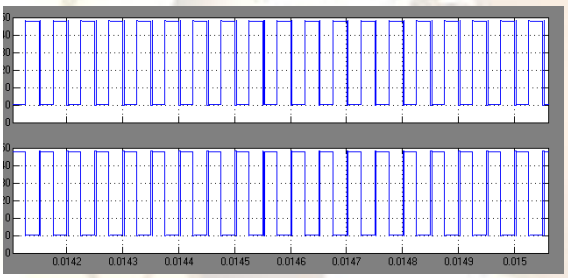

Fig.7 Output Voltage across Q_1 and Q_2

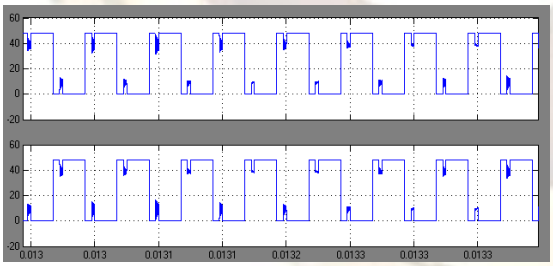

Fig.8 Output voltage across Q_3 and Q_4

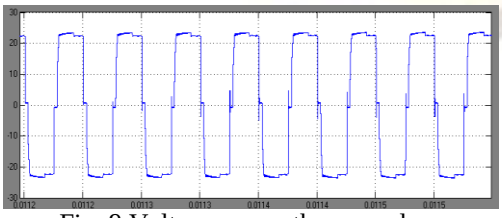

Fig. 9 Voltage across the secondary

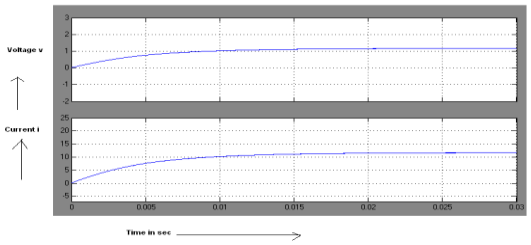

Fig.10 DC output current and voltage

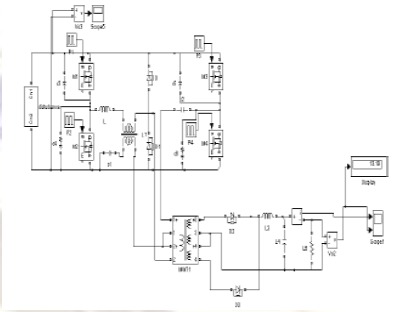

Fig.11 Open loop system

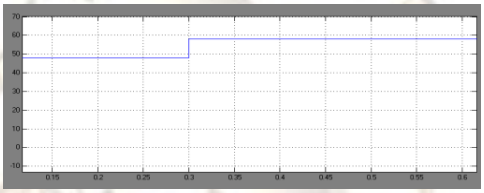

Fig.12 Dc input voltage with disturbance

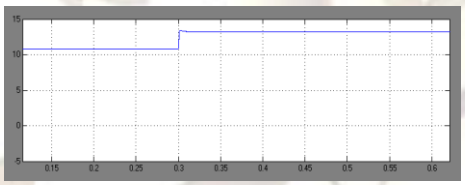

Fig.13DC output voltage with disturbance

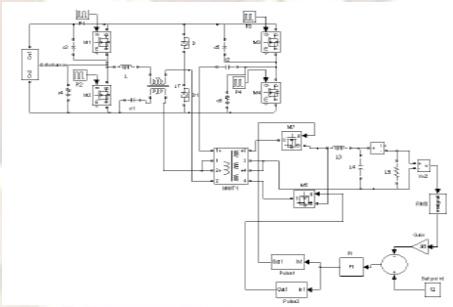

Fig.14 Closed loop system

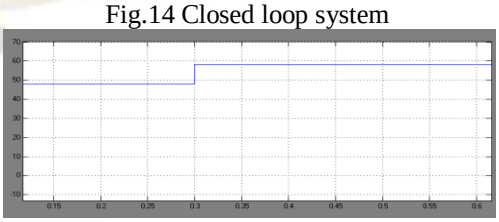

Fig.15 Dc input voltage with disturbance

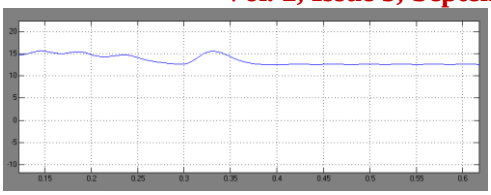

Fig.16 Dc output voltage with disturbance

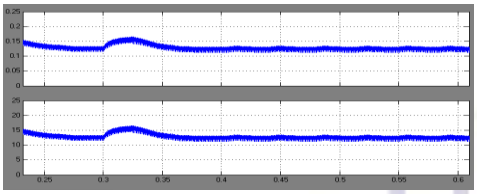

Fig.17 Output current and voltage with disturbance

V. COMPARISONS OF OPEN LOOP SYSTEM WITH CLOSED.

Simulink model of open loop system is shown in Fig.11 where input is given with disturbance. Fig.12 shows the DC input voltage with disturbance. Fig.13 shows DC output voltage with disturbance. When input voltage changes due to disturbance in Fig.12, output voltage also changes.

Simulink model of closed loop system is shown in Fig.14. It consists of a feedback circuit. The R.M.S value of instantaneous voltage signal is taken from the output. To reduce the output, a gain of 0.95 is taken and given to the sub tractor. Other input to the sub tractor is the set voltage of 12V. Output of sub tractor is the error signal which is given to the PI controller. The output of PI controller is given to the two comparators whose outputs are PWM waves. They are fed to the gates of MOSFETs 5&7as control signals. The Fig.15 shows DC input voltage with disturbance and Fig.16 shows DC output voltage with disturbance where output voltage changes with input. But the output reduces to a value of 12V. Output current and voltage with disturbance are shown in Fig.17.Thus the closed loop system is able to maintain constant voltage.

VI. CONCLUSION.

ZVS DC to DC converter is modeled using the blocks of Simulink. Soft switched ZVS PWM DC to DC Converter is analyzed and simulated and results are presented. Conversion from 48V DC to 12V DC is done using soft switched PWM converter. Switching losses and stresses are reduced using zero voltage switching. The simulation results are similar to the predicted results. This converter can be used for battery charging and Electrolysis. The scope of this work is the modeling and simulation of ZVS DC to DC converter. Hardware implementation is yet to be done. The simulation results are in line with the predictions.

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