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Design of Two-Stage CMOS Op-Amp and Analyze the Effect of Scaling

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Abstract:-

A method described in this paper is to design a Two Stage CMOS operational amplifier and analyze the effect of various aspect ratios on the characteristics of this Op-Amp, which operates at 5V power supply using tsmc 0.35µm CMOS technology. In this paper trade-off curves are computed between all characteristics such as Gain, PM, GBW, ICMRR, CMRR, Slew Rate etc. The OPAMP designed is a two-stage CMOS OPAMP. The OPAMP is designed to exhibit a unity gain frequency of 14MHz and exhibits a gain of 77.25dB with a 85.85^0 phase margin. Design has been carried out in Mentor graphics tools. Simulation results are verified using Model Sim Eldo and Design Architect IC.

The task of CMOS operational amplifiers (Op-Amps) design optimization is investigated in this work. This Paper focused on the optimization of various aspect ratios, which gave the result of different parameter. When this task is analyzed as a search problem, it can be translated into a multi-objective optimization application in which various Op-Amps' specifications have to be taken into account, i.e., Gain, GBW (gain-bandwidth product), phase margin and others. The results are compared with respect to standard characteristics of the op-amp with the help of graph and table. Simulation results agree with theoretical predictions. Simulations confirm that the settling time can be further improved by increasing the value of GBW, the settling time is achieved 19ns, gain is 77.25dB and a value of phase margin is 73.3^0. It has been demonstrated that when W/L increases the parameters GBW increases and settling time reduces.

Keywords

CMOS Analog Circuit, 2 stage CM OS Operational amplifier, Stability, GBW, Device Design, Scale Length, Scaling, Differential Amp.

I. Introduction

Over the last few years, the electronics industry has exploded. The largest segment of total worldwide sales is dominated by MOS market. CMOS technology continues to mature with minimum feature sizes now. Designing high performance analog integrated circuits is becoming increasingly exigent with the relentless trend toward reduced supply voltages and transistor channel length. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance. The feature size of individual transistor is shrinking from deep sum-micrometer (DSM) to even nanometer region. As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip.

Operational Amplifier is the most common building blocks of most of the electronics system may not need introduction**.** The design of OPAMPs continues to pose a challenge as the supply voltage and transistor channel lengths scale down with each generation of CMOS technologies. At different aspect ratio, there is a tradeoff among speed, power, gain and other performance parameters. The realization of a CMOS OPAMP that combines a considerable dc gain with high unity gain frequency has been a difficult problem. There have been several circuit approaches to evade this problem.

The aim of the design methodology in this paper is to propose straightforward yet accurate equations for the design of high-gain 2 staged CMOS op-amp. To do this, a simple analysis with some meaningful parameters (phase margin, gain-bandwidth, *etc*.) is performed. The method handles a very wide variety of specifications and constraints. In this paper, we formulate the CMOS op-amp design problem and their aspect ratios. The method we present can be applied to a wide variety of amplifier architectures, but in this paper we apply the method to a specific two stage CMOS op-amp. The variation in the performance of the op-amp with variations in the width and length of the CMOS and the effect of scaling the gate oxide thickness is discussed.

The simulation results have been obtained by tsmc 0.35 micron CMOS technology. Design has been carried out in Mentor Graphics tool. Simulation results are verified using Model Sim Eldo and Design Architect IC. Scaling effects are analyzed through experimental data and computer simulations. This search technique can be successfully applied to a class of optimization problems. After the simulation, most of the transistors' size still needed to be modified in order to optimize the performance. High gain in operational amplifiers is not the only desired figure of merit for all kind of signal processing applications. Simultaneously optimizing all parameters has become mandatory now a day in operational amplifier design.

In this case, the slew rate will increase for an increase in current. However, if the widths of the devices are increased with the bias voltages held constant. Thus, we can conclude that the selection of device sizes depends on trade-offs between stability (phase margin) and slew-rate.
As such, for the fastest slew-rate, the smallest channel length (350 nm) will be used, and at this length, the device is in the short channel regime and will require short channel topologies.

Outline of paper

This paper composed this work. Section II discusses the 2 stage amplifier and design optimization. Section III reviews the 2 stage CMOS Op-amp schematic design. Its specifications are briefly clarified, also gives the formula or calculation for designing of 2 stage CMOS Op-amp. Section IV presents the simulation results of the proposed op-amp, tables and graphs for optimization technique. Section V gives the scaling and finally section VI concludes this work.

II. Block diagram of two stage CMOS op-amp

Operational Amplifiers are the backbone for many analog circuit designs. Op-Amps are one of the basic and important circuits which have a wide application in several analog circuit such as switched capacitor filters, algorithmic, pipelined and sigma delta A/D converter, sample and hold amplifier etc. The speed and accuracy of these circuits depends on the bandwidth and DC gain of the Op-amp. Larger the bandwidth and gain, higher the speed and accuracy of the amplifier Op-amp are a critical element in analog sampled data circuit, such as SC filters, modulators.
The general block diagram of an op-amp with an output buffer is shown below

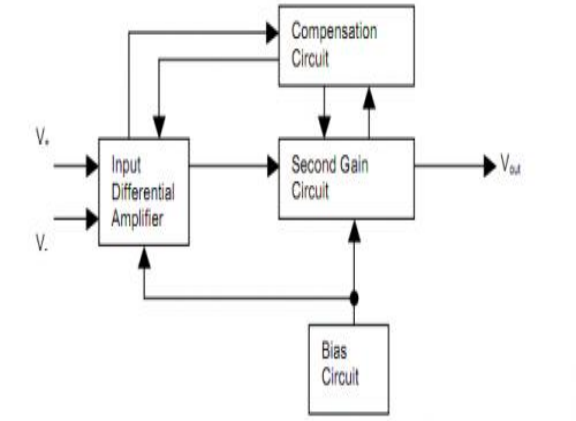

Figure 1. Block diagram of Op-Amp

The first block is a differential amplifier. It has two inputs which are the inverting and non-inverting voltage. It provides at the output a differential voltage or a differential current that, essentially, depends on the differential input only. The next block is a differential to single-ended converter. It is used to transform the differential signal generated by the first block into a single ended version. Some architecture doesn't require the differential to single ended function; therefore the block can be excluded. In most cases the gain provided by the input stages is not sufficient and additional amplification is required. This is provided by intermediate stage, which is another differential amplifier, driven by the output of the first stage. As this stage uses differential input unbalanced output differential amplifier, so it provide required extra gain. The bias circuit is provided to establish the proper operating point for each transistor in its saturation region. Finally, we have the output buffer stage. It provides the low output impedance and larger output current needed to drive the load of op-amp or improves the slew rate of the op –amp. Even the output stage can be dropped: many integrated applications do not need low output impedance; moreover, the slew rate permitted by the gain stage can be sufficient for the application. If the op-amp is intended to drive a small purely capacitive load, which is the case in many switched capacitor or data conversion applications, the output buffer is not used. When the output stage is not used the circuit, it is an operational transconductance amplifier, *OTA*. The purpose of the compensation circuit is lower the gain at high frequencies and to maintain stability when negative feedback is applied to the op amp.

A. Circuit Operation

The final circuit designed to meet the required specifications is shown in Figure 2. The topology of this circuit is that of a standard CMOS op-amp. It comprised of three subsections of

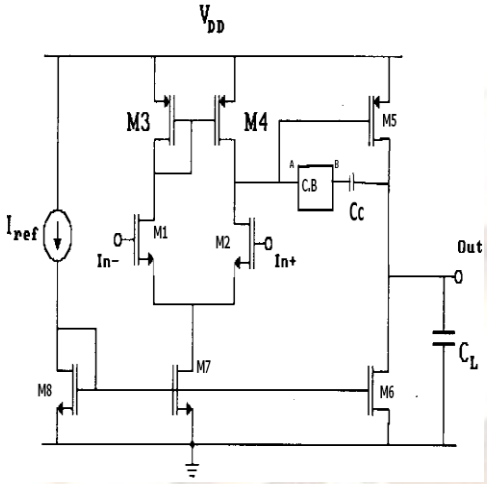

Figure2. The topology chosen for this Op-Amp design.

circuit, namely differential gain stage, second gain stage and bias strings. It was found that this topology was able to successfully meet all of the design specifications.

B. Differential Gain Stage

Transistors M1, M2, M3, and M4 form the first stage of the op amp the differential amplifier with differential to single ended transformation. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors which form the basic input stage of the amplifier. The gate of M1 is the inverting input and the gate of M2 is the non-inverting input. A differential input signal applied across the two input terminals will be amplified according to the gain of the differential stage. The gain of the stage is simply the transconductance of M2 times the total output resistance seen at the drain of M2. The two main resistances that contribute to the output resistance are that of the input transistors themselves and also the output resistance of the active load transistors, M3 and M4. The current mirror active load used in this circuit has three distinct advantages. First, the use of active load devices creates a large output resistance in a relatively small amount of die area. The current mirror topology performs the differential to single-ended conversion of the input signal, and finally, the load also helps with common mode rejection ratio. In this stage, the conversion from differential to single ended is achieved by using a current mirror (M3 and M4). The current from M1 is mirrored by M3 and M4 and subtracted from the current from M2. The differential current from M1 and M2 multiplied by the output resistance of the first stage gives the single-ended output voltage, which constitutes the input of the second gain stage.

C. Second Gain Stage

The second stage is a current sink load inverter. The purpose of the second gain stage, as the name implies, is to provide additional gain in the amplifier. Consisting of transistors M5 and M6, this stage takes the output from the drain of M2 and amplifies it through M5 which is in the standard common source configuration. Again, similar to the differential gain stage, this stage employs an active device, M6, to serve as the load resistance for M5. The gain of this stage is the transconductance of M5 times the effective load resistance comprised of the output resistances of M5 and M6. M6 is the driver while M7 acts as the load.

D. Bias String

The biasing of the operational amplifier is achieved with only four transistors. Transistors M8 and M9 form a simple current mirror bias string that supplies a voltage between the gate and source of M7 and M6. Transistors M6 and M7 sink a certain amount of current based on their gate to source voltage which is controlled by the bias string. M8 and M9 are diode connected to ensure they operate in the saturation region. Proper biasing of the other transistors in the circuit (M1-M5) is controlled by the node voltages present in the circuit itself. Most importantly, M5 is biased by the gate to source voltage (VGS) set up by the VGS of the current mirror load as are the transistors M1 and M2.

III. Design of the op-amp

The first aspect considered in the design was the specifications to be met. They appear in Table 1

Table1. Custom Design Specifications of the amplifier

Specification Names	Values
Supply VDD	5V
Gain	≥ 70dB
Gain Bandwidth	10MHz
Settling Time	1u Sec
Slew Rate	10V/uSec
Input common Mode Range	1.5 – 2.8V
Common mode rejection ratio	≥60dB
Output Swing	1 – 2.8V
Offset	≤10m

A. Design Methodology of Op-amp

3.1.1 Determine the necessary open-loop gain (Ao)

$g_{m1} = g_{m2} = g_{mI}$, $g_{m6} = g_{mII}$, $g_{ds2} + g_{ds4} = G_I$, and $g_{ds6} + g_{ds7} = G_{II}$

$$Id = \frac{\mu_{n,p}\, Cox \left(\frac{W}{L}\right) Veff\, 2}{2} \quad (1)$$

$$g_m = \sqrt{2\mu_{n,p} Cox \frac{W}{L} Id} \quad (2)$$

$$g_m = 2\frac{Id}{V_{eff}} \quad (3)$$

Slew rate $SR = \frac{I_5}{C_C}$ (4)

First stage gain $A_{v1} = \frac{-gm_1}{gds_2 + gds_4} = \frac{-2gm_1}{I_5\,(\lambda_2 + \lambda_4)}$ (5)

Second stage gain $A_{v2} = \frac{-gm_6}{gds_6 + gds_7} =$

$$\frac{-gm_6}{I_6\,(\lambda_6 + \lambda_7)} \quad (6)$$

Gain Bandwidth $GB = \frac{gm_1}{C_C}$ (7)

Output pole $p_{2=} \frac{-gm_6}{C_L}$ (8)

RHP zero $Z_{1=} \frac{gm_6}{C_C}$ (9)

Positive CMR $V_{in}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} -$
$|V_{TO3}|(\max) + V_{T1}(\min)$ (10)

Negative CMR $V_{in}(\min) = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} +$
$V_{T1}(\max) + V_{DS5}(\text{sat})$ (11)

Saturation voltage $V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}}$ (12)

It is assumed that all transistors are in saturation for the above relationships.

The design in this project is a two-stage op amp with an n-channel input pair. The op amp uses a dual-polarity power supply (Vdd and Vss) so the ac signals can swing above and below ground and also be centered at ground. The hand calculation results provided the estimated parameters (such as transistor width and length, capacitance, etc.) to make the circuit schematic (shown in figure 3) in Design Architect IC and for the circuit analysis in Model Sim Eldo of Mentor Graphic Tool.Schematic used in this design is

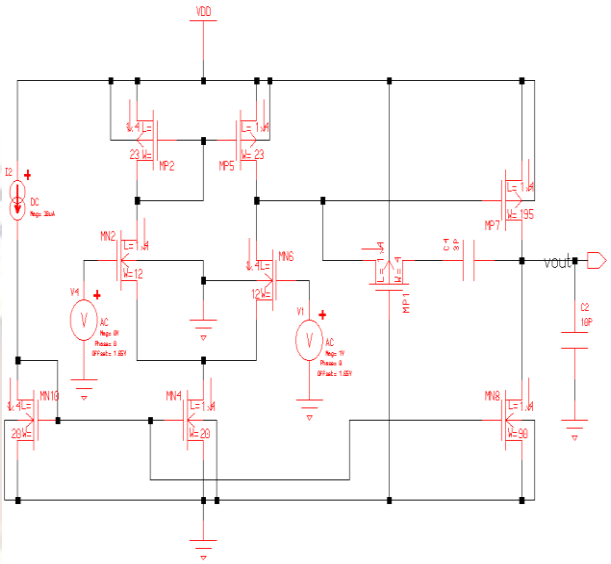

Figure 3. Schematic design of 2 stage CMOS Op-Amp

Open Loop Gain: It is the ratio between output voltage and differential input voltage. Because the output signal is much larger than the input signal, so it is commonly called as large signal voltage gain.

Slew Rate: The maximum rate of change of output voltage per unit time. (dVo/dt) The slope of the output signal is the slew rate.

Rise Time: the time required by the output to go from 10% to 90% of its final value is called the rise time.

CMRR: Common Mode Rejection ratio is the ratio between differential gain and common mode gain.

IV. Simulation results

To analyze the behavior of variations in aspect ratios, first discuss the results of basic design of two stage CMOS Op-amp

A. AC Analysis

In AC- Analysis we determine Phase margin, Gain and GB of the OP-Amp.

- Start frequency = 1Hz
- Stop frequency = 10 MHz

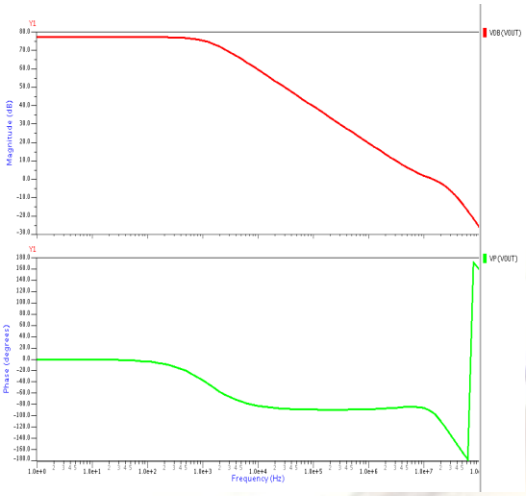

Figure 4. Output of AC Analysis

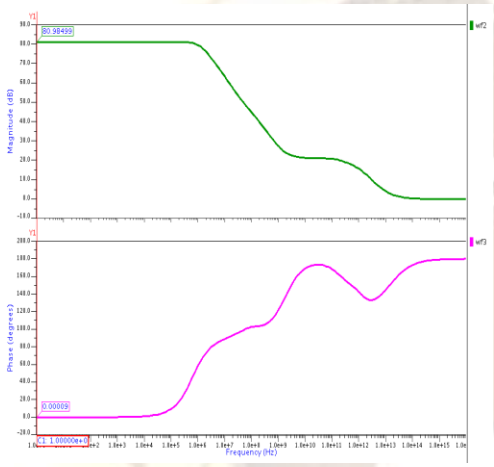

Figure 5. Result of CMRR

Output: The output results of AC analysis is as follows

Gain = 77.249 dB ω_{-3db} = 1.3 KHz
Phase margin = 85.85^0 ω_{UGB} = 14.1MHz
CMRR = 80.985 dB

B. Transient Analysis

The non inverting terminal is connected to a pulse with a rise and fall time equal to 1n sec (0.1us) and a pulse width of 384.61us. The value of pulse period is 769.23us. This analysis helps to determine the slew rate of the op-amp.

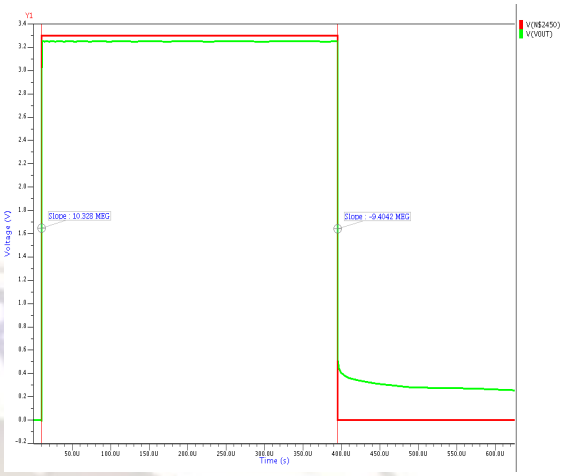

Figure 6. Result of Slew Rate

The slew rate achieved in this design is 10.32 V/µs.

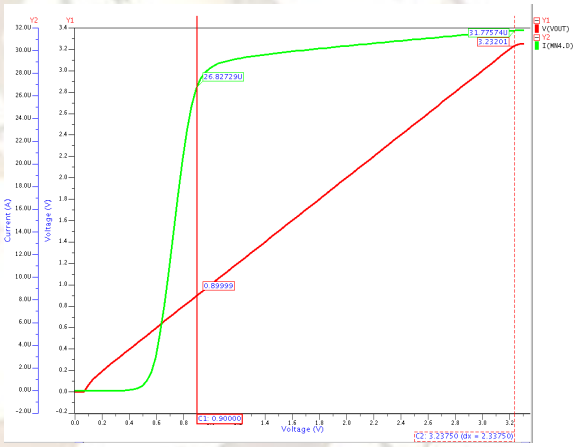

Figure 7. Result of ICMR

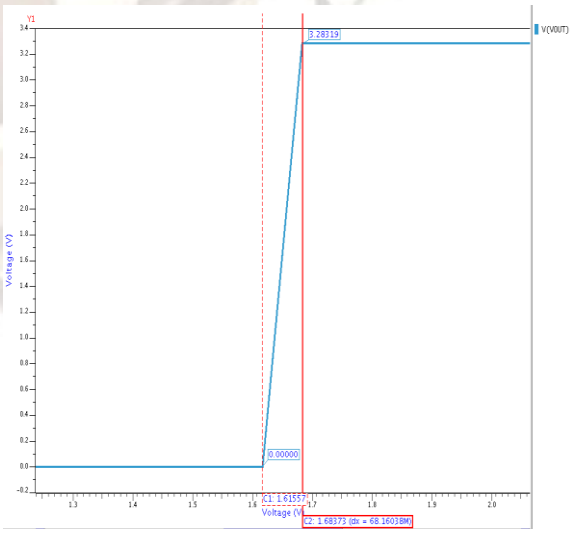

Figure 8. Output Swing

Positive Slew Rate = 10.328V/us
Settling Time = 0.4 us
Negative Slew Rate = 9.40V/us
ICMR = 0.9 – 3.237 V
Output Swing = 0.0 - 3.28V

V. Scaling

Proportional adjustment of the dimensions of an electronic device while maintaining the electrical properties of the device, results in a device either larger or smaller than the un-scaled device is called scaling. Scaling allows people to build more complex machines that run faster too and it does let you design more modules.
Impact of scaling is characterized in terms of several indicators:

- Minimum feature size
- Number of gates on one chip
- Power dissipation
- Maximum operational frequency
- Production cost

Implications of Scaling

1. Improved Performance
2. Improved Cost
3. Interconnect Woes
4. Power Woes
5. Productivity Challenges
6. Physical Limits

Reference Circuit L = 1.4 um

Table 2. Values of W of reference circuit

Name	Values
W1, W2	12
W3, W4	23
W5, W8	20
W6	195
W7	90

Consider all W/L of reference circuit as (W/L)1 and f is a multiplication factor.
(W/L)n = f * (W/L)1

A. By Reducing L:

Table 3. Values of various parameters after reducing value of L

Results	**f =1**	**f = 2, L=L1/2**	**f = 3, L=L1/3**	**f= 4, L = L1/4**
Gain (dB)	77.24	69.36	58.9	47.53
PM	53.46^0	59.96^0	65.57^0	73.3^0
ω_{-3dB} (KHz)	1.3	4.12	15.2	63.275
ω_{UGB} (MHz)	8.6	11.35	12.86	14.853
CMRR (dB)	80.985	78	67.29	53.49
ICMR (V)	0.9 – 3.23	0.812 – 3.245	0.75 – 3.224	0.93 – 3.13
Slew Rate (V/µs)	10.347, -9.527	10.931, -9.18	13.742, -9	26.078, -10.25
Settling Time (µs)	0.4	0.347	0.304	0.0192
Output Swing (V)	0.0 – 3.28	0.0 – 3.287	0.0 – 3.282	0.0 – 3.253

B. By increasing W:

Table 4. Values of various parameters after increasing value of W

Results	**f =1**	**f = 2, W=2W1**	**f = 3, W=3W1**	**f= 4,W =4W1**
Gain (dB)	77.24	78.165	78.38	78.417
PM	53.46^0	47.97^0	43.36^0	40.05^0
ω_{-3dB} (KHz)	1.3	1.47	1.58	1.654
ω_{UGB} (MHz)	8.6	10.37	11.05	11.258
CMRR(dB)	80.985	85.56	87.993	89.56
ICMR(V)	0.9 –3.23	0.8 – 3.258	0.76 – 3.266	0.73 –3.27
Slew Rate (V/µs)	10.347, -9.527	10.469, -8.68	10.494, -8.873	10.49, -8.82
Settling Time	0.4 µs	0.383 µs	0.4 µs	0.36 µs
Output Swing (V)	0.0 –3.28	0.0 – 3.297	0.0 – 3.285	0.0 -3.295

Graph: Graph shows the variations in different parameter of Op-Amp with various aspect ratios.

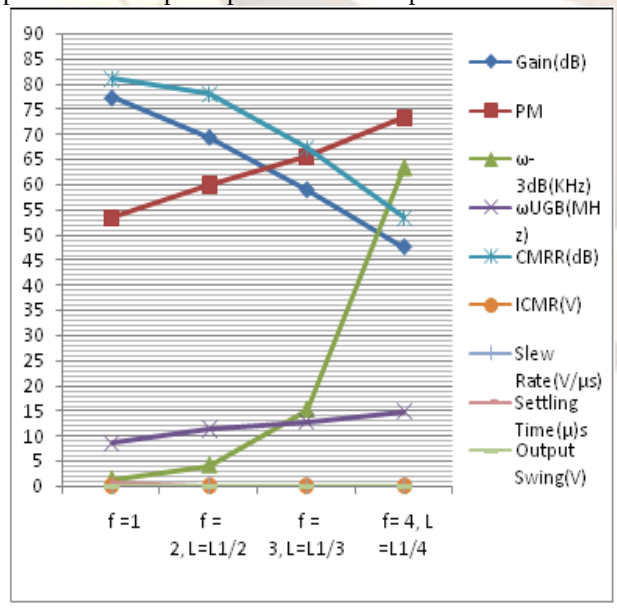

Figure 9.Variations in Parameters with reducing L

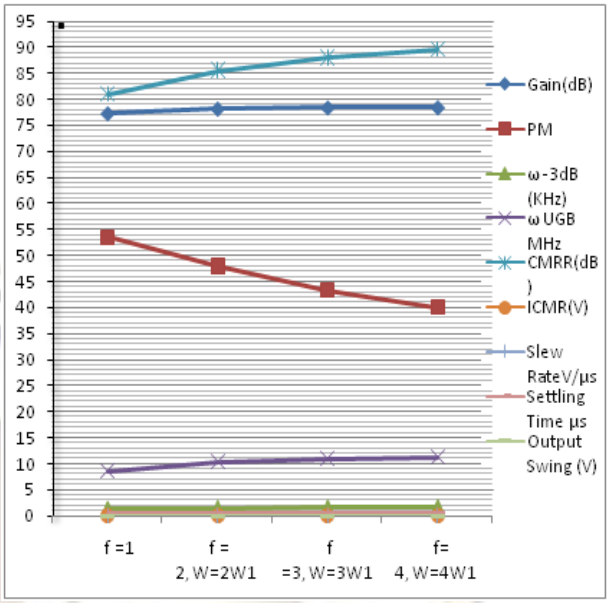

Figure 10.Variations in Parameters with increasing W

VI. Conclusion

This paper presented the full custom design of a two stage CMOS Op-Amp and analyzed its behavior for various aspect ratios. Design technique for this Op-Amp, its calculations and computer-aided simulation results are given in detail. The results show that the designed amplifier has successfully satisfied all the specifications given in advance. Tables and graphs of different parameters for various aspect ratios are drawn.

As a summary, a tables and graphs are provided to estimates the scaling limits for various applications and device types. The end result is that there is no single end point for scaling, but that instead there are many end points, each optimally adapted to its particular applications.

VII. Acknowledgements

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