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Physical Design Of Memory And Detection Of Stuck – At Faults

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Abstract

Fault detection in memories is an approach to practice fault analysis at the Transistor level of memory circuits by means of a specially designed fault injection block. This paper Proposed inject the single stuck-at fault at the nodes and observe the logic simulation of the block . This work introduces fault analysis capabilities to improve the skills in the field of memory testing. Test and diagnosis of memory circuits are therefore an important challenge for improving quality of next generation integrated circuits. During each memory **write cycle , the current data is written into that address of the memory selected and during the read cycle the data is read from the selected memory location. Both the input and output are compared and fault is detected depending on the results.**

Keywords— SRAM cell, Memory array, Counter Controller, Decoder.

1. INTRODUCTION

Memory is one of the technology devices in the integrated circuit business because of the highly repetitive nature of memory arrays. Relatively small improvements in the design of a memory bit multiplied by the large number of bits on a chip can make a big difference in chip cost and performance. A typical memory IC has addresses lines, data lines, and control lines. The address lines are used to identify the location of the memory storage element(s) or cell(s) to be read from or written to. The data lines contain the value of the data read or being written into the memory cells accessed.

The control lines are used to direct the sequence of steps needed for the read or write operations of the memory cell. The memory elements of an SRAM are arranged in an array of rows and columns. Each row of memory cells share a common "Word " line, while each column of cells share a common "bit" line. The number of columns of such a memory array is known as the data width of each word or length of a word.

In this modern era, electronic equipments and products have become part of our daily life. The Key components of an electronic product are integrated circuits. With the continuous increase of integration densities and complexities, the problem of integrated circuit testing has become much more accurate. Testing of integrated circuit is of crucial importance to ensure a high level of quality in both commercially and privately produced products. In the Stuck-at model, a faulty gate input is modeled as a stuck at zero or stuck at one. These faults most frequently occur due to gate oxide shorts (the NMOS gate to GND or the PMOS gate to VDD) or metal-to-metal shorts. When the poly of the PMOS transistor is permanently connected to VDD, then SA1 fault occurs, when the poly of NMOS is connected to VSS, SA0 fault occurs.

Other fault models include "Stuck-open "or "shorted"models. A particular problem that arises with CMOS is that it is possible for a fault to convert a combinational circuit into a sequential circuit. Bridging faults occur when two leads in a logic network are connected accidently and a wired logic.
These faults detect the manufacturing errors in the memory arrays. When the faults are detected we can find the rectification methods of those errors easily.

2. BLOCK DIAGRAM

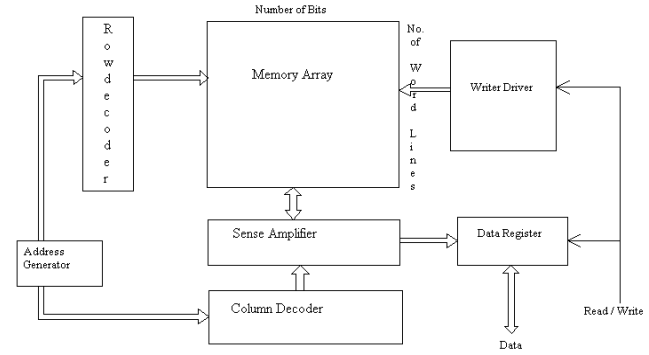

Fig 1: Block diagram of a typical memory IC

2.1 Design Description

The design is carried out in stages. The process of transforming the idea into a detailed circuit description in terms of the elementary circuit components constitutes design description. The final circuit of such an IC can have up to a billion such components; it is arrived in a step-by-step manner.
The first step in evolving the design description is to describe the circuit in terms of its behavior. The description looks like a program in a high level language like C. Once the behavioral level design description is ready, it is tested extensively with the help of a simulation tool.

It checks and confirms that all the expected functions are carried out satisfactorily. If necessary, this behavioral level routine is edited, modified, and rerun all done by manually.

Finally, one has a design for the expected system described at the behavioral level. The behavioral design forms the input to the synthesis tools, for circuit synthesis. The behavioral constructs not supported by the synthesis tools are replaced by data flow and gate level constructs. To summarize, the designer has to develop synthesizable code for the designs. The design at the behavioral level is to be elaborated in terms of known and acknowledged functional blocks. It forms the next detailed level of design description. Once again the design is to be tested through simulation and iteratively corrected for errors. The elaboration can be continued one or two steps further. It leads to a detailed design description in terms of logic gates and transistor switches.

2.2 SRAM CELL

The fundamental building block of memory is the SRAM cell. The cell is activated by raising the word line and is read or written through the data line. Fig 2: shows a 6-transistor (6T) SRAM commonly used in practice. Such a cell uses a single word line and both true and complementary bit lines is often called bit_b or bit. The cell contains a pair of cross-coupled inverts and an access transistor for each bit line. True and complementary versions of the data are stored on the cross coupled inverters.

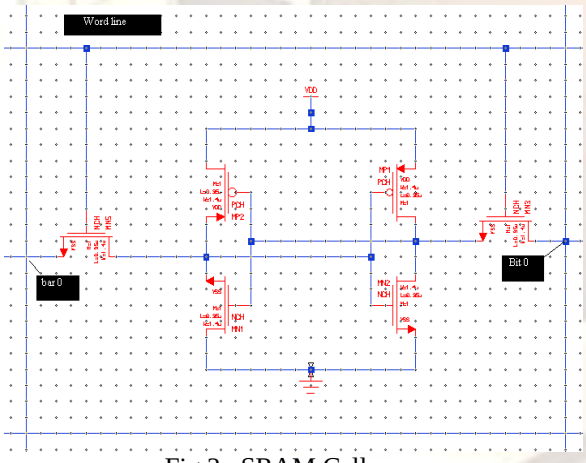

Fig 2: SRAM Cell

The basic storage element of an SRAM is a circuit that consists of 4 to 6 transistors. This multi-transistor circuit usually forms cross-coupled inverters that can hold a '1' or '0' state as long as the circuit is powered up. A pair of cross-coupled inverters have the output of one inverter going into the input of the other and vice versa, such that the output (and input) of one inverter is the complement of that of the other. A single SRAM memory cell is presented in a diagram above.

As can be noted, six total transistors are required for our design. Two NMOS and two PMOS transistors are used to construct a simple latch to store the data, plus two more pass NMOS transistors are controlled by Word Line to pass Bit Line and Bit bar Line into the cell. Write and Read operations are performed by executing a sequence of actions that are controlled by the outside circuit.

2.2.1 Write Operation

A Write operation is performed by first charging the Bit Line and Bitbar Line with values that are desired to be stored in the memory cell. Setting the Word Line high performs the actual write operation, and the new data is latched into the circuit.

2.2.2 Read operation

A Read operation is initiated by pre-charging both Bit Line and Bitbar Line to logic 1. Word Line is set high to close NMOS pass transistors to put the contents stored in the cell on the Bit Line and Bitbar Line.

2.3 Sense Amplifier

Sense amplifier circuit is an essential circuit in memory chips. It is shown in Fig 3: Due to large arrays of SRAM cells, the resulting signal, in the event of a Read operation, has a much lower voltage swing. To compensate for that swing a sense amplifier is used to amplify voltage coming off Bit Line and Bit Line. Sense amplifier also helps to reduce the delay times and power dissipation in the overall SRAM chip. There are many versions of sense amplifiers used in memory chips. The design used in our design is called a Cross-coupled Sense Amplifier.

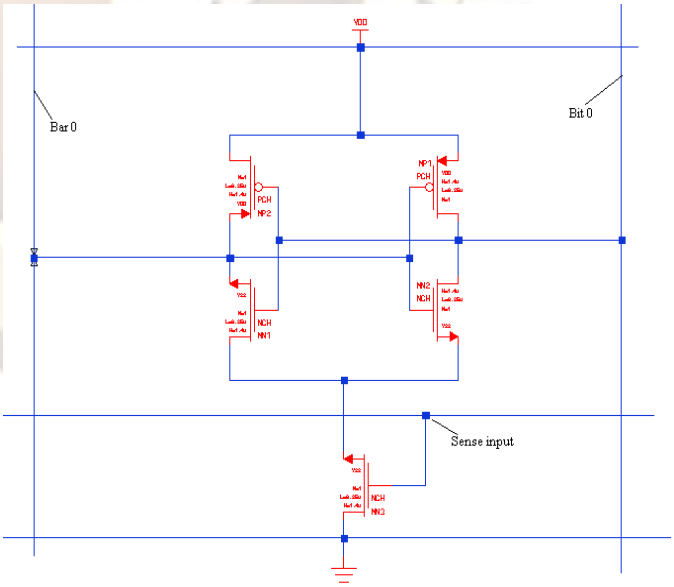

Fig 3:Sense amplifier

2.4 Decoder

The decoder is a collection of AND Gates using true and complementary versions of the address bits AND gates are formed by static NAND gates followed by an inverter. This structure is useful for more inputs. The NAND transistors are usually made minimum size to reduce the load on the buffered address lines because there are 2^{n-k} transistors on each true and complementary address line in the row decoder.

2.5 Counter

In this Design 4-bit counter is used as an address generator.

Based on count 2-bits are applied to row decoder and 2-bits are applied to column decoder. Counter selects row decoder and column decoder that in turn selects specific cell of memory and the data is written into the cell and that can be read.

Testing and testable design of high density RAMs dealt with fault modeling. Fault location or fault diagnosis is important for two reasons. First, finding the location of a fault is essential if the faulty RAM cell array has to be repaired in situation to make it operational. Second defects are caused by imperfections in the fabrication process. Another method of achieving fault tolerance is by the use of an error correcting code (ECC) in storing data. In the Read/Write circuitary, the faults commonly noticed are stuck-at-faults(SAFs) and dominant 0/1 bridging faults(0/1 BFs) and stuck-open addressing faults (SOAFs),Which transform the combinational address decoder circuit into a sequential circuit.

3. RESULTS AND DISCUSSIONS

Verification of the "Stuck at Faults" in the memory circuit shown below.

3.1 SA0 Fault in SRAM Cell

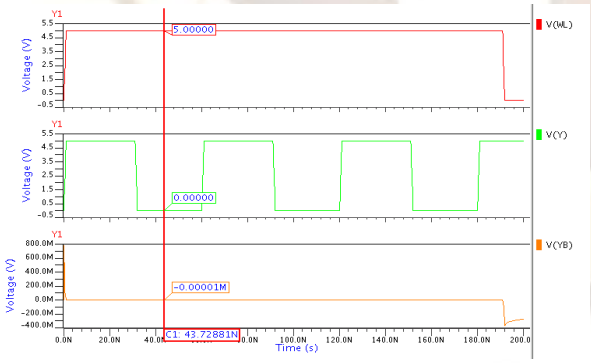

Fig 4: SA0 Fault in SRAM cell

3.2 SA1 Fault in SRAM

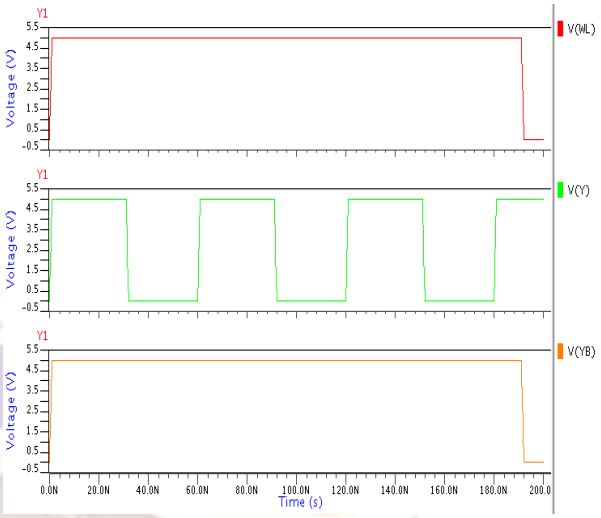

Fig 5: SA1 Fault in SRAM Cell

3.3 Fault free output in SRAM Cell

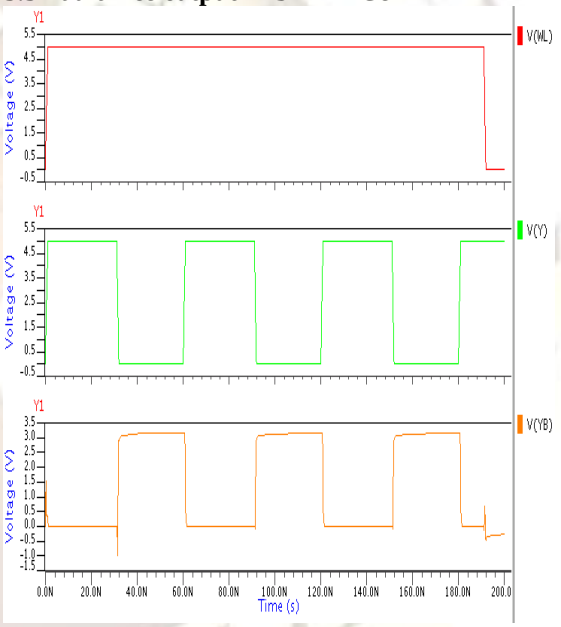

Fig 6: Fault free output in SRAM Cell

4 LAYOUT

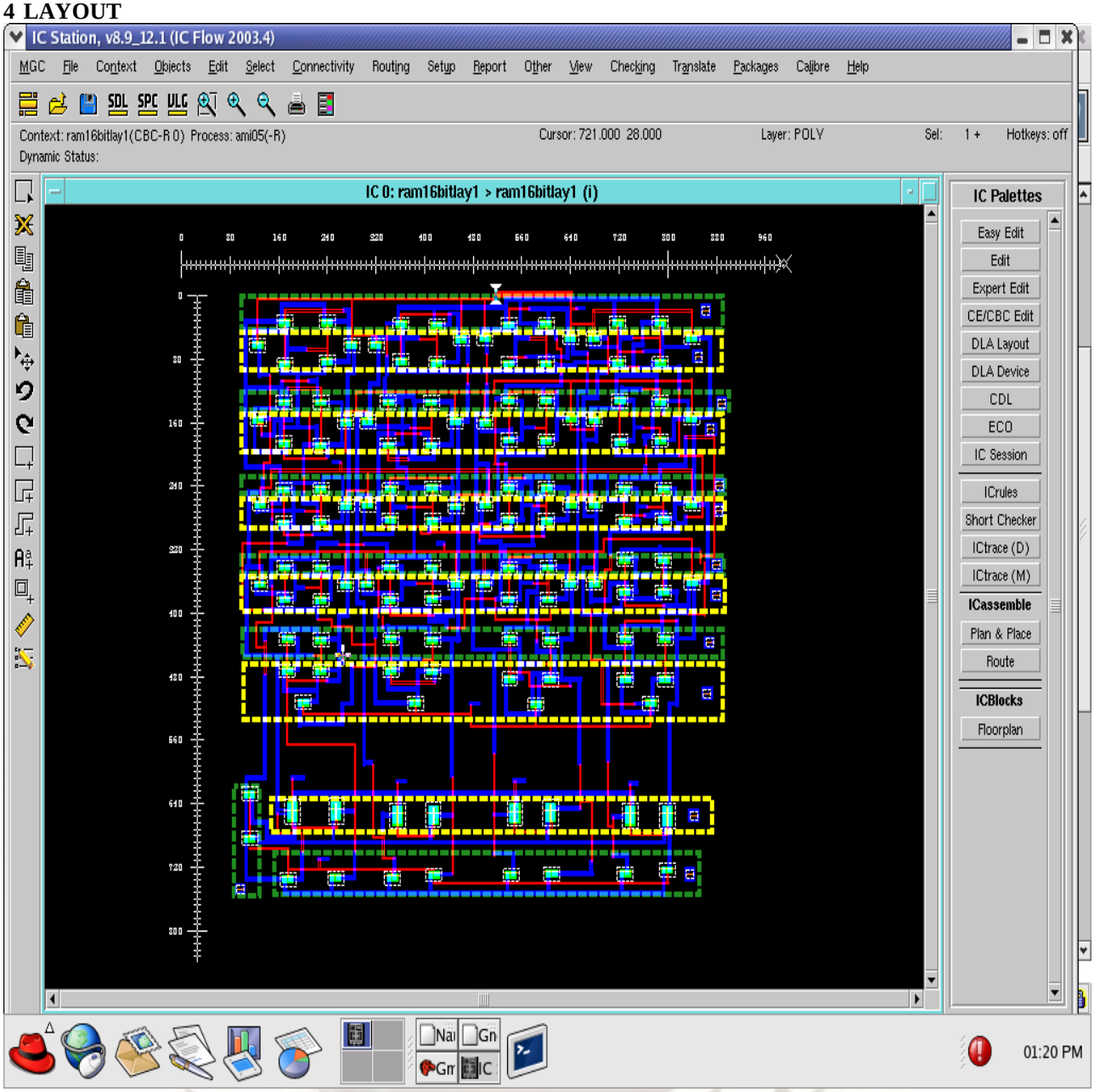

Fig 7: Layout of the typical memory IC

4.1 Layout Description

Once the placement and routing are completed, the performance specifications like silicon area, power consumed, path delays, *etc*., can be computed. Equivalent circuit can be extracted at the component level and performance analysis carried out. This constitutes the final stage called "verification" . One may have to go through the placement and routing activity once again to improve performance. The physical (mask layout) design of CMOS logic gates is an iterative process, which starts with circuit topology and the initial sizing of the transistors. After a topologically feasible layout is found, the mask layers are drawn (using a layout editor tool) according to the layout design rules. This procedure may require several small iterations in order to accommodate all the design rules. After the W/L values of the transistors are decided upon, the design entry is done in spice editor and the .cir is streamed out to carryout pre-layout simulations. Spice file can be used as source file in IC Station tool , Physical layout can be drawn , save that file with .gds file to generate netlist of the layout Then obtain the post layout simulation with exact functionality as pre layout simulation shown in waveform below.

4.2 The Post Layout Simulation Output Waveform

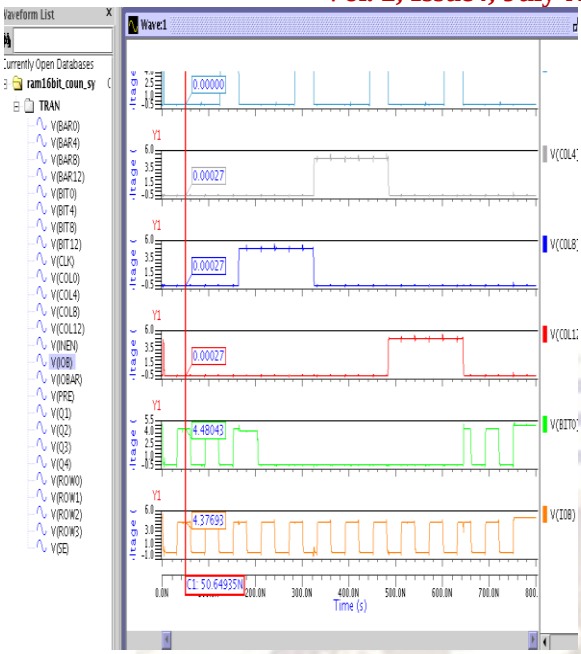

Fig 8: Waveform for the data on the bit0 line.

4.3 Comparisons Table

PARAMETER	PRE LAYOUT SIMULATION	POST LAYOUT SIMULATION
GLOBAL CPU TIME	250 ms	740 ms
CPU TIME	200 ms	650 ms
GLOBAL ELAPSED TIME	9 s	9 s
TOTAL POWER DISSIPATION	5.6942 mW	3.8717 mW
TEMP	27°C	27°C
MEMORY SPACE	558290 bytes	559807 bytes
NO. OF ELEMENTS	157	146
NO. OF NODES	65	65
NO. OF INPUT SIGNALS	12	12

Table 1: comparison between pre layout results and post layout results .

5. CONCLUSION

Diagnosis, repair and reconfiguration have become increasingly important issues in memory design .Manufacturing process technologies used nowadays produce a variety of defect mechanism that cause either yield loss or field failures in the integrated circuits. Some of these failures caused are permanent errors in RAM Arrays. Through the spice pre-layout simulations, the 'W' value for various transistors in the SRAM bit cell are determined and there by the W/L values are now conformed, the leaf cells are designed and the mask design is done for the entire memory structure, this procedure may require several small iterations to satisfy the DRC rules. Finally, all the blocks of the memory design are integrated to form a single memory. Designing the physical layout using IC Station Supported by Mentor Graphics. Parasitic extraction file and DRC and Post layout simulation of the design is performed using Calibre tool. Design rules are in built in this tool which automatically performs design rule check and hence facilitating us to draw an optimized layout. Memory is designed and observed how the each cell in a RAM is selected, and detected SA1 and SA0 faults, using spice simulation and Post route simulation.

6. REFERENCES

[1] Ferris –Prabhu , A. V." Improving Memory Readability Through Error Correction ," Comput.Des., July 1979 ,pp.137- 144

[2] Lewyn , L.L. AND Meindl , J . D ., " Physical Limits of VLSI DRAMSs," IEEE J. Solid State Circuits , Vol.20, 1985,pp.231-241.

[3] Nair,R., "Comments on An Optimal Algorithms forTesting Stuck-At Faults in Random Access Memories ," IEEE Trans .Comput., Vol.28,no .3 , 1979, pp.258-261.

[4] R.J Bakcer, H. W.Li, D. E. Boyce "CMOS design, layout and simulation", IEEE Press, 1998, www.ieee.org

[5] M. John, S. Smith, "Application Specific Integrated Circuits", Addison Wesley, 1997, ISBN 0-201- 50022-1, www.awl.com/cseng

[6] B. Razavi "Design of Analog CMOS integrated circuits", McGraw Hill, ISBN 0-07-238032-2,2001,

[7] Y. P. Tsividis "Operating and Modeling of the MOS transistor", McGraw-Hill, 1987, ISBN

[8] S. M Sze "Physics of Semiconductor devices", John-Wiley, 1981, ISBN 0-471-05661-8

[9] Y. Cheng, C. Hu "MOSFET Modeling & BSIM3 user's guide", Kluwer Academic Publishers, 1999

[10] A. Hastings "The Art of Analog Layout", Prentice- Hall, 2001, ISBN 0-13-087061-7

[11] N. Weste, K. Eshraghian "Principles of CMOS VLSI design", Addison Wesley, ISBN 0-201 53376-6, 1993

[12] K. Lee, M. Shur, T.A Fjeldly, T. Ytterdal "Semiconductor Device Modeling for VLIS", Prentice Hall, 1993, ISBN 0-13-805656-0

[13] W. Liu "Mosfet Models for SPICE simulation including Bsim3v3 and BSIM4", Wiley & Sons, 2001, ISBN 0- 471-39697-4

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