Low Power High Performance Baud Rate Generator using MTCMOS Voltage Interface Circuits

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ABSTRACT

Multiple supply voltages (multi-V_{DD}) is an effective technique for reducing the power consumption without compromising speed in an integrated circuit(IC). Different blocks of the design may be operated with different supply voltages. To transfer signals among the circuits operating at different voltage levels different level conversion circuits are required. Two types of Voltage Interface Circuits, feedback based and Multi- V_{TH} are implemented and used in the implementation of Baud Rate generator. The need for level conversion has delay and energy penalties. In this paper, the Voltage Interface circuits are individually optimized for minimum propagation delay. Baud Rate generator is designed and implemented using 90nm TSMC CMOS technology.

Keywords – Feedback based, Integrated circuits, Multi-V_{th}, Multi-V_{DD}, Voltage interface circuits

I. INTRODUCTION

Power is considered as the most relevant design objective for many classes of CMOS circuits, and has replaced more conventional metrics such as area, delay, or testability. Technology scaling has naturally helped low-power design. In fact, scaling implies lower supply voltages. Since dynamic power is proportional to the square of the supply voltage and scaling provides an effective way to reduce power consumption. Unfortunately, supply voltage scaling adversely affects performance of circuit.

The feedback based and Multi-V_{TH} based voltage interface circuits (level converters) are implemented here for minimum delay and low power. The standard level converters based on feedback has one or more feed back paths because of which delay is more. The new circuits employ multi-V_{TH} transistors in order to suppress the dc current paths in CMOS gates driven by low-swing input signals. These level converters (Voltage interface circuits) are compared with the feedback-based designed circuits for different values of the lower supply voltages in a multi-V_{DD} system.

In this paper, the Feedback and Multi-V_{TH} based voltage level converters are designed and implemented. Also, these level converters are used in Baud Rate generator. The Baud Rate Generator using Multi-V_{TH} level converter reduces power when compared with Baud Rate Generator with Feedback level converters. Section II reviews some basic concepts such as sources of power dissipation in digital CMOS circuits and section III describes Low Power Multi-V_{DD} techniques for reducing the power dissipation. Section IV introduces the level converters. Section V introduces the Design and Implementation of Baud Rate Generator. Baud Rate Generator is the component that allows varying signaling rate and communicates with other devices. Section VI discusses the results of all the level converters and baud rate generator implemented at transistor level using cadence Virtuoso tool in 90nm CMOS technology. Section VII presents the conclusion and future scope of the work.

II. SOURCES OF POWER DISSIPATION

The major sources of power dissipation in CMOS circuit can be summarized as follows.

i. Dynamic Power Dissipation

Current flows from V_{DD} to GND when logic transition occurs. Dynamic power is due to the dissipation during the capacitances charge/discharge process. CMOS circuits dissipate power by charging the various load capacitances whenever they are switched. In one complete cycle of CMOS logic, current flows from V_{DD} to the load capacitance to charge it and then flows from the charged load capacitance to ground during discharge:

$$P = CV^2f ------------(1)$$

Since most gates do not switch at every clock cycle, they are often accompanied by a factor α, called the activity factor. Now, the dynamic power dissipation may be re-written as:

$$P = \alpha CV^2f -----------(2)$$

ii. Static Power Dissipation

Static power dissipation occurs when current flows from V_{DD} to GND regardless of logic transition. It consists of three components, (a) Sub-threshold condition when the transistors are off, (b) Tunneling current through gate oxide and (c) Leakage current through reverse biased diodes.

iii. Short circuit Power Dissipation

Since there is a finite rise/fall time for both PMOS and NMOS, during transition from off to on, both the transistors will be on for a small period of time in which current will find a path directly from V_{DD} to ground, hence creating a short circuit current. Short circuit power dissipation increases with rise and fall time of the transistors [4].

III.   MULTI-V_{DD} TECHNIQUES

Even though many low power techniques are existing to reduce dynamic power, Multi-V_{DD} is efficient. Dynamic power is directly proportional to power supply. Hence naturally reducing power significantly improves the power performance. At the same time gate delay increases due to the decreased threshold voltage. High voltage can be applied to the timing critical path and rest of the chip runs in lower voltage. Overall system performance is maintained. Different blocks having different voltage supplies can be integrated in SoC. This increases power planning complexity in terms of laying down the power rails and power grid structure[1]. Level shifters are necessary to interface between different blocks. Multi voltage design strategies can be broadly classified as:

Static Voltage Scaling (SVS): Different voltages are applied to different blocks or subsystems, but they are fixed voltage sources in the SoC design.

Multi-level Voltage Scaling (MVS): The block or subsystem of ASIC or SoC design is switched between two or more voltage levels. But for different operating modes limited numbers of discrete voltage levels are supported[3].

 Dynamic Voltage and Frequency Scaling (DVFS): Voltage as well as frequency is dynamically varied as per the different working modes of the design so as to achieve power efficiency. When high speed of operation is required voltage is increased to attain higher speed of operation with the penalty of increased power consumption[6].

Adaptive voltage Scaling (AVS): Here voltage is controlled using a control loop. This is an extension of DVFS[9,10].

IV. LEVEL CONVERTERS

In this section various level conversion techniques are considered. The issues related to the standard feedback-based level converters and the multi-V_{TH} level converters in CMOS technology are discussed here. When a low swing signal directly drives a gate that is connected to a higher supply voltage, the p-type transistors in the pull-up network of the receiver cannot be fully turned off. Static dc current is produced by the receiver driven by low voltage swing signal. To reduce this dc current, voltage interface circuits are used between

a low voltage driver and a full voltage swing receiver [5,11,12].

A. Feedback-Based Level Converters

The operation of p-type transistors in the pull-up network is controlled by an internal feedback mechanism. This is not directly operated by the low voltage swing input signal. Therefore it avoids the formation of static dc current paths within the circuit. Due to the slow response of the internal feedback circuitry, these traditional level converters suffer from high short-circuit power and long propagation delay [7].

The n-type transistors in the pull-down network are driven by low voltage swing signals unlike the p-type transistors in pull-up network that receive higher gate overdrive voltages from the full-voltage swing feedback paths. Particularly, at very low input voltages, the widths of the transistors that are directly driven by the low-swing signals need to be significantly increased to balance the strength of the pull-up and the pull-down networks. This causes further degradation in the speed and the power efficiency of the level converters when utilized with very low input voltages. Only two circuits are considered from standard feedback based level converters [12].

i. Standard Feedback-Based Level Converter, LC1

The standard feedback-based level converter , LC1 is shown in Figure1. The circuit has two feedback paths and delay is more with this.
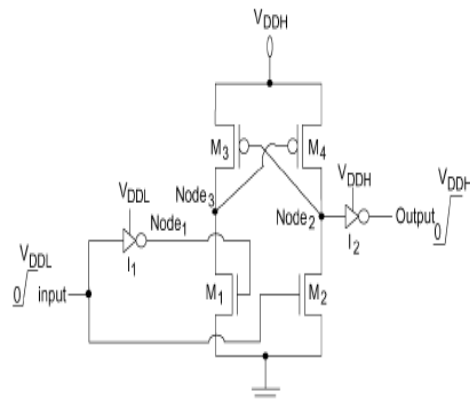

Figure1. Standard level converter, LC1

ii. Feedback based Level Converter, LC2

To improve the speed of operation while compared to level converter LC1, level converter LC2 is designed. With only one feedback path, delay is reduced. The circuit diagram level converter LC2 is shown in Figure2.
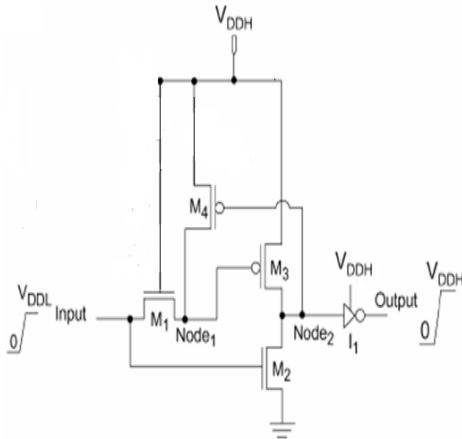
Figure2. Level converter, LC2

As LC1, LC2 also consumes significant short-circuit power during both low-to-high and high-to-low transitions of the output. Furthermore, when V_{DDL} is reduced, the size of M2 must be increased significantly for maintaining functionality. The load seen by the driver circuit therefore increases at lower V_{DDL}[11].

B. Multi-V_{th} Based Level Converters

The feedback based level converters depend on the feedback, but the Multi-V_{th} based level converters employ a multi-V_{th} CMOS technology to eliminate the static dc current. The high threshold voltage pull-up network transistors in this type of level converters are directly driven by the low-swing signals and they do not produce static dc current problem[8,12].

i. Multi-V_{th} Based Level Converter, LC3

The circuit diagram of level converter LC3 is shown in figure3. This circuit also takes low supply voltage as input and converts to a higher voltage level.
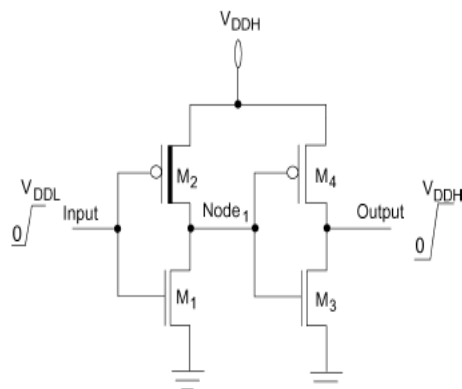

Figure 3. Level converter LC3

ii. Multi-V_{th} Based Level Converter LC4

The circuit of *Multi-V_{th} Based* level converter LC4 is shown in Figure 4.
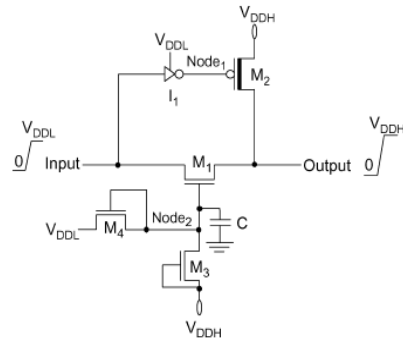

Figure4. Level converter LC4

iii. Multi-V_{th} Based Level Converter LC5

Another circuit of *Multi-V_{th} Based* level converter, LC is shown in Figure 5. This circuit is best among all the above mentioned in terms of power and delay.
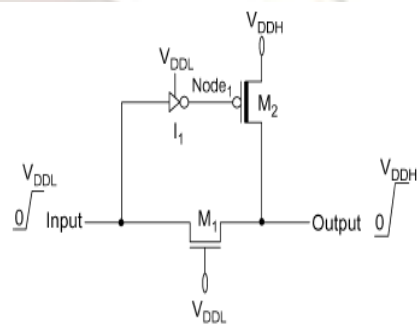

Figure5. Level converter LC5.

V. BAUD RATE GENERATOR

Baud rate generator is the component which allows varying the signaling rate and communicates with other devices. The baud rate generator is an oscillator. It provides a frequency signal which is used to control the timing on the serial interface. Since different line speeds need a different timing, the baud rate generation needs to be flexible.

There are two general ways to achieve a flexible baud rate generation. Either the baud rate generator itself is programmable and can produce the necessary different frequencies, or the UART has a programmable divider or multiplier, which converts the frequency from the baud rate generator into the required frequencies.

Depending on the actual UART, the baud rate generator either needs to be some external component, or it is directly integrated into the UART chip. From the outside, the programmatic change of the baud rate generation is the means to control the speed of the serial connection. Often when programming the baud rate one doesn't provide the desired baud rate in 'clear text', but needs to provide some divider or factor. Providing the right divider or factor requires knowing the basic frequency of the used baud rate generator.

The Verilog code for the Baud rate generator is developed and simulated using the Xilinx ISE simulator and also synthesized using the XSTSynthesizer. The gate level schematic of the baud rate generator is considered as the logic block diagram. The Logic block diagram of baud rate generator is shown in figure6. It consists of four different block are 4-bit count, 8-bit count, 3-bit count and 8x1Multiplexer.
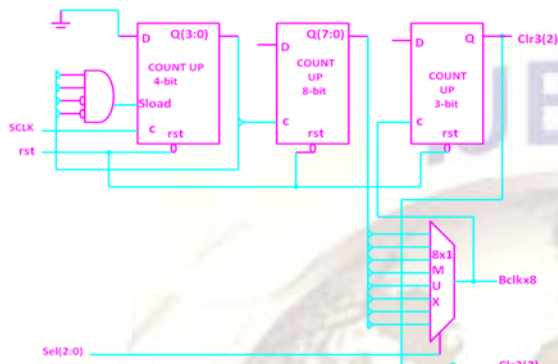

Figure6. Logic Block diagram of Baud rate generator

VI. RESULTS

All level converters are designed using Cadence Virtuoso Schematic Editor. Simulation waveform for standard level converter is shown in figure7. Table1 shows the comparison of power and delay values of the different level converters.
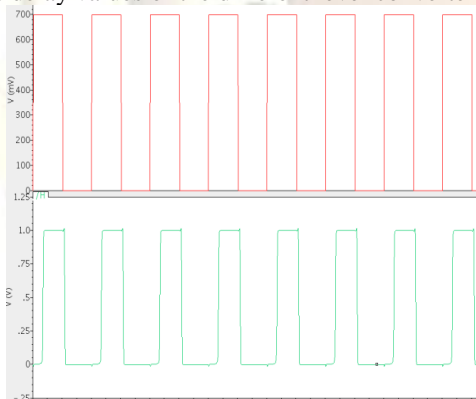

Figure 7. Simulation waveform of standard level converter

TABLE1 :Comparison of Power and Delay calculations of the level converters

Level Converter	Power (µw)	Delay (ns)
LC1	11.26	1.081
LC2	3.81	1.069
LC3	3.341	1.034
LC4	2.137	1.011
LC5	1.897	1.010

The schematic diagram of baud rate generator (BRG) is shown in figure8.
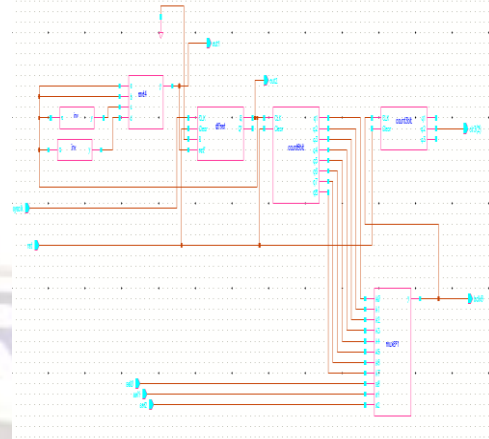

Figure8. Schematic diagram of baud rate generator. The Test Bench of baud rate generator is shown in figure9.
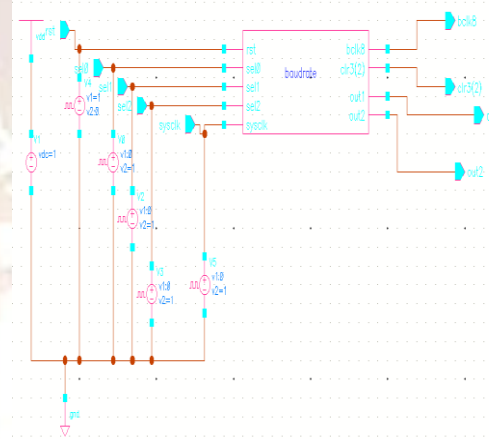

Figure9. Test Bench of baud rate generator.

The Simulation waveform of baud rate generator is shown in figure10 and figure 11 shows the out put waveforms of the baud rate generator with level converters. Figure 12 and figure 13 shows the power of the baud rate generator with and without level converters.
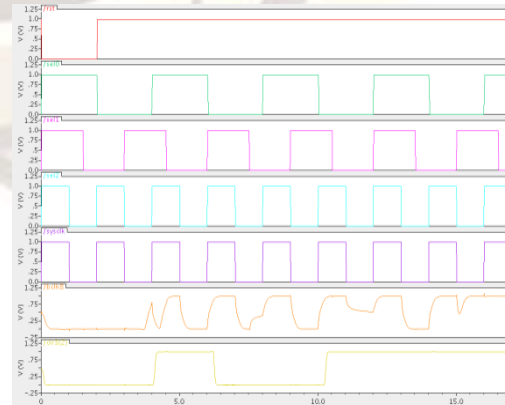

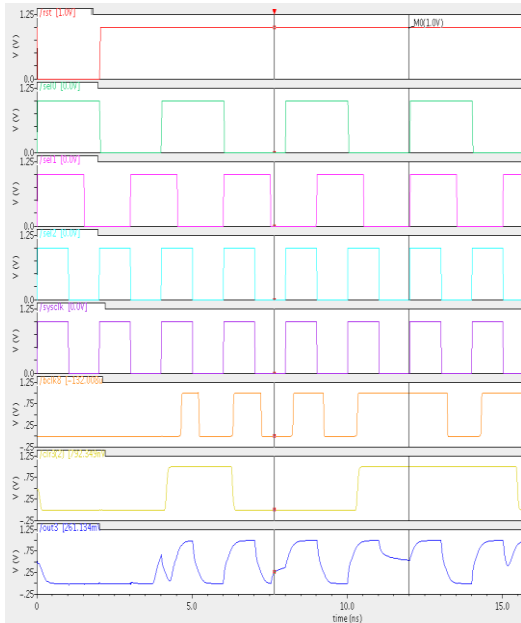Figure10. Simulation waveform of baud rate generator.

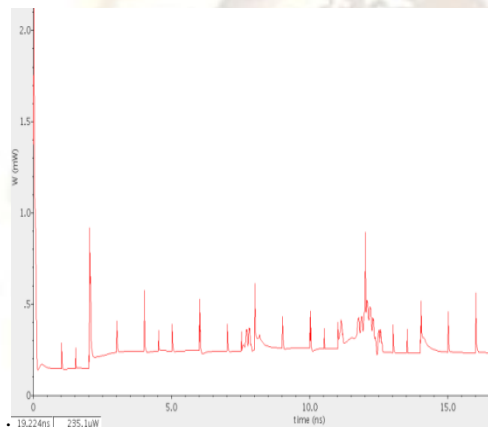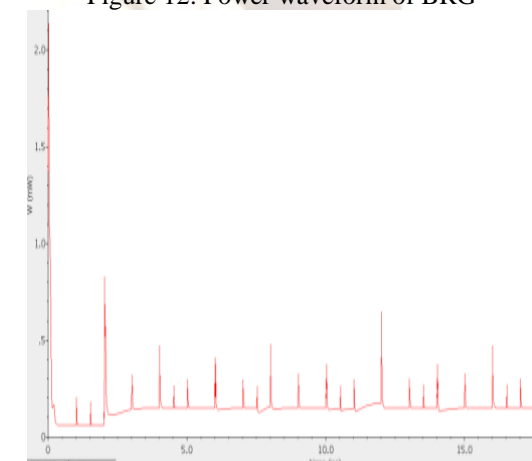Figure 11.Simulation waveform of BRG with level converter

TABLE II: Comparison of Power for baud rate generator with different level converters

Baud rate Generator with Level Converter	Power (µw)
LC1	322.3
LC2	136.6
LC3	301.4
LC4	133.6
LC5	122.3

Figure 12. Power waveform of BRG

Figure 13 Power output of BRG with level converter

VII. CONCLUSION

In the standard feedback based level converters the low voltage level is converted to high voltage level based on feedback. But the Multi-Vth circuits employ multi-V_{TH} transistors in order to suppress the dc current paths in CMOS gates driven by low-swing input signals. These level converters are compared with the feedback-based designed circuits for different values of the lower supply voltages in a multi-V_{DD} system. When the circuits are individually optimized for minimum power consumption in a 90nm technology, the multi-V_{TH} level converters offer significant power savings as compared to the feedback-based circuits. Alternatively, when the circuits are individually optimized for minimum propagation delay, speed is enhanced in the multi-V_{TH} circuits. Significant power savings are observed when Multi-Vth level converter LC5 is used as interfacing circuit.

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