A 1.8 Ghz-2.4 Ghz Fully Programmable Frequency Divider And A Dual-Modulus Prescaler For High Speed Frequency Operation In PLL System Using 250nm Cmos Technology

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ABSTRACT

A Programmable Dual-modulus Prescaler and a fully programmable Frequency divider with 250nm are presented in this paper. The Dual-Modulus prescaler includes a synchronous counter and a asynchronous counter. A high sped dynamic D-FF is used in cmos phase locked loops for GHz applications that reduce the power consumption. Dynamic D-FF is constructed using True single phase clock logic (TSPC).The maximum operating frequency varies between 1.8 GHz – 2.4 GHz with power consumption of 24mw at 2.5v supply voltage.

Keywords - Frequency divider, high speed dynamic logic, Logic Flip-Flop, Phase Locked Loop.

I. INTRODUCTION

In the study of PLL there is requirement of frequency divider also called Prescalers.Frequency divider is an important factor in performance of PLL because it provides the feedback path. However without feedback path frequency locking gets difficult. The Implementation of Frequency divider in GHz application is done by choosing a vco into loop to the range of signal, The reason for that is there is no practical means to generate a pure & stable reference frequency above few GHz. Such a feedback system able to lock a high frequency vco output to lower frequency signal is called phase locked loop(PLL)[1].Fig 1. Shows the complete PLL system. To describe the behavior of PLL frequency divider a linear model is used. For phase locking mechanism, the phase domain is chosen for analysis. We proceed here with the analysis of each building block which is modeled in phase domain.

A. Phase Frequency Detector –

The *phase-frequency detector (PFD)* can be interpreted as a functional block having the output signal proportional to the phase difference between the two input signals. The proportionality factor is set to be 1 (unitless).

B. Charge-pump (CP)-

Can be modeled as a trans-conductive block, transformingThe phase difference into a proportional current.

C. Loop Filter –

the *loop filter* purpose is to integrate the current pulses generated by the PFD/CP blocks.

D. Voltage control oscillator -

In the phase domain, the *voltage-controlled oscillator (VCO)* can be modeled like an integrator having a proportionality factor of kvco.

E. Frequency Divider –

There are three types of frequency divider cascaded divider by two stages, Dual- modulus prescaler, programmable divider (divide by N). This paper presents a frequency divider by a factor N & a dual modulus prescaler which divides phase of input signal by N.

The paper starts with section II. Includes a description of fully programmable frequency divider architecture. Section III explains the working of programmable frequency divider and a dual modulus prescaler. Section IV provides a comparison with previous work and this work. Section V provides concluding remarks.
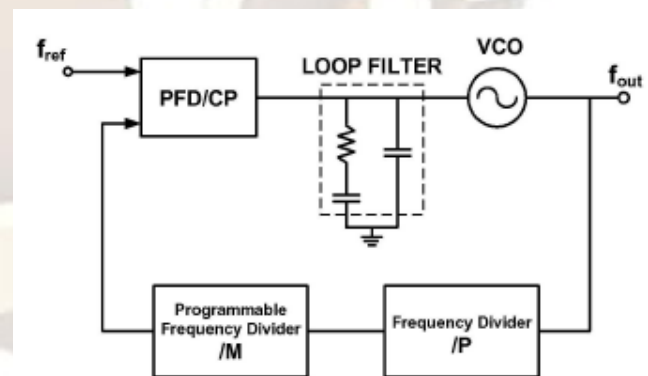

Fig 1. PLL System Architecture

II. FREQUENCY DIVIDER ARCHITECTURE

High-frequency operation is attained when the logic function is kept simple. The programmable dividers have a fixed-modulus high-speed divider as its first stage. In this context, the fixed-modulus divider is commonly referred to as a prescaler. Scaling down the signal frequency makes it possible

to have a presettable asynchronous divider after the prescaler. This approach limits the clock loading and the overall divider power consumption, while allowing for high-speed operation. The obvious drawback, however, is the necessity of lowering the reference frequency to get the same frequency resolution. If a presettable modulo-P divider follows a modulo-N prescaler, the overall frequency divisionRatio is NP. Thus, the reference frequency has to be lowered exactly by the modulus of the prescaler N. This would imply narrowing the loop bandwidth, which may be undesirable.Atypical solution is the pulse-swallowing technique. [2, 3] If S input pulses are swallowed in the preceding arrangement, the output period becomes longer by S reference periods. Therefore, the overall frequency division ratio is $M = (NP +S)$, which can be varied in unity steps by changing S. A pulse-swallower circuit is shown in Figure 2. Assuming $P > S$. The output signal Acts as a 'swallow enable'. The first stage is a dual-modulus prescaler, i.e., a high-speed counter whose modulus can be alternated between two numbers. The modulus control is set either to $(N + 1)$ or to N, depending on the output signal. Hence, the output signal has a period equal to: $S(N + 1)T\text{in} + (P − S)NT\text{in} = (NP + S)T\text{in}$ where $T\text{in}$ is the input clock period. The modulo-P counter is commonly referred as a program counter, while the modulo-S counter is called the swallow counter. The inequality $P > S$ and the required division ratios identify a set of possible values of N, P and S.
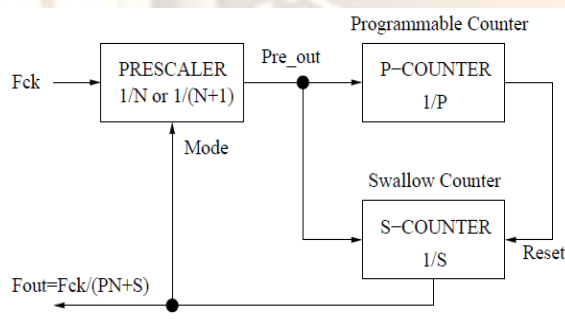

Fig 2. Programmable frequency divider

Fig 2.shows a dual-modulus frequency divider consist of a dual -modulus prescaler, programmable counter (P-CNTR)& swallow counter(S-CNTR).Initially, the mode signal sets the prscaler to divide the input signal frequency by N+1,then P-CNTR & S-CNTR count the prescaler output,F_{ck}/N+1,P & S times respectively. When counter number S is smaller than P, S-CNTR counts S times & then controls the prescaler by mode signal so that the prescaler divides the input signal by N times,& P-CNTR counts (P-S) cycles with the prescaler output which is F_{ck}/N. When the P-CNTR, completes its cycle, it resets the S-CNTR & the mode signal sets the prescaler to divide the input by N+1.Therefore after one complete cycle the frequency of output signal F_{out} will be given as $F_{out} = F_{ck}/[(N+1).S+N.(P-S)]=F_{ck}/(NP+S)$

A. Frequency Divider for Multi-Standard Applications

There are standards in modern wireless communication applications as shown in Table 1.Multiple wireless standards requires various division ratios of a prescaler & those of P-CNTR & S-CNTR. Prescaler division ratios can be obtained from building several prescalers for each wireless standard. Some commercial products are available in the market which have limited division ratios, such as 2^n,n=1,2 or dual-modulus division ratios of 4/5,6/7,8/9 or 10/11…etc.These fixed ratios are selected by designer according to his own frequency planning.

Wireless standards	RX [MHz]	TX [MHz]	Ch. space	Access scheme
GSM	935-960	890-915	200KHz	TDMA/FDD
DCS 1800	1805-1880	1710-1785	200KHz	TDMA/FDD
PCS 1900	1930-1990	1850-1910	200KHz	TDMA/FDD
DECT	1880-1900	1880-1900	1.73MHz	TDMA/FDD
IS-95	869-894	824-849	1.25MHz	CDMA/FDD
WCDMA	2110-2170	1920-1980	5MHz	CDMA/FDD

Table1. Wireless standards

With reference to above table aim of this paper is to design a programmable frequency divider which covers a range of frequency such as 1.8GHz for DCS (voice) application & 2.4GHz for Bluetooth (Data).

B. Frequency Division Method:DR-MR

A dual-modulus frequency division is described as $F_{div}=F_{ch.}.(N.P+S)$ where F_{div} is the output signal frequency of frequency divider,F_{ch} is channel space,N is division ratio of prescaler,P is division ratio of P-CNTR,S is division ratio of S-CNTR. For a DCS1800 system application which has receiver band of 1805-1880MHz with 200KHz of channel spacing, $F_{div}=0.2*[9025+(0-375)]$MHz. 9025 = 5*5*361. N can be set to 5 or 25.If a prescaler can only provide a division ratio of 16, then P-CNTR must be able to provide the division ratio of 564.0625.This is a decimal point so it is not possible by P-CNTR to provide the decimal division using simple divide by 2 or 2^n operation using T-FF. This difficulty can remove by maintaining the simple dual-modulus scheme by manipulating and remapping values of NP & S.This division method is called "Division Ratio-Manipulation & Re-mapping (DR-MR). Table 2, shows the DR-MR division for DCS1800 & Bluetooth system.

Standard	DR:F_{ch}[NP+S] MHz	MR:F[NP+S] MHz
DCS1800	0.2[9025+(0-375)]	0.2[9024+(1-376)]
Bluetooth	1[2402+(0-78)]	1[2400+(2-80)]

Table 2.Dual-Modulus division schemes using DR-MR

III. PRESCALER ARCHITECTURE

Frequency divider employ prescalers so that lower frequency signal can be applied to the Programmable counter,ie P-CNTR & S-CNTR. Prescalers can be made using simple2^n architectures or dual modulus architectures. Table 3. Shows different prescaler used in commercial PLL system.

Manufactures	Product No.	Division Ratios	Applications
ADI	ADF4210 series	8/9,16/17,32/33	GSM,PCS
Fujitsu	MB15F03 SL	8/9,16/17,64/65	SM,DCS, PCS
Conexant	CX&4016	8/9,32/33	GSM,DCS
National semi.	LMX2305	64/65, 128/129	PCS, WLAN

TABLE 3. Dual-Modulus prescaler in commercial products.

A. Design of High speed D-FF

To implement a D-FF is by mean of *dynamic* logic. In this Kind of realization, the logic state is stored in the parasitic capacitance of a high impedance node of the circuit. This method provides very high speed of operation, but imposes a limit on the minimum refresh frequency at which the circuit can operate. In fact, this type of state storing mechanism has the drawback of being sensitive to the leakage currents discharging (or charging, depending on the logic value stored in the node) the small parasitic capacitances. If the clock period is longer than the time needed for the voltage (representing the logic state) to drop below the logic threshold, the functionality of the circuit would be compromised. A dynamic logic D-FF needs to be edge-triggered. To this extent, the circuit timing is decomposed into the so called *pre-charge* and *evaluation* phases. The principle of operation is exemplified in Fig. 12The circuit shown in Fig 3. Is positive edge-triggered, meaning that the input D is sampled in correspondence of the clock rising edge. The input portion of the circuit (pre-charge), is transparent when the clock is in the low state (logic 0). During this time interval, the node A is reproducing the logic value provided at the input node D. When the clock

switches to the high state (logic 1), the input portion of the circuit becomes no longer transparent to the input, and the logic value stored at the node A is passed to the output node Q. Since the output Q reproduces the input value at the time the clock switches from the low state to the high state (but it could have been the opposite), this kind of logic is said to be edge-triggered.For the purposes of this work, the selected D-FF topology is shown in Fig 4.The presented schematic is an evolution of the D-FF proposed in [4].In high operating speed Tspc type D-FF can be used as it works at very high frequency. There are different types of Tspc D-FFs are proposed [5], [6], [7], [8], [9].
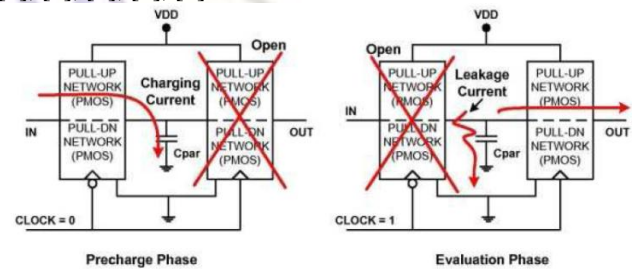

Fig 3.Precharge & Evaluation phases in a Dynamic logic

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A. Divide by 2 divider using Tspc Toplogy

Tspc divider topology [10] is based on D type Flip-Flop. It was first proposed by Yuan & svensson(1989) & as shown in fig 4(a) requires only one single clock phase & contains only nine transistor, owing to small number of transistor & small delay from D to 'out' the operation frequency can be high. Therefore Tspc divider is suitable architecture for a divider as compared to static divider when working at high frequencies. However Tspc requires the input clock to have a nearly rail to rail voltage swing in order to achieve high frequency operation. Operation of Tspc D-type Flip-flop is as follows and consists of two working nodes: the evaluation mode & Hold mode. When clk is high the D type Flip-flop works in evaluation mode if node n1 is high the transistor mn2 & mn3 are turned on. Node n2 will be pulled low & output B becomes high. If node n1 is low the transistor mn2 is turned off & node n2 which was previously precharged remains high. Thus the state of outB becomes low. Therefore node n1 is transparent to node output outB in evaluation mode. When clk is low D type Flip-flop works in hold mode namely precharged mode. Node n2 is precharged to high through Mp3, transistors mn3 & mn5 are off the value at outB is held. When feedback from output is not applied to the input the circuit will behave as a simple D-FF.Now, Fig 4(a) explains the working of divide by two circuits which have clk input as output of previous stage & output being feedback to D input. As value of node 1 is inverted

value of input D when data at node1 is transmitted to outB in evaluation mode. The data at outB becomes inverted value of input D. when output node outB is feedback to D outB will toggle its own state after two clock cycles. Hence it performs divide by two circuit function.
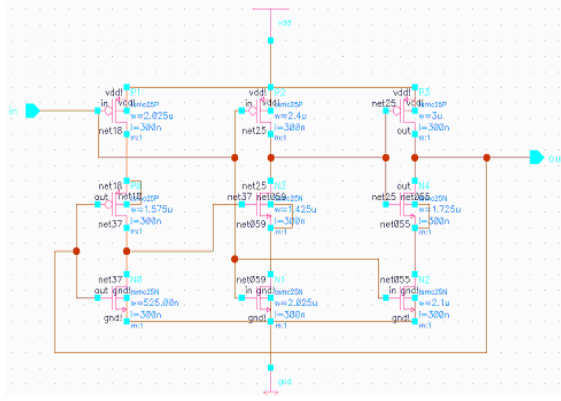

Figure 4(a) Divide By-2 Divider using Tspc Topology

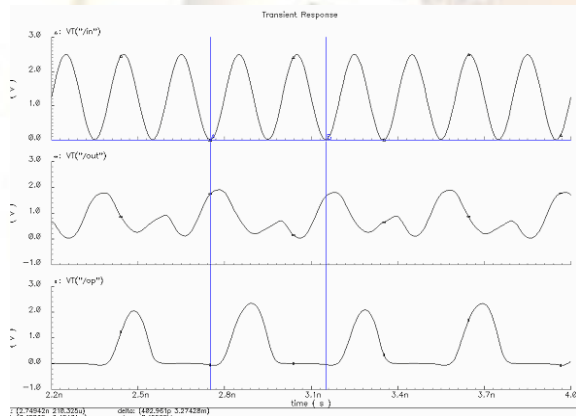Figure 4(b) shows the divide by-2 divider Transient simulated waveforms for (i)sine wave input.(ii)square wave input.

Fig 4(b)(i) divide by-2 Transient waveform for sine wave input
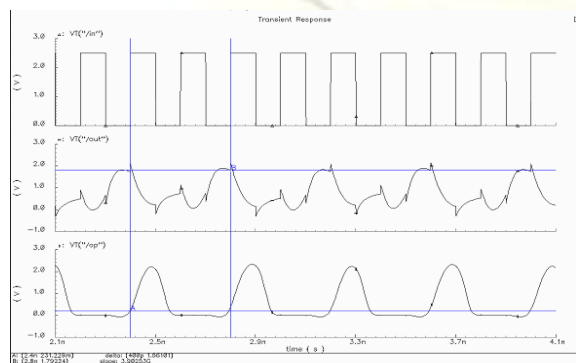
Fig 4(b)(ii) divide by-2 Transient waveform for square wave input

C. Design of 2/3 Prescaler using Tspc Toplogy

Using divide by-2 Tspc topology we can design 2/3 prescaler.This prescaler is used in design of other prescalers that depends on designers own frequency division choice.To understand the working of divide by2/3 prescaler we have to know the working of divide by 3 which is explained in fig 5(a). DFF (DFF1) and the combinational gate G are inserted in the feedback path of the dividerthen the system can be in three states: Q1 Q2 = 01, 10, and 11. The Q1 Q2 = 00 is Obviously illegal as that implies the previous values of Q2 and G would have had to be in the impossible states of `0' and `1', respectively. In order to control the mod-select an extra gate is required, such as the OR gate in Figure 5(b) this simple 2/3 divider Works in divide-by-2 mode when Mod Select is `1' and in divide-by-3 mode for Mod Select `0'. The above discussion can be extended to higher division moduli 2N/2N+1 prescalers easily.
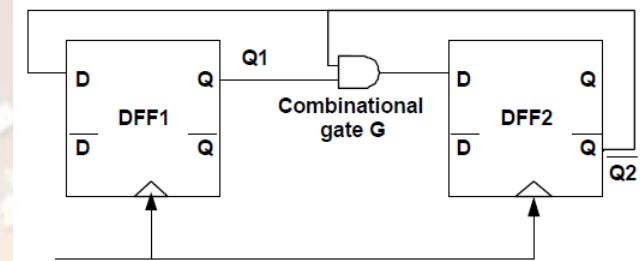

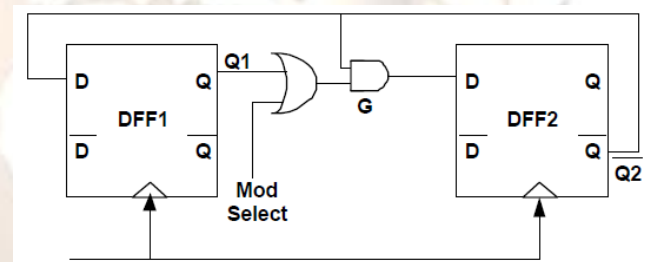Fig 5(a) Divide by-3 Block representation

Fig 5(b) Divide by-2/3 Prescaler Block representation

Fig 5(c) shows the Schematic diagram of 2/3 prescaler and Fig 5(d) shows the transient waveform for 2/3 prescaler (i)for sine wave input when MC=0 and MC=1.(ii)for square wave input when MC=0 and MC=1.
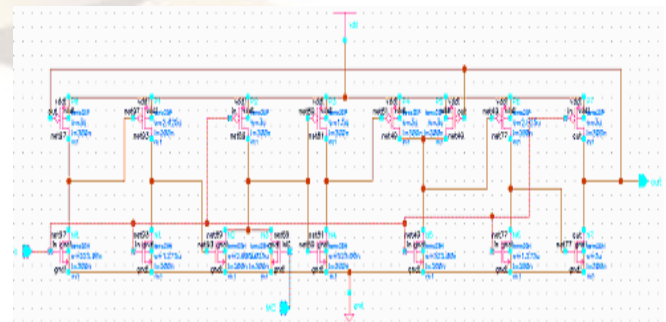

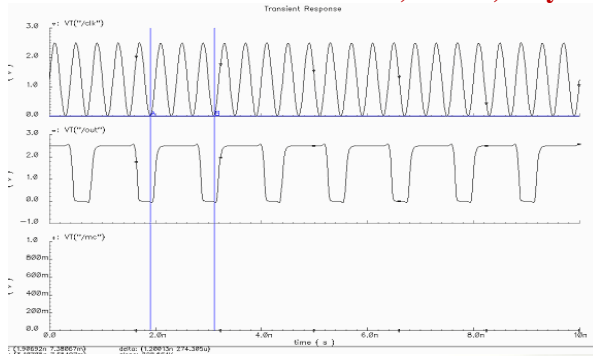
Fig 5(c) Schematic of 2/3 Prescaler

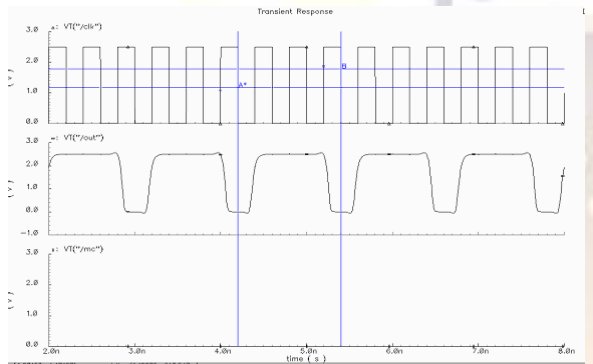Fig 5(c)(i)Transient waveform for 2/3 Prescaler for sine wave input when MC=0

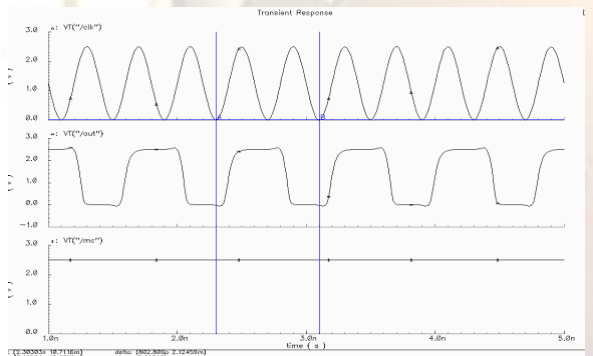Fig 5(c)(ii)Transient waveform for 2/3 Prescaler for square wave input when MC=0

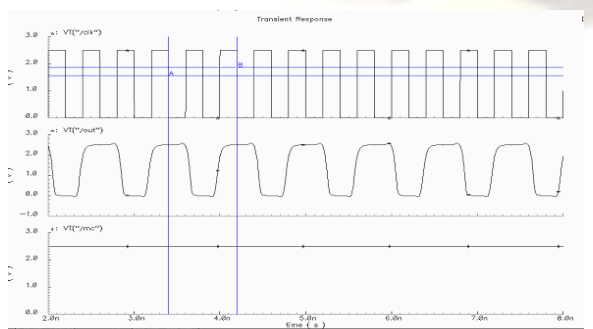Fig 5(c)(iii)Transient waveform for 2/3 Prescaler for sine wave input when MC=1

Fig 5(c)(iii)Transient waveform for 2/3 Prescaler for square wave input when MC=1

D.Design of 8/9 Prescaler using 2/3 Prescaler

he 8/9 prescaler is designed using 2/3 prescaler,This prescaler is chosen as it satisfies the frequency division range which is required,referring table 3.The 8/9 dual modulus prescaler is illustrated in Figure 6. The synchronous portion, which works at maximum frequency, is the critical block to design. The master-slave D ip-ops FF1 and FF2 perform conventional divide-by-4 in the absence of a pulse-swallow" signal. Such a control signal can be suppressed by disabling FF3 when Mod-Select signal is inactive. The output of the FF2 is further divided asynchronously to generate a divide-by-8 signal. When this divide-by-8 signal, Q4, is combined with the Mod-Select signal appropriately, ip-op FF3 gets included in the divider feedback loop in such a way that FF1 is forced to hold state for exactly one extra clock period. The output of the synchronous portion now has a duty cycle of 3/5, i.e., the output Q2 is high for 3 and low for 2 clock periods. Q2, obviously, follows a high for 2, low for 3 clock-periods trend by virtue of the differential operation of the current mode logic. As the synchronous pulse clocks the asynchronous divider, this translates into Q3 being high for 5, low for 4 pulses (and vice-versa for Q3). The time period of the prescaler output is now 9 pulses giving it the 8/9 modulus operation.
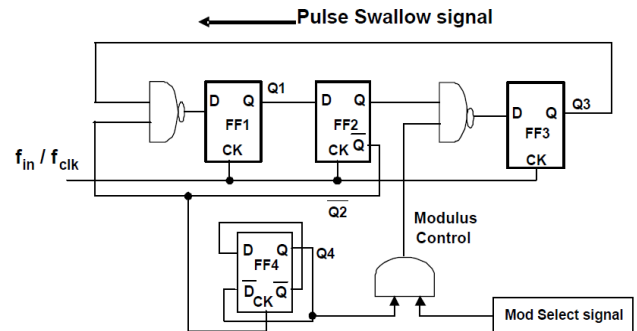

Fig 6. 8/9 Prescaler Block representtion

Figure 7.shows the transient simulated waveform for8/9 Prescaler(a) sine wave & (b) square wave input for   MC=0,1
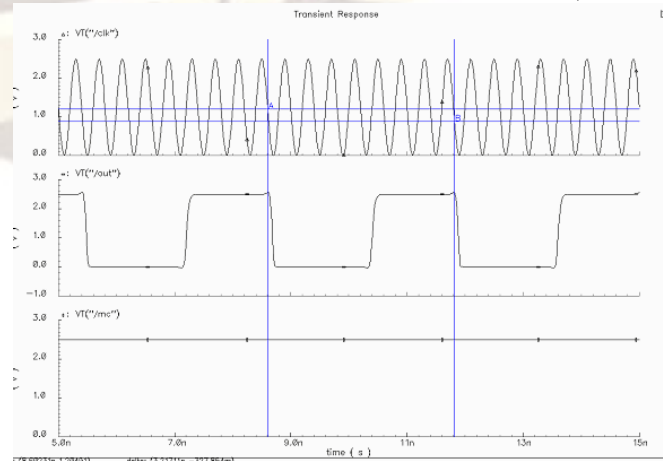

Fig 7(a)(i)Transient waveform for 8/9 Prescaler for sine wave input when MC=1
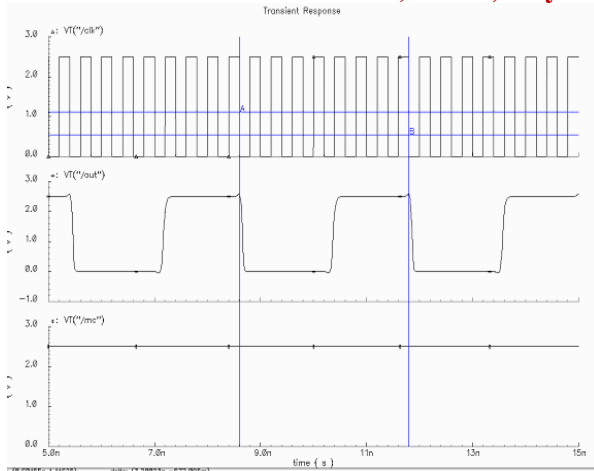
Fig 7(a)(ii)Transient waveform for 8/9 Prescaler for square wave input when MC=1
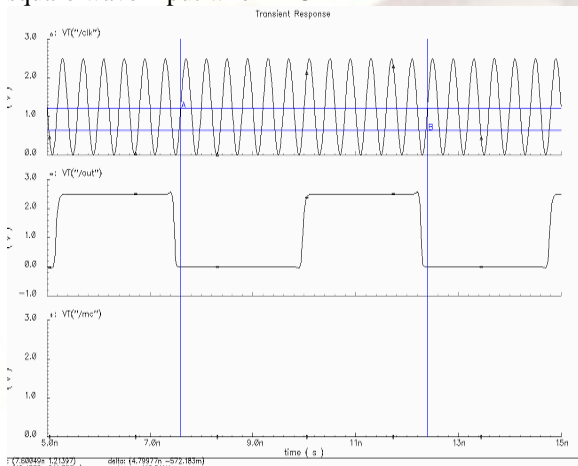

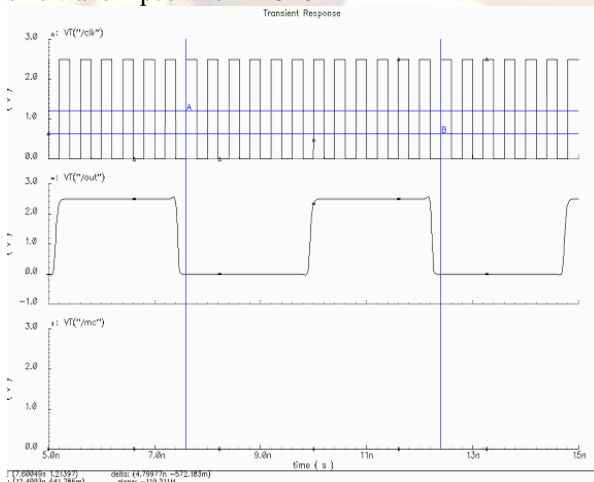Fig 7(a)(iii)Transient waveform for 8/9 Prescaler for sine wave input when MC=0

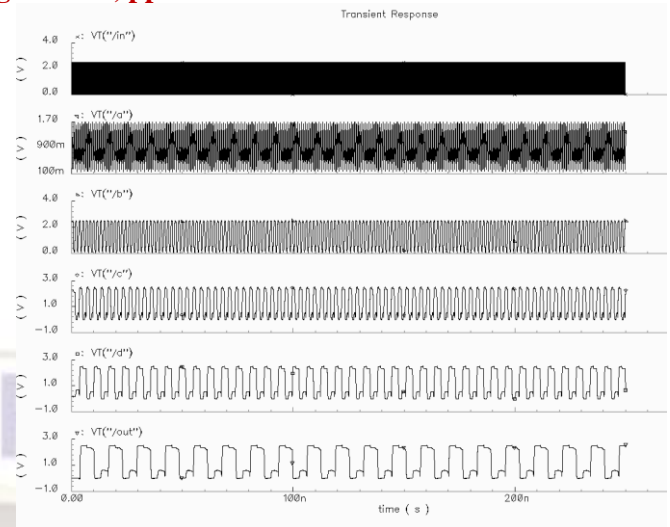Fig 7(a)(iv)Transient waveform for 8/9 Prescaler for square wave input when MC=0

Figure 8. Transient waveform of prescaler at intermediate nodes.

E. Design of a P-Counter
Referring the Table 2. We will design a 10bit P-Counter for Complete divider using TSPC logic type FF & combinational logic components & also provides high speed operation. So for this reasons a TSPC logic type loadable FF is chosen in the design. For P-CNTR a TFF that loads a data value while loading phase & its output exhibits the loaded value at same time regardless of previous state & clock signal. After data loading, The TFF should toggle the present state,ie newly loaded data, depending on the clock signal. Fig 9. Shows the complete circuit of P-CNTR

F. Design of a S-Counter
Referring the Table 2. We will design a 9bit S-Counter for complete divider using TSPC logic type FF & combinational logic components Fig 10. Shows complete circuit of S-CNTR.
G. Frequency divider simulation Results
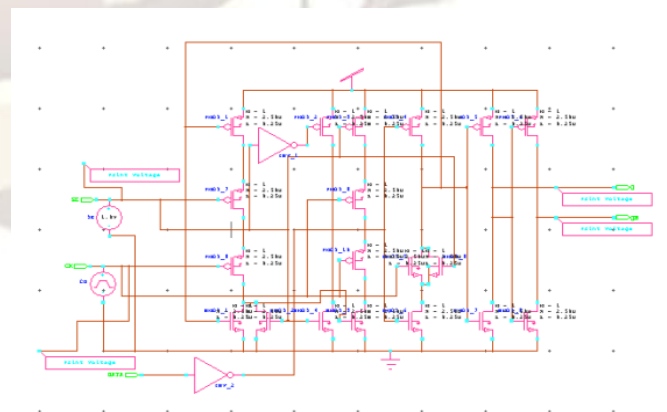Fig 11. Shows the complete divider simulation results
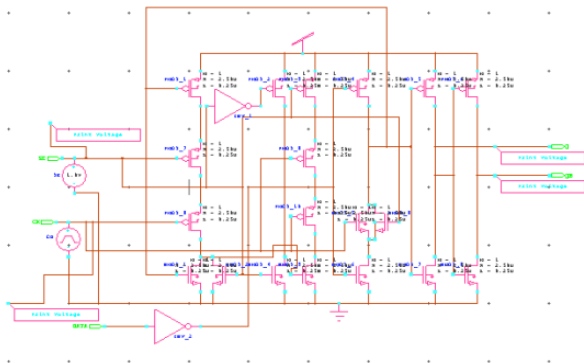

Fig 9. Schematic of P-Counter using TSPC loadable TFF
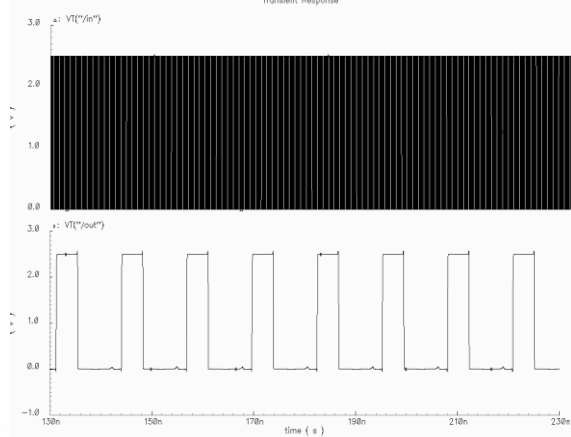
Fig 10. Schematic of S-Counter using TSPC FF

Fig 11.Complete divider circuit Transient simulation waveform

IV. Comparison of Divider with other Work

	Frequency	Division Ratio	Power	Tech code
JSSC[5]	1.75GHz	128/129 Dual	24 mW	0.7um CMOS
JSSC[11]	3GHz	32/33 Dual	27 mW	0.35um CMOS
JSSC[12]	1.4GHz-1.8GHz	511-1023	4.4 mW	0.35um CMOS
[13]	2.4GHz	256-271	28 mW	0.35um CMOS
[14]	2.4-2.48GHz	481-496	9 mW	0.18um CMOS
JSSC[15]	20-21GHz	256-263	9 mW	0.13um CMOS
This Work	1.8-2.4GHz	8/9 Dual	24mW	0.25um CMOS

Table 5. Comparison with existing designs

V. CONCLUSION

The design of our high speed fully programmable divider & Dual modulus frequency dividers implemented using TSPC FF, P-CNTR 10bit, and S-CNTR 9bit.The output frequency varies from 1.8GHz to 2.4GHz.power consumption of complete circuit is 24mW with 2.5v supply. After simulation is done we see our project requirement is fulfilled.

REFERENCES

[1] Y. Sun, S. Glisic and F. Herzel, "A Fully Differential 60 GHz Receiver Front-End with Integrated PLL in SiGe:C BiCMOS", *Proceedings of the 1st European Microwave Integrated Circuits Conference*, pp. 198 – 201, September 2006.

[2] B. Razavi, *RF Microelectronics*, New York, NY: Prentice-Hall, 1997.

[3] W. F. Egan, *Frequency Synthesis by Phase Lock*, New York, NY: Wiley 2nd edn, 2000, 142–6.

[4] S.-H. Yang, C.-H. Lee, and K.-R. Cho, "A CMOS Dual-ModulusPrescaler Based on a New Charge Sharing Free D-Flip_Flop",*Electronics Letters*, pp. 1222 – 1223, June 24th, 1993

[5] J.craninckx and M. Steyaert, "A 1.75 GHz/3-V Dual-Modulus divide by128/129 Prescaler in 0.7um CMOS," IEEE J. of solid state circuits Vol 31, No. 7,PP.890-897,July 1996.

[6] J.Yuan and C.Svenson, "High-Speed CMOS Circuit Technique,"IEEE J. Of solid state circuits, Vol.24, no.1, PP. 62-70, Feb.1989.

[7] H.Oguey and E.Vittoz, "CODYMOS frequency divider achieve low Power consumption and high frequency," Electronics letters,Vol.9, no.17.PP 386-387,Aug .23 1973.

[8] Q.Huang and R.Rogenmoser, " Speed optimization of Edge-Triggered CMOS circuits for Gigahertz single phase clocks," IEEE J. of solid state Circuits,Vol 31,no.3,PP.456-465,Mar.1996.

[9]   R.Rogenmoser, Q.Huang,and F.Piazza, "1.57GHz asynchronous and 1.4GHz dual-modulus 1.2um CMOS Prescalers,"Custom Integrated Circuits conf.,1994,Proc.IEEE 1994,PP.387-390,1994

[10] J. Yuan and C. Svensson, "High-speed CMOS circuit technique," *IEEE J. Solid-State Circuits,* vol. 24, no. 2, pp. 62–70, 1989.

[11] Salvatore Levantino, Luca Romano, Stefano Pellerano, Carlo Samori, and Andrea L. Lacaita. Phase noise in digital frequency dividers. IEEE Journal of Solid-State Circuits, 39(5):775–784, May 2004.

[12] Cicero S. Vaucher, Igor Ferencic, Matthias Locher, Sebastian Sedvallson, Urs Voegeli, and ZhenhuaWang. A family of low-power truly modular programmable dividers in standard 0.35-μm cmos technology. IEEE

Journal of Solid-State Circuits, 35(7):1039–1045, July 2000.

[13]   Sheng-Che Tseng, Chinchun Meng, Shao-Yu Li, Jen-Yi Su, and   Guo-Wei Huang.2.4 ghz   divide-by-256/271   single-ended frequency   divider in standard 0.35-μm cmos technology. In Microwave Conference Proceedings 2005 APMC Asian Pacific Conference Proceedings. Department   of Communication Engineering, NationalChiao Tung University, Hsinchu, Taiwan R.O.C., December 2005.

[14]   Rangakrishnan Srinivasan, Didem Zeliha Turker, Sang Wook Park, and Edgar Sanchez-Sinencio. A low-power frequency synthesizer with quadrature signal generation for 2.4 ghz zigbee transceiver Applications. In 2007 ISCAS International Symposium on Circuits and   Systems, pages 429–432, May 2007.

[15]   Yanping Ding and Kenneth K.O. A 21 ghz 8-modulus prescaler and a 20-ghz phase-locked loop fabricated in 130-nm cmos. IEEE Journal of Solid-State Circuits, 42(6):1240–1249, June 2007.