

## Global clock calibration for an SAR ADC interface

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### Abstract—

This paper presents the interface circuit which incorporates the technique of analog value to digital value conversion utilising a self clocking method. The architecture consists of the Globally Asynchronous and Locally Synchronous (GALS) building blocks, where the processing hardware is being realized by the set of smaller slices of similar structure, each running synchronously with independent clocks. This is used in different real-time commercial applications like digital filtering, fourier transform applications. The described architecture will allow for load-balancing depending specifically on the input load which is present in all of the used processing units. The architecture itself leads to process tolerance since it capable of detecting process variations in each and every individually present processing module and is able to finely determine the appropriate operating frequency that is finely applicable for each of the modules. Once the clock acting as a local circuit has been appropriately adjusted, it needs no further precision measurement and calculation. Also, it is efficiently free from the various changes occurring mainly because of the different and unique environmental effects. The main consideration has been laid for the efficient and the proper kind of established communication between the present modules used in the interfacing.

**Keywords—** GALS, ADC, clock skew, asynchronous interconnect, SAR

### I. INTRODUCTION

Analog to Digital Converters (ADCs) perform mainly the function of translating analog form into digital quantity form. These are preferably used for information processing, in computing [1], data transmission and various control system applications. ADCs are considered as the base components while designing for limited power requirement systems. In the paper, description of a specific type of Analog to Digital Converter is being made. The type used is primarily of the Successive Approximation Register (SAR). Additionally, there is inculcation of a global clock calibration scheme to induce the technique of Globally Asynchronous Locally Synchronous.

GALS designs work upon the concept of providing truly the possibility of an asynchronous communication in between the locally placed synchronous blocks. Each of these locally placed

synchronous blocks is capable of using an oscillator of ring type for generation of the clock. Both the

clocks at the transmitter side and the receiving part can be stopped for the asynchronous data transfer. Such a combination of the features of synchronous and the asynchronous communication leads to enhancement of decreasing the unwanted strain of the clock skew in the overall circuitry.

Clock skew factor is generally the variation in timing of one signal in a comparison to the second signal, caused due to timing or propagation delay.

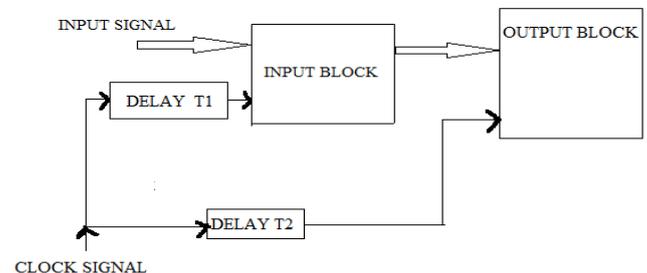


Fig. 1 Depiction of occurrence of clock skew

Fig. 1 is a depiction of occurrence of the clock skew in the shown circuit. In this circuit, clock skew factor will generally be exhibited due to the two different delays, DELAY T1 and DELAY T2. There may be basically the two types of sets of violations which exist due to presence of the clock skew in a circuit: hold type violation and set-up type violation. The former type violation will occur when the output block, for example, a flip-flop receives the clock signal after sometime than the input block flip-flop. The set-up type violation [2] is generated in case the next clock transition or edge arrives at the output block before the establishing of any new valid data to be mainly sent to the output.

### II. ARCHITECTURES

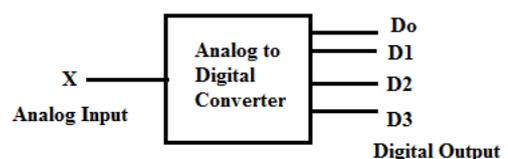


Fig. 2 A general block diagram for an ADC

Fig. 2 shows the general diagram for a simple ADC circuit. In terms of number system, the input will be fed in decimal form and output will be in binary form.

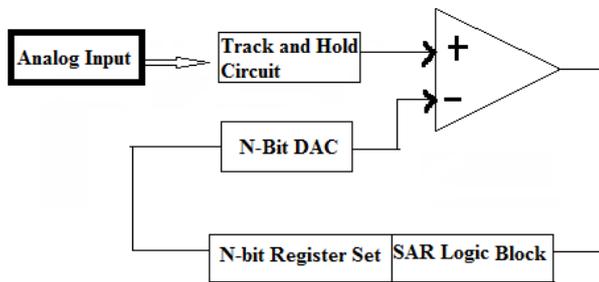


Fig. 3 An N-Bit SAR type ADC

In Fig. 3, an N-Bit SAR (Successive Approximation Register) type of the ADC (Analog to Digital Converter) is highlighted. The analog input, through the track and the hold circuit is being fed to the integrator circuit. Such a type of adjustable arrangement for the N-Bit ADC will require N number of comparison periods [1]. This kind of topology is mostly being used to allow for having reduced power dissipation, but there is the unwanted addition to pay for the disadvantage of a slow sampling rate [4]. The main benefit of an SAR type ADC is the good ratio value of speed factor to the power. Such a structure holds the benefit of having a sleek design in comparison to a flash type ADC. This makes an SAR type ADC an inexpensive device [3].

Now, for the design process and implementation of the 12-bit SAR ADC with the combination of GALS concept, the handshake signals can be utilized. Considering the handshake-based architecture of GALS, there will be a communication directly in between the synchronous components through the handshaking signals. An RTU (a receiver-transmitter unit) is incorporated [2] to each component for ensuring the proper request-acknowledgement signals based GALS handshake signaling. Each of the individual signals carrying justified and valid data is furnished with two handshake signals: request and acknowledge.

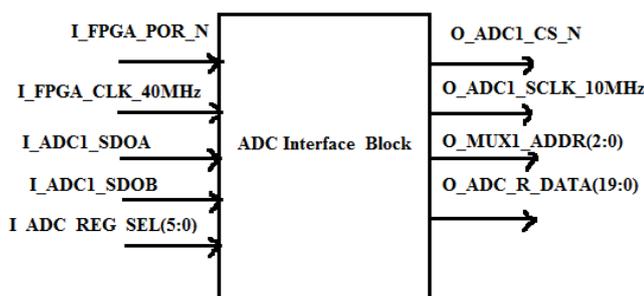


Fig. 4 Block Diagram for a 12-bit ADC interface

Fig.4 depicts the input and output signal directions for the 12-bit ADC interface. The ADC has been interfaced to the Field Programmable Gate Array (FPGA). The important functions of this ADC interface are as follows:

- It initiates the part of process of the sampling for the ADC ,
- It will generate the multiplexer select signals for analog multiplexers used,
- It carries out the implementation part of memory mapping for the registers for the ADC.

This ADC interface consists of the various sub-modules as given below:

- The ADC Interface Module,
- The ADC Multiplexer Interface Module,
- The ADC Registers Module.

The signals depicted in the block diagram for the SAR ADC interface can be described as:

- I\_FPGA\_POR\_N represents the synchronized core reset signal which is going as the input to the Interface block for the ADC,
- I\_FPGA\_CLK\_40MHz is the FPGA clock input signal to the ADC Interface block,
- I\_ADC1\_SDOA is the serial input from the A register of ADC1,
- I\_ADC1\_SDOB is the serial input data from B register of ADC1,
- I\_ADC\_REG\_SEL(5:0) is the register select input address line utilized to get data from A registers and B registers (registers A1 to A8 and registers B1 to B8) based on the select line during the read operation,
- O\_ADC1\_CS\_N is acting as the output from the ADC interface block representing the ADC Chip Select Active Low Signal,
- O\_ADC1\_SCLK\_10MHz is the output ADC Serial Clock Signal with frequency of 10 MHz,
- O\_MUX1\_ADDR(2:0) is another output from the ADC interface block for the ADC multiplexer selection signal,
- O\_ADC\_R\_DATA (19:0) is another output from the ADC interface block for the reading of the valid data required from the register module based upon address bus selection during read operation.

The amount of power variable consumed in this circuit is mainly divided into the three different parameters [1]. These are broadly classified as follows:

- Dynamic power consumption – This type occurs on the variation of the logic states of the signals.
- Short circuit type power consumption – It occurs when a direct conducting path is

developed between the main power supply portion and the ground during the switching state of the PMOS type and NMOS type transistors present in the circuit.

- Leakage or static power consumption parameter – This parameter of power consumption occurs due to electric current flow from the power rails when none of the switching activities are taking place. Two main sources of leakage in the MOS transistors include the sub-threshold leakage and the gate-oxide leakage.

As the size of MOS transistors is being reduced to very deep submicron sizes, unwanted consequences related to power consumption are arising. By causing decrease in the dimensional parameters for the used transistors, there arises a requirement to cause a linear corresponding decline in the supply voltage value in order to get imposed a restriction on the dynamic power consumption within reasonable limits.

- O\_Reg\_Sum\_En is the data valid pulse for indicating the reading process of serial data from 12-bit ADC which is converted into parallel data,
- O\_Reg\_Sw\_En is the register enable pulse.

The other signals have been described in the previous diagram. In the prescribed ADC model, there are various important parameters which are proved to be eminent for the evaluation criteria of its performance [1]. Some of these are:

- DNL – DNL stands for Differential Non-Linearity error value unit. It is uniquely the difference point value between the actual width of a step and 1 LSB's ideal value.
- INL - INL is the abbreviation for the Integral Non Linearity error point value. It highlights the maximum value for deviation of the transition point of any conversion at a particular instant to the corresponding point of transition for an ideal conversion.
- SNR – It stands for Signal to the Noise Ratio unit.
- SFDR – It stands for Spurious Free Dynamic Range.

### III. RESULTS

The results for the GALS based SAR ADC have been achieved with the Xilinx Synthesis Tool and ISE Simulator (ISim).

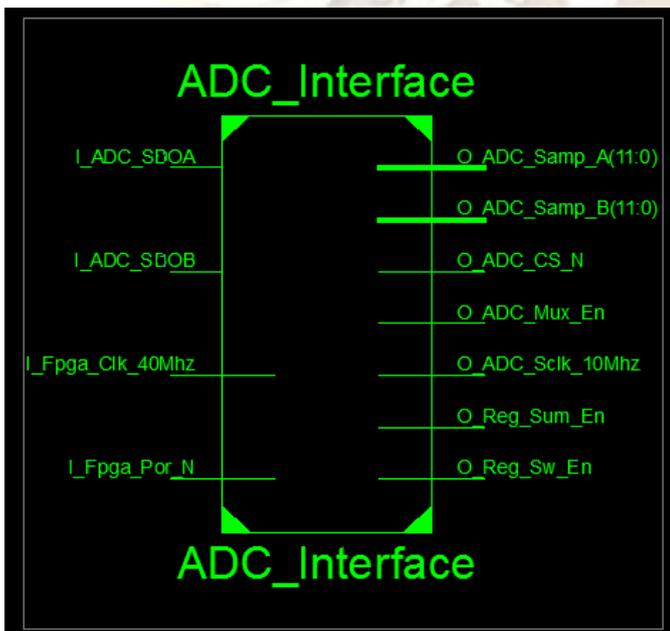


Fig. 5 Top level entity for the 12-bit ADC interface block

Fig. 5 represents the top level entity window for the 12-bit ADC interface block. The signals as in Fig. 5 are:

- O\_ADC\_SAMP\_A(11:0) is the output signal representing the serial data from ADC converted into parallel data for register A,
- O\_ADC\_SAMP\_B(11:0) is the output signal representing the serial data from ADC converted into parallel data for register B,
- O\_ADC\_Mux\_En is the Multiplexer address switching trigger pulse,

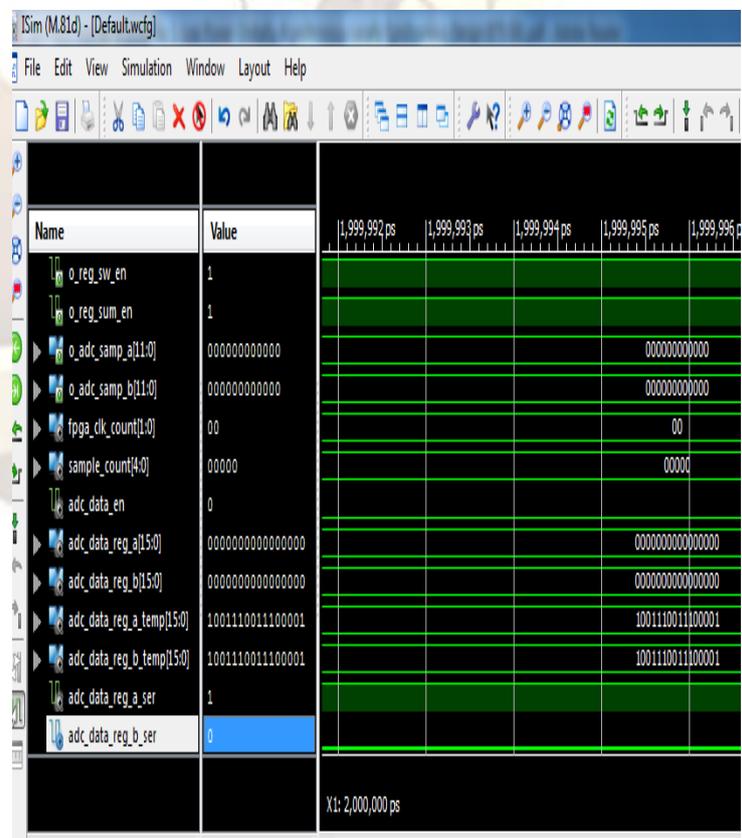


Fig. 6 Simulation results for 12-bit ADC interface block

Fig. 6 shows the simulation result window for the 12-bit ADC interface block. The design block has been brought out by synthesis using the xc3s50 device of Spartan 3 family. The output parameters achieved in terms of area overhead are as follows:

- Number of slice flip-flops – 30,
- Number of 4 input LUTs – 30,
- Number of occupied slices – 28.

The operating frequency for the ADC interface was 186.296 MHz. Considering the input signal side, an ADC circuit may be classified as the single ended signal type or a fully differential signal type [1]. In the single ended ADC, all the signals are generally referred together to a common ground portion. In the fully differential ADC, the two inputs are generally 180° angle out of phase. The Fig. 7 is showing the floorplanning window for the ADC interface.

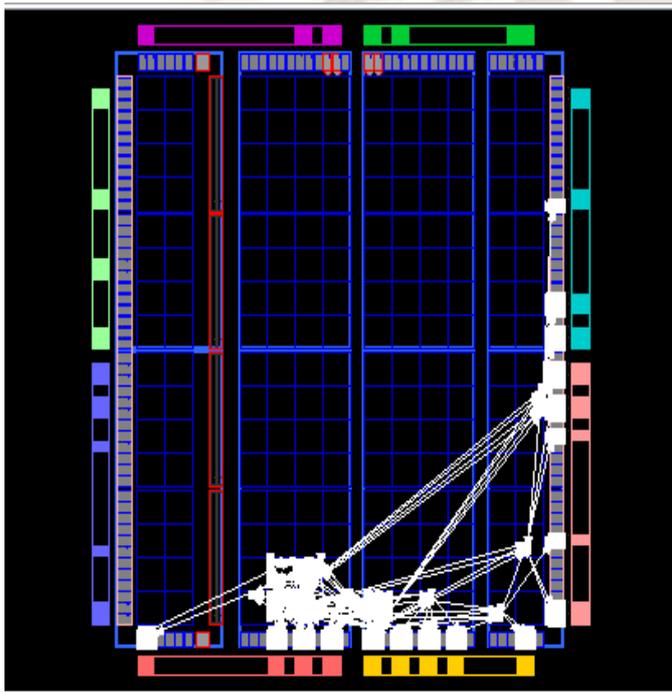


Fig. 7 Floorplanning window for ADC interface

#### IV. CONCLUSIONS

The conceptual point for the main Globally Asynchronous Locally Synchronous design circuit is the enabling of handshaking signals between the synchronously placed blocks. However, unavailability of appropriate tools and the different design methodologies for facilitating the GALS designs [2] is still present. In many cases, GALS based designs are constructed using ad hoc type methods. For these methods, the synchronous parts are encapsulated using some wrapper concept. The

communication process is done either by handshake principles or by bounded FIFOs concept.

An SAR type ADC is suitable for the medium type resolution effect with high speed ranging from Kilo Samples in one Second (kSPS) to Mega Samples per Second (MSPS) [3]. The SAR type of ADC interface implemented allows the inclusion of GALS methodology. Also, the inculcation of the self clocking technique has been largely indulged in the process of implementation of the SAR ADC. So, there has been prevention of metastability in the circuit. A metastable state can also be synonym to a quasi-stable state.

#### ACKNOWLEDGMENT

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