A low noise and low power 3-GHz 64~127 Multi-Modulus Frequency Divider implementation using   BiCMOS technology

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ABSTRACT

This paper presents implementation of a high speed, low noise and low power frequency divider based on current mode logic and cascade connection of divide-by-2/3 cells for high division range. The proposed divider is optimized for high frequency and low power operation. Integration of the proposed divider in a frequency synthesizer is an attractive option for the ultra-low power carrier signal generation in coherent wired and wireless communication systems.

A prototype has been implemented in 0.24μm SiGe-BiCMOS technology. The operating frequency is 3 GHz; the divide ratio is 64/127 with step of 1 with 2.5V power supply and current consumption is 1.5mA occupying $0.06mm^2$ chip areas. The modulus may be integer or fractional.

Keywords – **Frequency Divider, Multi-Modulus, Prescaler, Phase Switching, 2/3 Cell, Frequency Synthesizers, Wireless Transceivers, BiCMOS, Current Mode Logic.**

I.   INTRODUCTION

Frequency dividers are critical components for frequency translation and channel selection in wireless transceivers used in frequency synthesizers. Divider design is a challenging task due to the stringent requirements imposed by RF systems. Multi-modulus frequency divider plays an important role in frequency synthesizers for wireless communications. It operates at the highest frequency and must be controllable over a wider range in order to synthesize the desired output frequencies, which is narrow channel spaced. HIGH-SPEED frequency dividers are critical in a variety of applications from frequency syntheses in wireless communications to broadband optical fiber communication systems. These applications require high speed, low power, high sensitivity, and monolithic integration. To date, the highest operating frequencies have been achieved with bipolar and III–V technologies though their power consumptions are high. Compared to the bipolar and III–V dividers, CMOS dividers usually operate at lower frequencies. To increase the operating frequency at a given power consumption, several techniques are used, such as injection locking, dynamic circuit, and improved Miller dividers. Compared with them, a static divider has a much wider operating range and moderate operating frequency and power consumption. CMOS static frequency dividers operating around 20 GHz have recently been reported, but the power consumption is too high. In this paper, by optimizing the transistors size, a power efficient 64:127 CMOS static frequency divider is presented. The power consumption of the first 2:3 stage is less than 15% of other bulk CMOS static frequency dividers at the same frequency. The tradeoff between the speed and power consumption is discussed in detail.

1.BiCMOS Process Technology

BiCMOS technology is a combination of **Bi**polar and **CMOS** technology. CMOS technology offers less power dissipation, smaller noise margins, and higher packing density. Bipolar technology, on the other hand, ensures high switching and I/O speed and good noise performance. It follows that BiCMOS technology accomplishes both improved speed over CMOS and lower power dissipation than bipolar technology. The main drawback of BiCMOS technology is the higher costs due to the added process complexity. Impurity profiles have to be optimized to both NPN and CMOS issues. This greater process complexity results in a cost increase compared to conventional CMOS technology.

The primary approach to realize high performance BiCMOS devices is the addition of bipolar process steps to a baseline CMOS process

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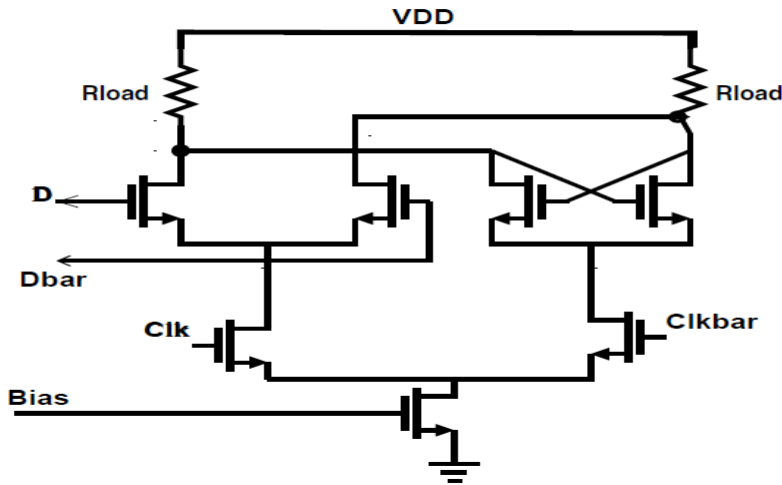
2. Latch implemented by CML logic

FIGURE 1: Current-Mode D-Latch.

The conventional CML Flip-Flop of Figure 4.4 works similar to a latched comparator with the positive feedback supplementing the gain of the differential pair. The latch mode time constant in the positive feedback phase has been derived using a linearized model in The result derived indicates that the transient response of the latch is represented by the solution

$$\Delta V = \Delta V_o e^{(A_v - 1)t/\tau}$$

.

So if change Vo is small, the latch time can be larger than the allowed time to latch (half the clock period) causing metastability. Further, low voltage swings are more susceptible to noise and mismatch. Although not very critical in the case of frequency dividers, this would be relevant for the design of oscillator delay stages. The upper bound on voltage swings (V_{sw}) is established by biasing conditions of differential pair transistors. When one differential delay stage drives a similar stage, then the differential pair transistor with a high input voltage requires a large enough V_{DS} to remain in saturation
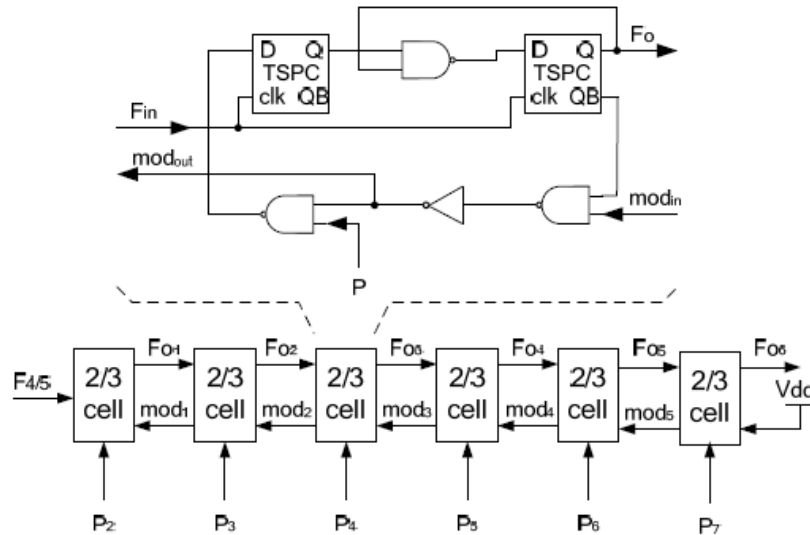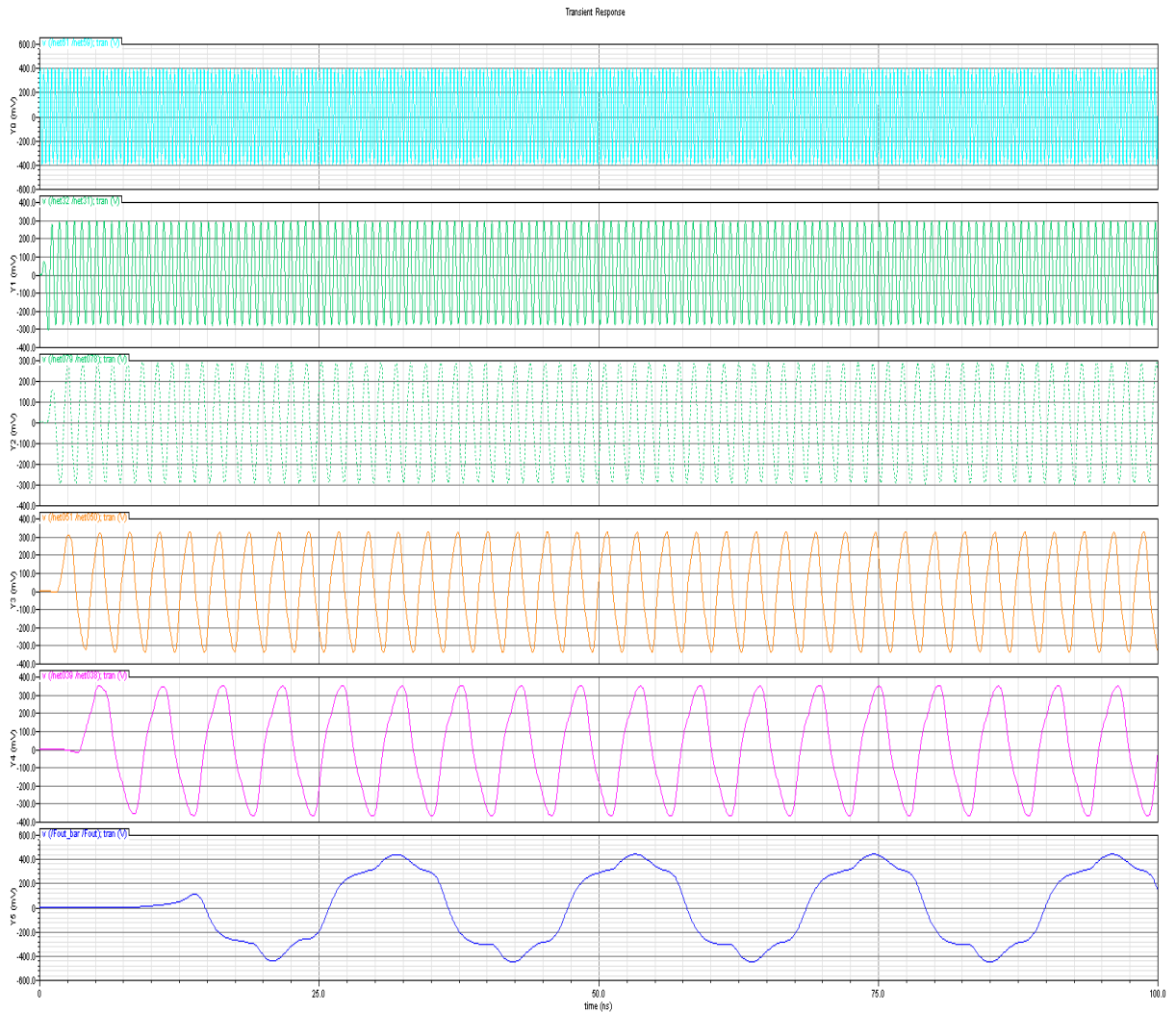
3. Divide-by-64~127 Divider

Fig.5.4. Circuit diagram of the divide-by-64~127 frequency divider

The divide-by-64~127 frequency divider is implemented in cascade connection of divide-by-2/3 cells architecture [5]. The circuit diagram of the divide-by-64~127 frequency divider is shown in Fig.5. It is constructed using cascade connection of six divide-by-2/3 cells. Each cell contains one control bit in which the division ratio can be selected. The detail implementation of the divide-by-2/3 cell is also shown in Fig.5. When the control bit P is set to high, the division ratio is three, and the division ratio becomes two when the control bit P is set to low. Thus, the overall division ratio is continuingly programmable ranged from 64 to127. Since the input frequency of the divide-by-64~127 divider has been scaled down by 4/5, in order to lower the power consumption, the D-Flip-Flops are implemented in true single phase clock D-Flip-Flop (TSPC), and the control logics are implemented in CMOS logic. The divide-by-64~127 divider require rail-to-rail input signal. Thus, a differential to single end buffer is used the differential output of F4/5 to rail-to-rail CMOS Logic level.

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4.Phase noise reduction in divider

Low power consumption and high performance are often contradictory requirements and this constitutes a design tradeoff. In particular, achieving a low phase noise in the phase locked loop (PLL) of frequency synthesizers is one of the most stringent requirements. Normally, the current trend towards lower power consumption degrades phase noise performance. Therefore, we need to define an appropriate way of optimizing towards low power consumption without sacrificing the phase noise performance of the PLL. To comprehend in depth this design trade-off, one should identify the internal phase noise mechanisms intrinsic to each block constituting a PLL. We choose the frequency dividers (FD) as the focus of this work. The phase noise generated by a FD affects the synthesizer noise performance within the PLL band, especially if a high division factor is used. Additionally, the digital FD is in general responsible for a significant portion of the total power consumption of the PLL. However, a decrease in the power consumption of the divider degrades its phase noise performance. Therefore, we need, first, to identify the fundamental tradeoff between noise and power consumption in this particular block and, second, to have a robust and reliable way of simulating phase noise of "sample and hold" based circuits such as a digital FD.
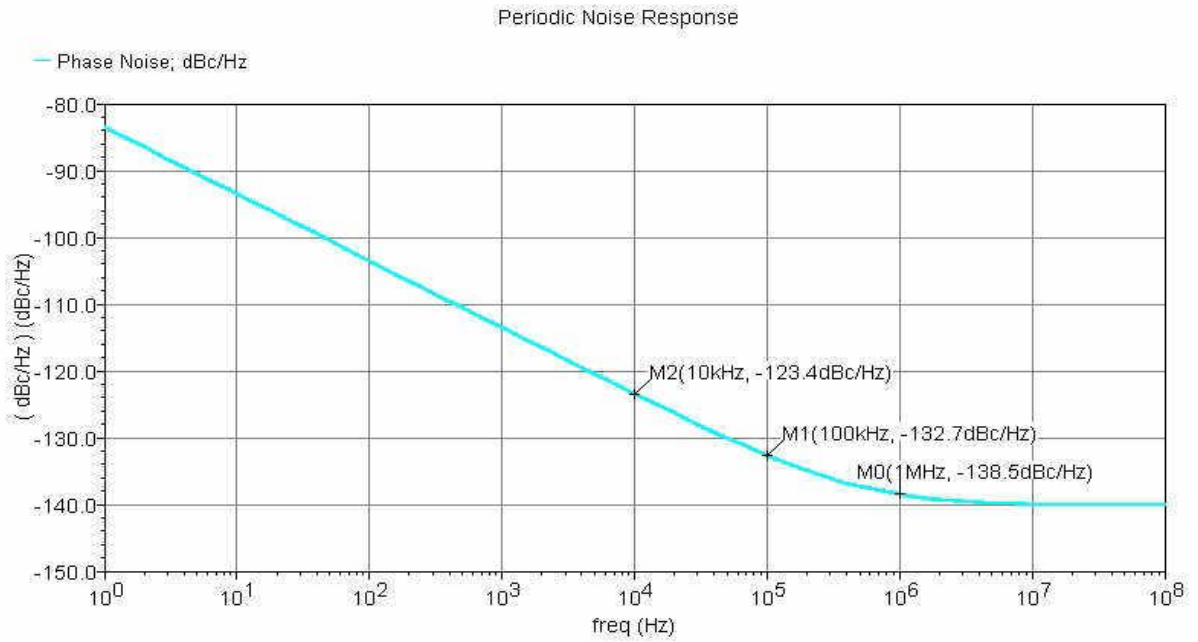
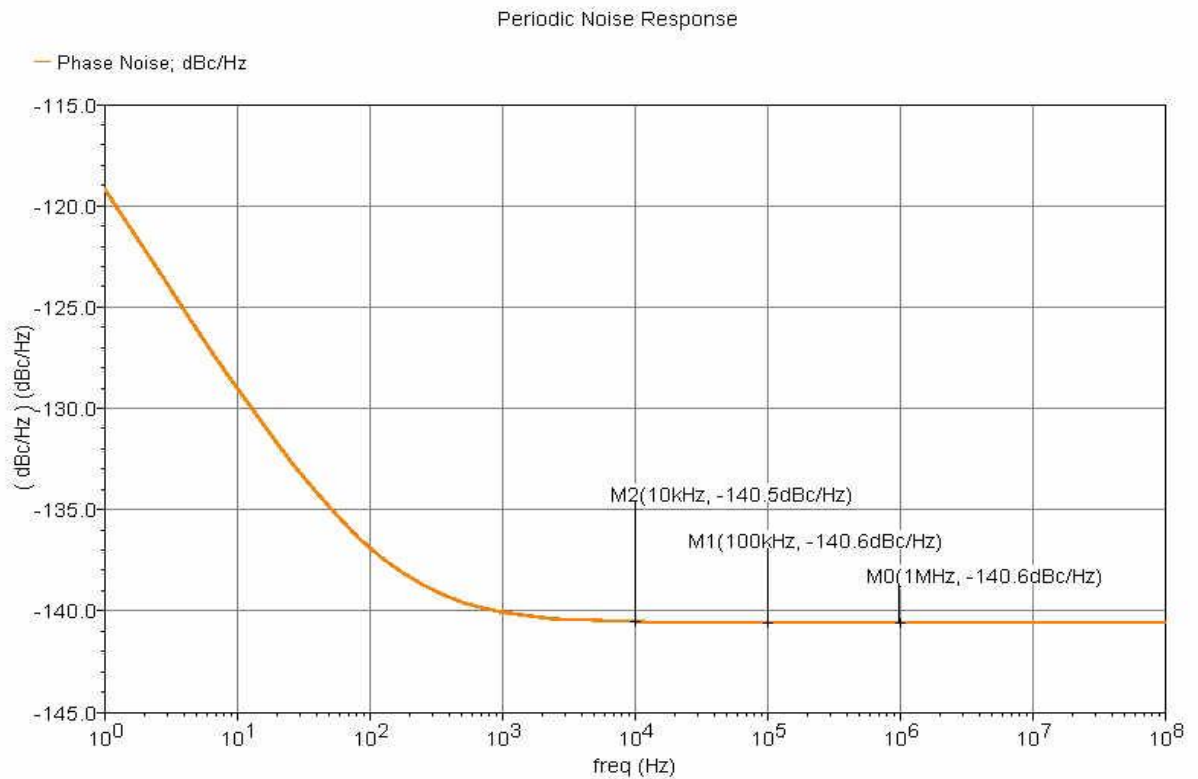Fig: phase noise simulation of Fdimplemented using bicmos technology

Fig: phase noise simulation of Fdimplemented using cmos technology

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PERFORMANCE SUMMARY OF THE MULTI-MODULUS FREQUENCY DIVIDER

Parameters	Symbol	performance	
Technology	-	0.24um Bicmos technology	0.24um cmos technology
Division Ratio	-	2~3	2~3
Supply Voltagr	vdd	2.5v	2.5v
Supply Current	idd	1.5mA	2mA
Power consumption	-	3.824mw	4.6mw
Maximum Operating Frequency	$F_{in\ MAX}$	3GHZ	3GHZ
Phase Noise@1kHz	P_n1khz	-140.5dBc/Hz	-123.4 dBc/Hz
Phase Noise@10kHz	P_n10khz	-140.6dBc/Hz	-132.7 dBc/Hz
Phase Noise@1MHz	P_n1Mhz	140.6dBc/Hz	-138.5 dBc/Hz

TABLE 1 COMPARISION OF CMOS AND BICMOS PROPERTIES

CONCLUSION:

A 3GHz multi-modulus frequency divider based on current mode logic has been demonstrated in 0.24μm SiGe BiCMOS technology. It is optimized for high frequency and low power operation both on architecture level and circuits implementations. The division ratio is ranged from 64 to 127 continually with step of 1, with the current consumption of 1.5mA from 2.5V supply voltage. the dedicated design approach and the BiCMOS SiGe process capabilities led to a good trade-off between maximum input frequency, input sensitivity, noise floor, power consumption, division ratios and die size compared with the current available high-frequency dividers.

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