Design Of An Fault Exposure And Data Resurgence Architecture For Motion Estimation Testing Applications

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Abstract—The critical role of motion estimation (ME) in a video coder, testing such a module is of priority concern. While focusing on the testing of ME in a video coding system, this work presents an error detection and data recovery (EDDR) design, based on the residue-and quotient (RQ) code, to embed into ME for video coding testing applications. An error in processing elements (PEs), i.e. key components of a ME, can be detected and recovered effectively by using the proposed EDDR design. Experimental results indicate that the proposed EDDR design for ME testing can detect errors and recover data with an acceptable area overhead and timing penalty. Importantly, the proposed EDDR design performs satisfactorily in terms of throughput and reliability for ME testing applications. While DFT approaches enhance the testability of circuits, advances in submicron technology and resulting increases in the complexity of electronic circuits and systems have meant that built-in self-test (BIST) schemes have rapidly become necessary in the digital world. BIST for the ME does not expensive test equipment, ultimately lowering test costs. Thus, extended schemes of BIST referred to as built-in self-diagnosis and built-in self-correction have been developed recently.

Keywords –motion estimation, error detection and data recovery, residue-and quotient code, design for testability, circuit under test.

I. INTRODUCTION

Advances in semiconductors, digital signal processing, and communication technologies have made multimedia applications more flexible and reliable. A good example is the H.264 video standard, also known as MPEG-4 Part 10 Advanced Video Coding, which is widely regarded as the next generation video compression standard Video compression is necessary in a wide range of applications to reduce the total data amount required for transmitting or storing video data. Among the coding systems, a ME is of priority concern in exploiting the temporal redundancy between successive frames, yet also the most time consuming aspect of coding. Additionally, while performing up to 60%–90% of the computations encountered in the entire coding system, a ME is widely regarded as the most computationally intensive of a video coding system. AME generally consists of PEs with a size of 4x4. However, accelerating the computation speed depends on a large PE array, especially in high-resolution devices with a large search range such as HDTV. Additionally, the visual quality and peak signal-to-noise ratio (PSNR) at a given bit rate are influenced if an error occurred in ME process. A testable design is thus increasingly important to ensure the reliability of numerous PEs in a ME. Moreover, although the advance of VLSI technologies facilitate the integration of a large number of PEs of aME into a chip, the logic-per-pin ratio is subsequently increased, thus decreasing significantly the efficiency of logic testing on the chip. As a commercial chip, it is absolutely necessary for the ME to introduce design for testability (DFT) DFT focuses on increasing the ease of device testing, thus guaranteeing high reliability of a system. DFT methods rely on reconfiguration of a circuit under test (CUT) to improve testability. While DFT approaches enhance the testability of circuits, advances in sub-micron technology and resulting increases in the complexity of electronic circuits and systems have meant that built-in self-test (BIST) schemes have rapidly become necessary in the digital world.

DISADVANTAGES OF EXISTING:

- Poor performance in terms of high accuracy design for real time applications in DCT core on FPGA implementation.
- Does not achieve in terms of implementation on CMOS technology DCT core.

ADVANTAGES OF PROPOSED:

- To fit for Real Time application in DCT Core.

II. PROPOSED SYSTEM

The conceptual view of the proposed EDDR scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) in Fig. utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors.

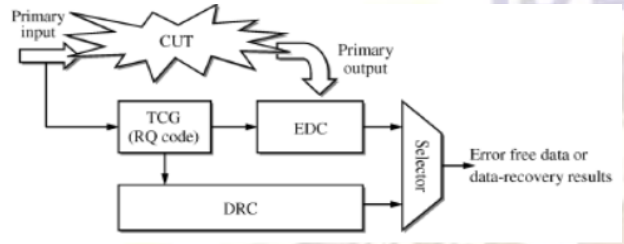

Fig.1. Proposed EDDR architecture

DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results. Importantly, an array-based computing structure, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDDR scheme to detect errors and recover the corresponding data.

ADAVANTAGES IN PROPOSED SYSTEM

1. More reliability.
2. Less number of gate counts.

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However, accelerating the computation speed depends on a large PE array, especially in high-resolution devices with a large search range such as HDTV. Additionally, the visual quality and peak signal-to-noise ratio (PSNR) at a given bit rate are influenced if an error occurred in ME process. A testable design is thus increasingly important to ensure the reliability of numerous PEs in a ME. Moreover, although the advance of VLSI technologies facilitate the integration of a large number of PEs of a ME into a chip, the logic-per-pin ratio is subsequently increased, thus decreasing significantly the efficiency of logic testing on the chip. As a commercial chip, it is absolutely necessary for the ME to introduce design for testability (DFT). DFT focuses on increasing the ease of device testing, thus guaranteeing high reliability of a system. DFT methods rely on reconfiguration of a circuit under test (CUT) to improve testability. While DFT approaches enhance the testability of circuits, advances in sub-micron technology and resulting increases in the complexity of electronic circuits and systems have meant that built-in self-test (BIST) schemes have rapidly become necessary in the digital world. BIST for the ME does not expensive test equipment, ultimately lowering test costs. Moreover, BIST can generate test simulations and analyze test responses without outside support, subsequently streamlining the testing and diagnosis of digital systems. However, increasingly complex density of circuitry requires that the built-in testing approach not only detect faults but also specify their locations for error correcting. Thus, extended schemes of BIST referred to as built-in self-diagnosis and built-in self-correction have been developed recently. While the extended BIST schemes generally focus on memory circuit, testing-related issues of video coding have seldom been addressed. Thus, exploring the feasibility of an embedded testing approach to detect errors and recover data of a ME is of worthwhile interest. Additionally, the reliability issue of numerous PEs in a ME can be improved by enhancing the capabilities of concurrent error detection (CED). The CED approach can detect errors through conflicting and undesired results generated from operations on the same operands. CED can also test the circuit at full operating speed without interrupting a system. Thus, based on the CED concept, this work develops a novel EDDR architecture based on the RQ code to detect errors and recovery data in PEs of a ME and, in doing so, further guarantee the excellent reliability for video coding testing applications. EXPERTS from ITU-T Video Coding Experts Group (VCEG) and ISO/IEC Moving Picture Experts Group (MPEG) formed the Joint Video Team (JVT) in 2001 to develop a new video coding standard, H.264/AVC. Compared with MPEG-4 , H.263, and MPEG-2, the new standard can achieve 39%, 49%, and 64% of bit-rate reduction, respectively. The functional blocks of H.264/AVC, as well as their features, are shown in Fig. 1. Like previous standards, H.264/AVC still uses motion compensated transform coding. The improvement in coding performance comes mainly from the prediction part. Motion estimation (ME) at quarter-pixel accuracy with variable block sizes and multiple reference frames greatly reduces the prediction errors. Even if inter-frame prediction cannot find a good match, intra-prediction will make it up instead of directly coding the texture as before. The reference software of H.264/AVC, JM, adopts full search for both Motion Estimation (ME) and intra-prediction. The instruction profile of the reference software on Sun Blade 1000 with Ultra SPARC III 1 GHz CPU shows that real-time encoding of CIF 30 Hz video requires 314 994 million instructions per second and memory access of 471 299 Mbytes/s. ME is the most computationally intensive part. In H.264/AVC, although there are seven kinds of block size (16x16, 16x8, 8 x 16, 8x8, 8x4, 4x8, 4x4) for Motion Compensation (MC), the complexity of ME in the reference software is not seven times of that for one block size. The search range centers of the seven kinds of block size are all the same, so that the sum of absolute difference (SAD) of a 4x4 block can be reused for the SAD calculation of larger blocks. In this way, variable block size ME does not lead to much increase in computation. Intra-prediction allows four modes for 16x 16 blocks and nine modes for 4x4 blocks. Its complexity can be estimated as the SAD calculation of 13 16x16 blocks plus extra operations for interpolation, which are relatively small compared with ME. As for the multiple reference frames ME, it contributes to the heaviest computational load. The required operations are proportional to the number of searched frames. Nevertheless, the decrease in prediction residues depends on the nature of sequences. Sometimes the prediction gain by searching more reference frames is very significant, but usually a lot of computation is wasted without any benefits. With the growing emergence of mobile communications, and the growing interest in providing multimedia services over wireless channels, providing a means of sending video data over wireless channels has become an increasingly important task. Because of the high bandwidth required to transmit raw video data over band-limited wireless channels, some form of compression is typically used to reduce the overall bandwidth. For example, 56x256 grayscale images at 30 fm/sec require bitrates over 15 Mbps. Certainly this is not acceptable for wireless transmission of video, provided that typical radio transceivers deliver only up to a few Mbps of raw data. Current standard compression techniques provide bitrates as low as a few Kbps up to over 1 Mbps through a combination of intraframe and interframe coding (MPEG, H.263, H.261, etc.), or intraframe-only coding (JPEG). Because of the additional compression achievable using interframe coding (a form of temporal coding of consecutive frames) allowing for bitrates < 100 Kbps, this is becoming the better choice for transmission of video over wireless. With the emergence of the ISO MPEG-4 and the ITU H.263+ standards, the trends are certainly toward motion video coding for wireless applications. Another technology trend is providing system on a chip solutions for video and image coding. With the growing interest of wireless video, and the trend toward small formfactored devices with limited battery power, the need for size reduction with reduced power consumption is of prime importance. Multi-chip sets are becoming obsolete as technology improves and deep sub-micron feature size is achieved. This allows for more features to be implemented on a single chip, reducing the overall area of the intended system, and reducing overall power consumption by eliminating the need of chip-to-chip I/O transfers. It is now common to find single-chip solutions of entire video coding algorithms such as MPEG-4 and H.263+ with embedded RISC cores. It is also feasible to implement complete capture-compress systems on a single chip. With the emergence of CMOS sensor pixel array technology, digital cameras are now available which capture 30 frames/ sec CIF images in monochrome and color, consuming less than 100 mW. The trend now is implementing both capture and compression on a single ASIC with mixed signal design. This allows for image capture, digitization, color conversion, DCT, motion estimation, and quantization/variable length coding to be done all in a single chip, resulting in a compressed video bitstream output . H.264/MPEG-4 AVC is the newest international video coding standard of the ITU-T Video Coding Experts Group and the ISO/IEC Moving Picture Experts Group. It represents the state-of-the-art video compression technology, and addresses the full range of video applications including low bit-rate wireless video applications, standard-definition & high-definition broadcast television, and video streaming over the Internet. In terms of compression performance, it provides more than 50% bit-rate savings for equivalent video quality relative to the performance of MPEG-2 video coding standard. To achieve such a high coding efficiency, AVC includes many new features such as variable block size motion compensation, quarter-pixel accuracy motion compensation, and multiple reference frame motion compensation. In the variable blocksize motion compensation, AVC supports luma block-sizes of 16x16, 16x8, 8x16, and 8x8 in the inter-frame prediction. In case 8x8 is chosen, further smaller block-sizes of 8x4, 4x8, and 4x4 can be used. In the multiple reference frame motion compensation, a signal block with uni-prediction in P slices is predicted from one reference picture out of a large number of decoded pictures. And similarly, a motion compensated bi-prediction block in B slices is predicted from two reference pictures both can be chosen out of their candidate reference picture lists. A scenario of Multiple Reference Frame Motion Estimation is shown in Figure 1. It is an effective technique to improve the coding efficiency. However, MRF-ME dramatically increases the computational complexity of the encoders because the Motion Estimation (ME) process needs to be performed for each of the reference frames. Considering motion estimation is the most computationally intensive functional block in the video codec, this increased complexity penalizes the benefit gained from the better coding efficiency, and thus may restrict its applicability. The reference software of AVC JM 8.6 performs the motion estimation for all block-sizes across all reference frames in the encoder. A fast algorithm is proposed to speed-up the MRF-ME by considering the different sub-pixel sampling position of each block, and performing ME on the selected reference frames with similarly sampled contents. several heuristics are used to decide whether it is necessary to search more than the most recent reference frame, and hence reduce the computations. a fast multiframe motion estimation algorithm based on Motion Vector (MV) reusing similar to our basic ideas described as independently proposed. The motion vector composition is done by choosing a dominant MV, and 5~7 checking points are needed to refine the composed MV. The proposed multiframe motion estimation method in this paper differs from in using a weighted average for motion composition, and there is no further refinement needed.

III. COMPRESSION

Wireless video transmission presents several problems to the design of a video coding system. First of all, some form of compression is needed for a bandwidth-limited system. Often, in a network environment for example, a certain amount of bandwidth is allocated to an individual user. Under these circumstances, a certain amount of "headroom" is allowed for each of the signal processing components based on user needs. The headroom for each of these components is usually not fixed, and is based on restricted channel capacity and networking protocols needed to service the needs of its users. Given this, and the fact that video requires the highest bandwidth in a multimedia environment, the ability to vary the compression rate in response to varying available bandwidth is desirable. To achieve a certain bandwidth requirement, some combination of the following is required:

Interframe compression: the idea behind inter fame compression is that consecutive frames tend to have a high degree of temporal redundancy, and that the difference frame between the two would have a large number of pixel values near zero. So the result is a much lower energy frame than the originals, and thus more amenable to compression. Figure 1-1 shows the strategy for interframe coding. Because of the complexity and power increase in implementing motion estimation for interframe coding (requiring more than 50% of the total number of computations per frame), the cost value is high for interframe coding . Algorithms using interframe coding are often termed video coding algorithm.

Intraframe compression: this implies spatial redundancy reduction, and is applied on a frame by frame basis. For situations where bandwidth is limited, this method allows for great flexibility in changing the compression to achieve a certain bandwidth. The key component in intraframe compression is the quantization, which is applied after an image transform. Because of the spatial correlation present after performing a transform (DCT or wavelet for example), quantization can be applied by distributing the bits based on visual importance of a spatially correlated image. This method of compression has the added advantage, that the compression can be easily varied based on available bandwidth on a frame by frame basis.

IV. MOTION ESTIMATION AND COMPENSATION

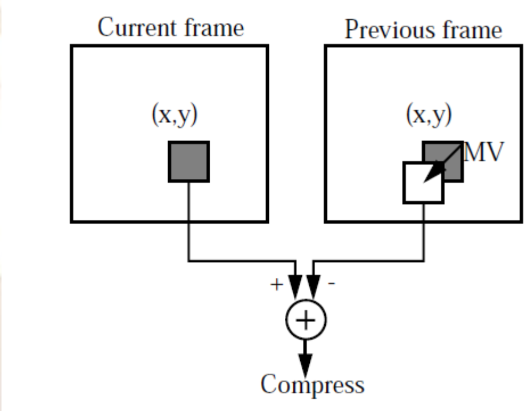

Fig.2. Motion Estimation and Compensation.

Frame rate reduction: Another form of compression is reducing the frame rate of coded images. This results in a linear (1/N factor) reduction in the bit rate, where N is the current frame rate divided by the reduced frame rate. The resulting decoded frames at the decoder are also reduced by 1/N.

Frame resolution reduction: The final form of compression is reducing the frame resolution. This results in a quadratic (1/N2) reduction in the bit rate, assuming uniform reduction in the horizontal and vertical directions. The encoder and decoder must have the ability to process variable resolution frames, thus making the design more complicated.

METHODOLOGIES

Coding approaches such as parity code, Berger code, and residue code have been considered for design applications to detect circuit errors. Residue code is generally separable arithmetic codes by estimating a residue for data and appending it to data. Error detection logic for operations is typically derived by a separate residue code, making the detection logic is simple and easily implemented. For instance, assume that N denotes an integer, N1 and N2 represent data words, and m refers to the modulus. A separate residue code of interest is one in which N is coded as a pair. N m is the residue N of m modulo . Error detection logic for operations is typically derived using a separate residue code such that detection logic is simply and easily implemented. However, only a bit error can be detected based on the residue code. Additionally, an error cannot be recovered effectively by using the residue codes. Therefore, this work presents a quotient code, which is derived from the residue code, to assist the residue code in detecting multiple errors and recovering errors. In order to simplify the complexity of circuit design, the implementation of the module is generally dependent on the addition operation. Additionally, based on the concept of residue code, the following definitions shown can be applied to generate the RQ code for circuit design. The corresponding circuit design of the RQCG is easily realized by using the simple adders (ADDs). Namely, the RQ code can be generated with a low complexity and little hardware cost.

DATA RECOVERY CIRCUIT

In this module will be generate error free output by quotient multiply with constant value (64) and add with reminder code. During data recovery, the circuit DRC plays a significant role in recovering RQ code from TCG. Notably, the proposed EDDR design executes the error detection and data recovery operations simultaneously. Additionally, error-free data from the tested PEi or data recovery that results from DRC is selected by a multiplexer (MUX) to pass to the next specific PEi+1for subsequent testing. Error concealment in video is intended to recover the loss due to channel noise, e.g., bit-errors in a noisy channel and cell-loss in an ATM network, by utilizing available picture information. The error concealment techniques can be categorized into two classes according to the roles that the encoder and the decoder play in the underlying approaches. Forward error concealment includes methods that add redundancy in the source to enhance error resilience of the coded bit streams. For example, I-picture motion vectors were introduced in MPEG-4 to improve the error concealment. However, a syntax change is required in this scheme. In contrast to this approach, error concealment by post-processing refers to operations at the decoder to recover the damaged images based on image and video characteristics.

In this way, no syntax is needed to support the recovery of missing data. we have only discussed the case in which one frame has been damaged and we wish to recover damaged blocks using information that is already contained in the bit-stream. The temporal domain techniques that we have considered rely on information in the previous frame to perform the reconstruction. However, if the previous frame is heavily damaged, the prediction of the next frame may also be affected. For this reason, we must consider making the prediction before the errors have occurred. Obviously, if one frame has been heavily damaged, but the frame before that has not been damaged, it makes senses to investigate how the motion vectors can be extrapolated to obtain a reasonable prediction from a past reference frame. Following this notion, we have essentially divided the problem of error concealment into two parts.

The first part assumes that the previous frames are intact or are close to intact. This will always be the case for low BER and short error bursts. Furthermore, a localized solution such as the techniques presented in the previous subsection will usually perform well. However, if the BER is high and/or the burst length is long, the impact of a damaged frame can propagate, hence the problem is more global and seems to require a more advanced solution, i.e., one which considers the impact over multiple frames.

In the following, we propose an approach that considers making predictions from a past reference frame, which has not been damaged. The estimated motion information which differs from the actual one may be recovered from that of neighbor blocks. Because a moving object in an image sequence is larger than the block size of a minimal block in many occasions, motion information of neighbor blocks are usually the same as, or approximate to, current blocks. The concept of global motion is discussed in many researches on motion estimation or related interests. In method which reconstructs the frame with the aid of neighbor motion vector is successfully applied to motion estimation. Thus, an error signal “1” is generated from EDC and sent to mux in order to select the recovery results from DRC.

V. MODULE DIAGRAM

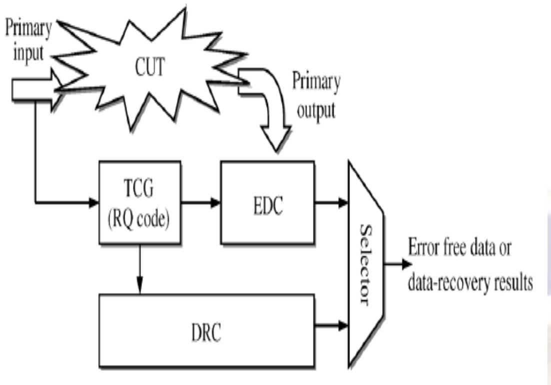

Fig. 3. Conceptual view of the proposed EDDR architecture

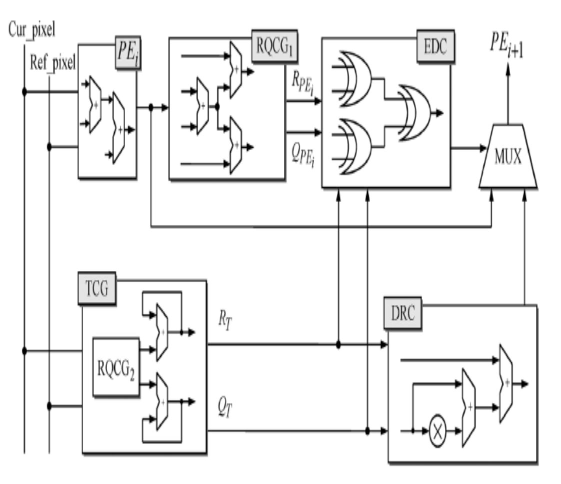

Fig. 4. A specific PEi testing process of the proposed EDDR architecture.

ACCUMULATOR

In this module consists flipflop act as a accumulator. We can store a bit of data. Flip-flop" is the common name given to two-state devices which offer basic memory for sequential logic operations. Flip-flops are heavily used for digital data storage and transfer and are commonly used in banks called "registers" for the storage of binary numerical data. There are some circuits that are not quite as straight forward as the gate circuits we have discussed in earlier lessons. However, you still need to learn about circuits that can store and remember information. They're the kind of circuits that are used in computers to store program information RAM memory.

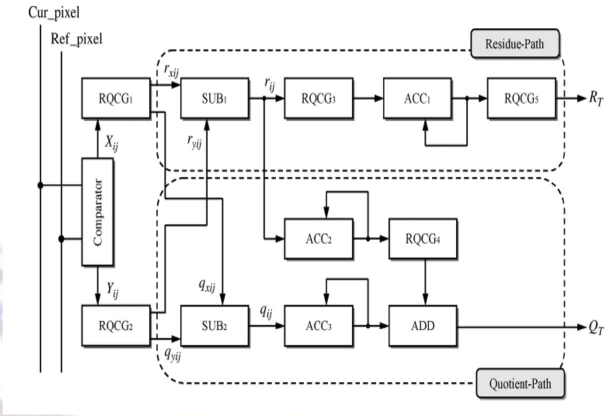

Fig. 5. Circuit design of the TCG

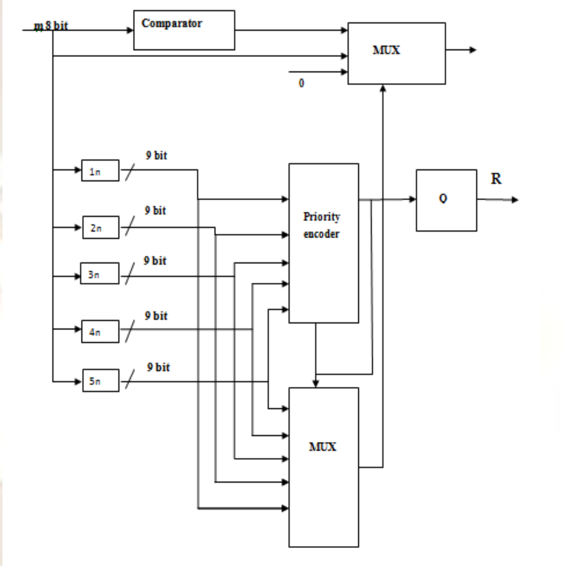

FIG-6 M MOD N OPERATION

VI. ERROR DETECTION ARCHITECTURE

Our proposed EDDR scheme, which comprises two major circuit designs, i.e. error detection circuit (EDC) and data recovery circuit (DRC), to detect errors and recover the corresponding data in a specific CUT. The test code generator (TCG) in utilizes the concepts of RQ code to generate the corresponding test codes for error detection and data recovery. In other words, the test codes from TCG and the primary output from CUT are delivered to EDC to determine whether the CUT has errors. DRC is in charge of recovering data from TCG. Additionally, a selector is enabled to export error-free data or data-recovery results. Importantly, an array-based computing structure, such as ME, discrete cosine transform (DCT), iterative logic array (ILA), and finite impulse filter (FIR), is feasible for the proposed EDDR scheme to detect errors and recover the corresponding data. This work adopts the systolic ME as a CUT to demonstrate the feasibility of the proposed EDDR architecture. A ME consists of many PEs incorporated in a 1-D or 2-D array for video encoding applications. A PE generally consists of two ADDs (i.e. an 8-b ADD and a 12-b ADD) and an accumulator (ACC). Next, the 8-b ADD (a pixel has 8-b data) is used to estimate the addition of the current pixel (Cur_pixel) and reference pixel (Ref_pixel). Additionally, a 12-b ADD and an ACC are required to accumulate the results from the 8-b ADD in order to determine the sum of absolute difference (SAD) value for video encoding applications Notably, some registers and latches may exist in ME to complete the data shift and storage. For example of the proposed EDDR circuit design for a specific PEi of a ME. The fault model definition, RQCG-based TCG design, operations of error detection and data recovery.

Motion estimation explores the temporal redundancy, which is inherent in video sequences, and it represents a basis for lossy video compression. Other than video compression, motion estimation can also be used as the basis for powerful video analysis and video processing.

A standard movie, which is also known as motion picture, can be defined as a sequence of several scenes. A scene is then defined as a sequence of several seconds of motion recorded without interruption. A scene usually has at least three seconds. A movie in the cinema is shown as a sequence of still pictures, at a rate of 24 frames per second. Similarly, a TV broadcast consists of a transmission of 30 frames per second (NTSC, and some flavors of PAL, such as PAL-M), 25 frames per second (PAL, SECAM) or anything from 5 to 30 frames per second for typical videos in the Internet. The name motion picture comes from the fact that a video, once encoded, is nothing but a sequence of still pictures that are shown at a reasonably high frequency. That gives the viewer the illusion that it is in fact a continuous animation. Each frame is shown for one small fraction of a second, more precisely 1/ k seconds, where k is the number of frames per second. Coming back to the definition of a scene, where the frames are captured without interruption, one can expect consecutive frames to be quite similar to one another, as very little time is allowed until the next frame is to be captured. With all this in mind we can finally conclude that each scene is composed of at least 3 × k frames (since a scene is at least 3 seconds long). In the NTSC case, for example, that means that a movie is composed of a sequence of various segments (scenes) each of which has at least 90 frames similar to one another.

Before going further with details on motion estimation we need to describe briefly how a video sequence is organized. As mentioned earlier a video is composed of a number of pictures. Each picture is composed of a number of pixels or pels (picture elements). A video frame has its pixels grouped in 8×8 blocks. The blocks are then grouped in macroblocks (MB), which are composed of 4 luminance blocks each (plus equivalent chrominance blocks). Macroblocks are then organized in “groups of blocks” (GOBs) which are grouped in pictures (or in layers and then pictures). Pictures are further grouped in scenes, as described above, and we can consider scenes grouped as movies. Motion estimation is often performed in the macroblock domain. For simplicity’ sake we’ll refer to the macroblocks as blocks, but we shall remember that most often the macroblock domain is the one in use for motion estimation.For motion estimation the idea is that one block b of a current frame C is sought for in a previous (or future) frame R. If a block of pixels which is similar enough to block b is found in R , then instead of transmitting the whole block just a “motion vector” is transmitted. MPEG-1 is a standard for lossy compression of video and audio. It is designed to compress VHS-quality raw digital video and CD audio down to 1.5 Mbit/s (26:1 and 6:1 compression ratios respectively) without excessive quality loss, making video CDs, digital cable/satellite TV and digital audio broadcasting (DAB) possible. Today, MPEG-1 has become the most widely compatible lossy audio/video format in the world, and is used in a large number of products and technologies. Perhaps the best-known part of the MPEG-1 standard is the MP3 audio format it introduced. The MPEG-1 standard is published as ISO/IEC 11172 – Information technology Coding of moving pictures and associated audio for digital storage media at up to about 1.5 Mbit/s. The standard consists of the following five Parts:

1. Systems (storage and synchronization of video, audio, and other data together)
2. Video (compressed video content)
3. Audio (compressed audio content)
4. Conformance testing (testing the correctness of implementations of the standard)
5. Reference software (example software showing how to encode and decode according to the standard).

Applications

- Most popular computer software for video playback includes MPEG-1 decoding, in addition to any other supported formats.
- The popularity of MP3 audio has established a massive installed base of hardware that can play back MPEG-1 Audio (all three layers).
- "Virtually all digital audio devices" can play back MPEG-1 Audio.[41] Many millions have been sold to-date.
- Before MPEG-2 became widespread, many digital satellite/cable TV services used MPEG-1 exclusively.
- The widespread popularity of MPEG-2 with broadcasters means MPEG-1 is playable by most digital cable and satellite set-top boxes, and digital disc and tape players, due to backwards compatibility.
- MPEG-1 is the exclusive video and audio format used on Video CD (VCD), the first consumer digital video format, and still a very popular format around the world.
- The Super Video CD standard, based on VCD, uses MPEG-1 audio exclusively, as well as MPEG-2 video.
- The DVD-Video format uses MPEG-2 video primarily, but MPEG-1 support is explicitly defined in the standard. The DVD-Video standard originally required MPEG-1 Layer II audio for PAL countries, but was changed to allow AC-3/Dolby Digital-only discs. MPEG-1 Layer II audio is still allowed on DVDs, although newer extensions to the format, like MPEG Multichannel, are rarely supported.
- Most DVD players also support Video CD and MP3 CD playback, which use MPEG-1.
- The international Digital Video Broadcasting (DVB) standard primarily uses MPEG-1 Layer II audio, and MPEG-2 video.
- The international Digital Audio Broadcasting (DAB) standard uses MPEG-1 Layer II audio exclusively, due to MP2's especially high quality, modest decoder performance requirements, and tolerance of errors.

Part 1: Systems

Part 1 of the MPEG-1 standard covers systems, and is defined in ISO/IEC-11172-1.

MPEG-1 Systems specifies the logical layout and methods used to store the encoded audio, video, and other data into a standard bit stream, and to maintain synchronization between the different contents. This file format is specifically designed for storage on media, and transmission over data channels that are considered relatively reliable. Only limited error protection is defined by the standard, and small errors in the bit stream may cause noticeable defects.

VII. SIMULATION RESULTS

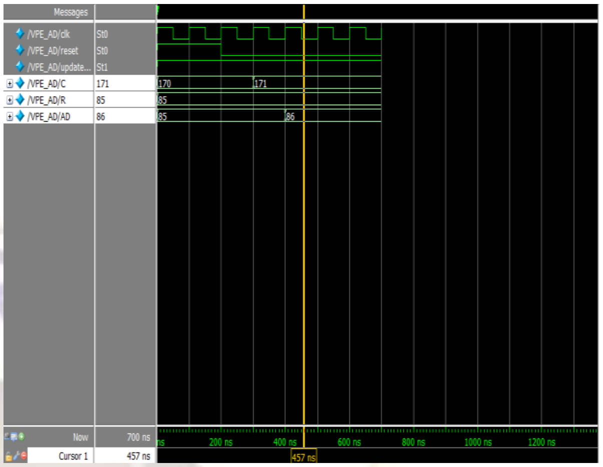

Fig.7. Processing element

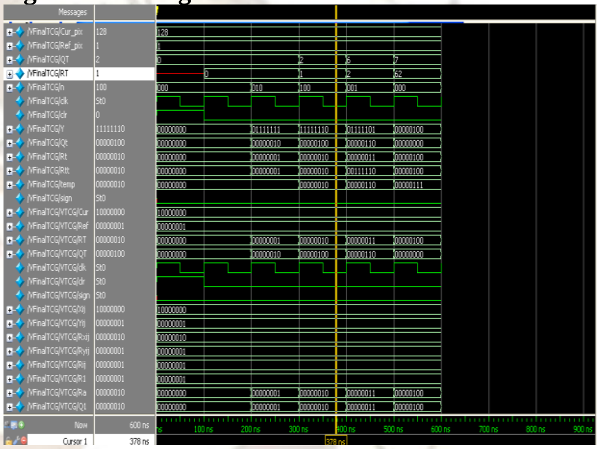

Fig.8. Test Code Generation

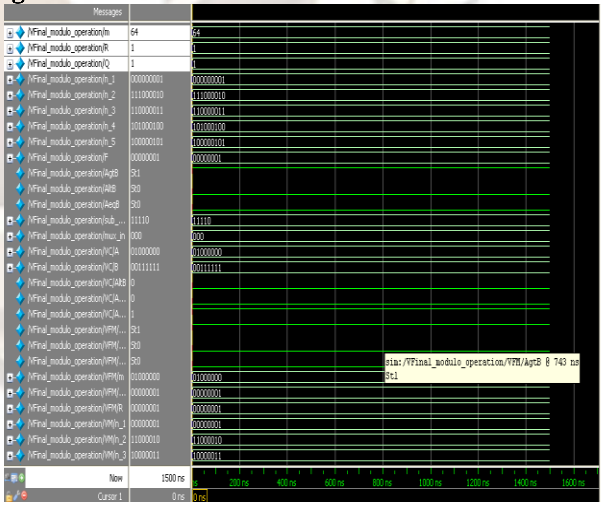

FIG.9. RQ Code Generation

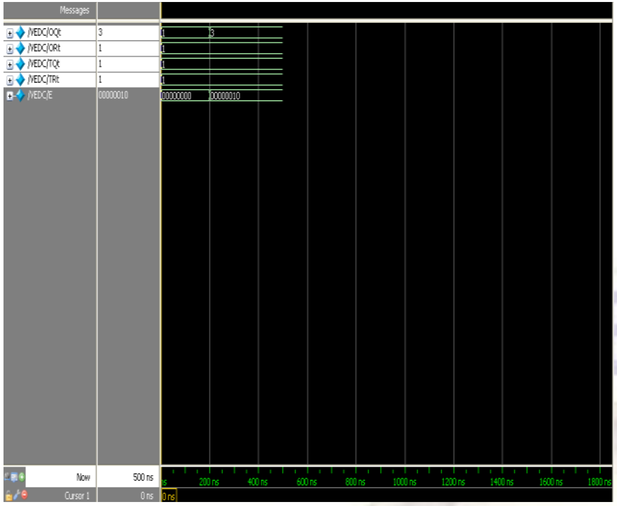

Fig.10. Error Detection Circuit

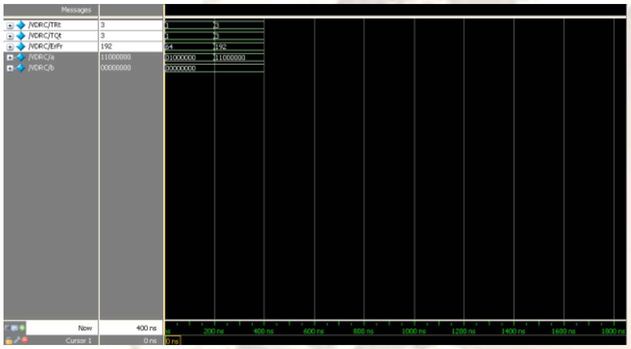

Fig.11. Data Recovery Circuit

VIII. CONCLUSIONS

This paper presents an FPGA implementation of efficient architecture for computing the 2-D DCT with distributed arithmetic. The proposed architecture requires less hardware than conventional architectures which use the original DCT algorithm or the even-odd frequency decomposition method. The modules of the transpose memory and parallel Distributed Arithmetic 2-D DCT architecture were designed and synthesized. The paper contributed with specific simplifications in the multiplier stage, by using shift and adds method, which lead to hardware simplification and speed up over architecture.

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