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4-Transistors of Dynamic Memristor based TCAM

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Abstract: **New hybrid hardware architecture, which compatible to CMOS technology also important role in a network like internet of fast searching of data. Here an explored new idea of CAM (content addressable Memory) with implemented emerging technology of Memristor. Great advantage of memristor, its nonvolatile, retention time of data stored at longer period In Dynamic 4 NMOS transistor used to describe about idea of CAM with memristor. Cell is assets of two things storing and matching with three elements required, hence terms comes ternary. It has three states is zero (0), one (1) and don't care condition (x). Circuits simulations show that all basics operations read, write and match at good speed. We proposed new dynamic hybrid TCAM cell good optimization of retention time and high speed search data.**

Keywords Memristor, CAM(content addressable memory), Modeling , SPICE, Window function, drift. TCAM

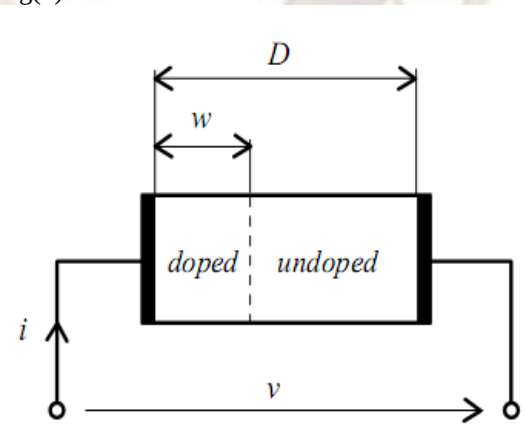
1. Introduction

In this paper new conceptualization of design and modeling of a Memristor based content addressable Memory (CAM) of architecture design and modeling. A typical base conventional content addressable Memory cell of SRAM that has 2 n-type and 2 p-type MOS transistors which requires both VDD and GND connections of well-plugs within each cell[2]. But also volatile, data is lost when memory is not powered. Here memristor technology, which has non-volatile memory (NVM) behavior and can be fabricated as an extension to a CMOS process technology with nanoscale geometry. In this single CAM only 4-NMOS transistors and 2-Mermristors is used. Main important data is never lost inside a memristor, if the powered is switch off also search line in this novel CAM inside. The main principle behind to stored and compared data it is allows data in parallel to be comparison. Therefore, fast speed search the data. if input data match to stored data indicated that data should be match. The application of CAM in major network side and pattern matching here main focus on Ternary CAM widely used in routers at routing table to compare destination address also memristor is work like switch, much similar to transistor but parameter view it has two terminal rather than three. The physics principle behind in memristor mobile ionic charge transfer one state to another state vice versa. This paper innovation new idea of architecture CAM of fast search good retention time without lost data.

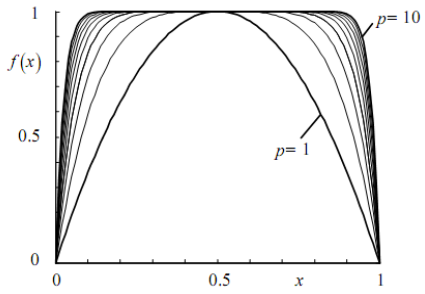
2. Nonlinear behavior of memristor

First prediction in 1978 theoretical of memristor in missing circuit paper by professor Chua [1] then later on 2008 first prototype memristor made in HP Lab [6]. The two layers of thin films one is doped region TiO_{2-X} another is undoped TiO_2 and sandwich between platinum is connected. Diameter (D=10nm) approx, which consist oxygen vacancies on doping side when voltage has given on doped area the mobile ionic charge of oxygen depleted on undoped region also resistance of both side should variable depend upon voltage. Such type characteristics has been done by using spice model by taken joglekar window function[8].

fig(1) Memristor Model in HP lab



D – diameter of thin film,
w- width of doped region
P- parameter of window function
μ_V- Migration coefficient
$R_{ON/ROFF}$ – Resistance ON/OFF States
R_{INIT} Resistance of T=0



fig(2) Window function, different 'p'value

fig(2) is window function depend upon by 'p' integer, if increase 'p' value disappear nonlinear drift.

Here ohm's law applicable in Memristor between voltage and current fig(1)

$$V(t) = R_{MEM}(w)\, I(t)$$

Variable and transfer the resistance from doped to undoped region depend upon current passed through Memristor.
Sum of resistance of R_{MEM} in doped and undoped region.

$$R_{MEM} = R_{ON}(X) + R_{OFF}(1-X)$$

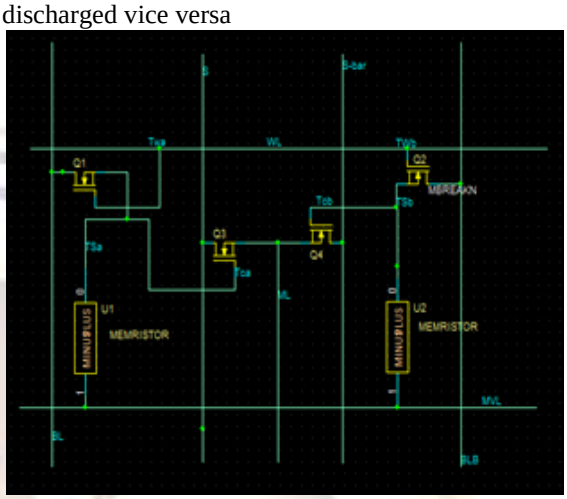
The proposed window function is a following term fig(2)

$$f(x) = 1 - (2x-1)^{2p}$$

Characterization of memristor in a form such manner to regulated in HP Lab in spice tools, here implementing of MCAM (Memristor based content addressable memory) Embodiment of TCAM to more efficiency and less power drop ,and high searching speed.

3. SPICE Modeling of Memristor based TCAM

Here used pass transistor of NMOS for made proposed MCAM (Memristor based CAM). They are 4 NMOS only used stored data and compared here below schematic diagram in fig (3) . Parameter mention write condition (Twa,Twb), data is stored in a (Tsa,Tsb) memristor here if compared data, its worked like XOR by (Tca,Tcb), Retrieved data Voltage has been given (MVL) , Which passed through (U1,U2) of Memristor. Stored data comes outside for start to matched. Now if data pass through (S1,S-bar) then inside data already present in a (Tca,Tcb) which comes from memristor to start matched. If data should be match line does not discharged vice versa



Fig(3) 4-T DCAM with Memristor

Table1: match operation

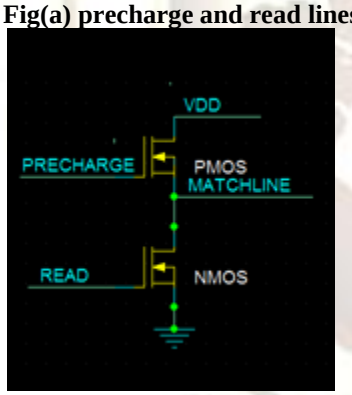
Stored	Tsa memristor(U1)	Tsb memristor(U2)	S(search line)	S0(search bar line)	Match condition
0	0	1	0	1	Match
0	0	1	1	0	No match
1	1	0	1	0	Match
1	1	0	0	1	No Match
X	0	0	X	X	Match

Here above table ternary cam operation has been done there is match condition its only created. When the (U1,U2) memristor and search line should be 1 or 0 . There is X dont care condition which can resembale to be operated fast search the data in ternary cam. Also XOR Tca and Tcb is word compared data between search line and memristor (U1,U2). The proposed Dynamic CAM cell needed refresh cycle during read and write operation[3].

4. Read and Write Operations

Simple basic operation of write condition (Twa,Twb) of Transistors is can be done by logic '1.' Here pointed out the write condition take place all the same row also that time match line should be kept as floating, Tpch and Trd are off. In memristor of U1 and U2 data is saved during write time at that time do not need refresh only simple write and saved data is present. Memristor is very prominent data saved long duration time. And (S,S0) input address search line will be off on write conditionRead time of MVL(Memristor Voltage line) would be activated, so in such case memristor in data is retrived passed through transistor (Tca,Tcb). Here compared data between search data (S,S0) and Transistor (Tca,Tcb), if both data should be match then data should not be discharged. If does not match then it is discharaged. In convational CAM, search line located in outside. But in this proposed CAM search line are inside In fig(5) during read operation its necessary BIT,NBIT and match line precharge must be one. Once's precharged is activated Trd line is high then match line drawn to ground state. So ternary CAM, its followed don't care condition, whatever data present in BIT,NBIT line latched also (Tca,Tcb) equal to '0' and line is not to be discharged.

Fig(a) precharge and read lines

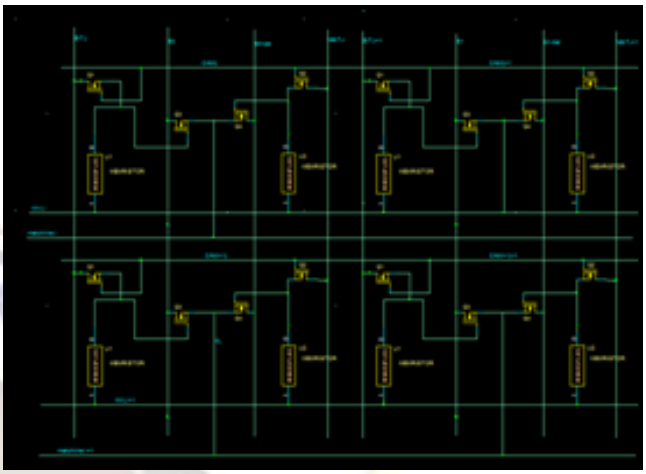


In **fig(4)** 2×2 MCAM architecture by suggested Matchline1 condition, Here data is search(1,0), In fig(c) waveform green is MVL and yellow is a Match line. "The first row cells are programmed "10". As the consequence, ML is discharged since there is a match between the stored and search bit for mention ML is output

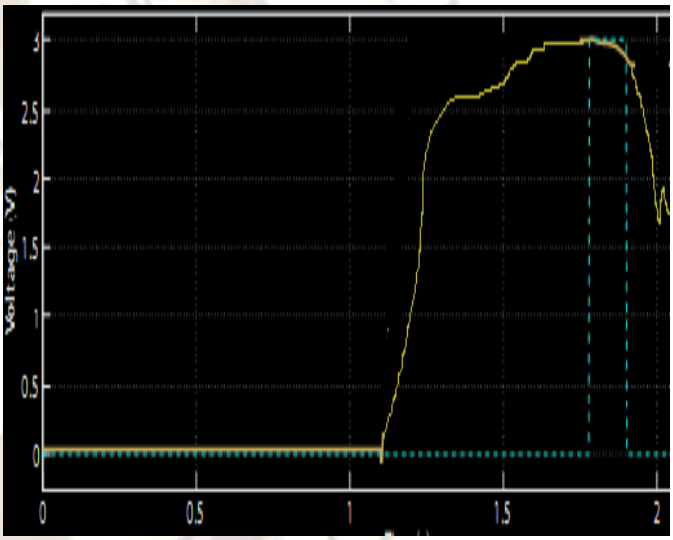
RESULT Simulation circuit based on following parameters [9] Ron = 100Ω, Roff = 100kΩ, D = 10nm, P = 5,μ_v = 3×10^{-8} $m^2/s/V$ it can be impleme0.18technology

Table2: Power TCAM and Memristor

Dynamic MCAM	Power (Memristor)	Total Power
4T	36.2µW	409.4µW



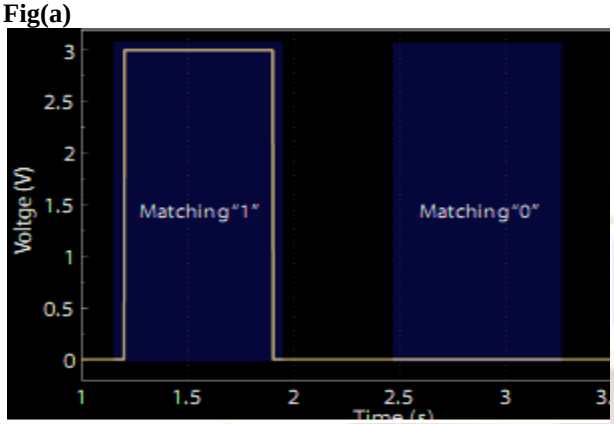
Fig(b) 2x2 HybridTCAM



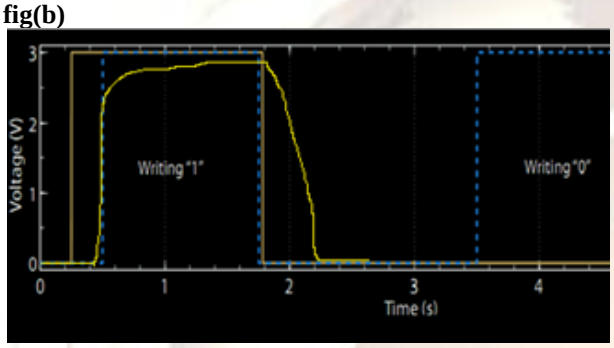
fig(c) 2x2 TCAM wave form Analysis

5. Waveform Analysis

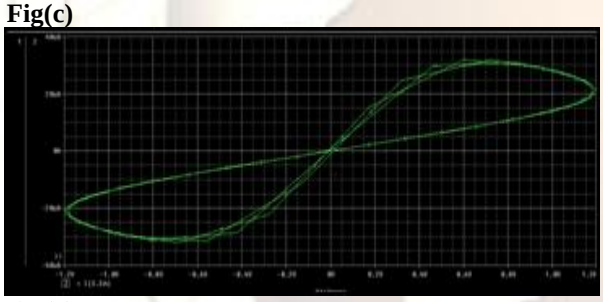
Fig(a)



fig(b)



Fig(c)



Fig(d)

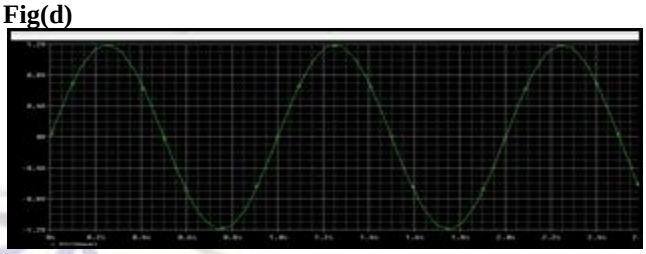


Fig (e)

Fig (5)

Search line S in 3Volt during match condition at Matching line fig (a) read, write and match in 3 volt fig (b) 40µA current passed U1memristor(e), Indicated 1.2 voltage and frequency 1Hz (d) , Hystresis curve volgate versus current in Memristor(c)

6. SPICE code of TCAM with Memristor:-

```
* source Dynamic_4T_CAM
M_M1          BL TWB M1 M1 NFET
+ L=180nm
+ W=1800nm
M_M2          S M1 ML ML NFET
+ L=180nm
+ W=1800nm
X_U2          M2 MVL MEMRISTOR PARAMS:
+  UV=3E-8 P=5
M_M3          S0 M2 ML ML NFET
+ L=180nm
+ W=1800nm
M_M4          BLB TWB M2 M2 NFET
+ L=180nm
+ W=1800nm
V_V1          BL GND 3Vdc
V_V2          S GND 3Vdc
V_V3          S0 GND 0Vdc
V_V4          BLB GND 0Vdc
V_V5          TWB GND 3Vdc
X_U1          M1 MVL MEMRISTOR PARAMS:
+  UV=3E-8 P=5
V_V6          MVL GND 3Vdc
.END
```

Conclusion

In this paper presented novel dynamic hybrid based TCAM only utilizes 4T-NMOS. Here we can flash a made new technology in future, which challenge scaling CMOS technology below 15nm of nanoscale. Memristor strong innovate device for terabit/compare logic. Main important factor data is never lost of many years if power is lost. In future hope new trend to design of TCAM with memristor which emphasize electronic circuits

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