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An Effective BIST TPG for Variable Precision Floating Point Multiplier

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ABSTRACT
The accuracy of the multiplication depends on the precision of the multiplier. The variable precision floating point multiplier will have more accuracy when compared with the fixed precision multiplier. In this paper a variable precision floating point multiplier is considered. An effective BIST test pattern generator for variable precision floating point multiplier is proposed. A BIST TPG consists of pseudo random test pattern generator for the variable precision floating point multiplier and a comparator is used to compare the output response and the expected response, a control unit is used for selecting either primary inputs or the test pattern for the variable precision floating point multiplier. The Linear feedback shift registers are used to generate the pseudo random test pattern generation. The LFSR are very much efficient in producing the random test vectors which is used to produce high fault coverage.

Keywords: - **Variable Precision, Multiplication, BIST TPG, LFSR, Fault Coverage, Accuracy.**

I. INTRODUCTION
The speed of computation in computers has increased dramatically during the last decade. This increase in speed is due to the development of VLSI technology that has enabled the integration of millions of transistors on the same chip [1]. The accuracy of the computation has not been developed in proportionate with speed of computation. When large operands are considered the accuracy plays a major role in the overall computation. Without accuracy, errors can easily prone in the system. When multipliers are considered the accuracy of the multipliers depend on the precision of the multiplier. So variable precision floating point multipliers will have more accurate results when compared with the fixed precision multipliers.

The digital systems are tested and diagnosed during its lifetime on numerous occasions. The development of denser and faster ICs resulted in logic blocks with low controllability and observability that need to be tested at speed to make the entire chip reliable product. The BIST (Built-In-Self-Test) is very much useful in such a scenario where they can reduce the cost of testing by eliminating the need of external testing circuitry [2], also the BIST have the capability of applying the pseudo random test vectors using LFSR [3] at desired operating speed. A proper designed Built-In-Self-Test (BIST) is able to offset the cost of added test hardware while at the same time ensuring the reliability, testability and reduce maintenance cost[4]-[7]. The basic idea of BIST, in its most simple form, is to design a circuit so that the circuit can test itself and determine whether it is fault-free or faulty, respectively. In this paper a BIST TPG for variable precision floating point multiplier is proposed which is capable of testing the circuit with very high fault coverage.

This paper is organised as follows, the section II introduces the existing variable precision multiplication, in section III gives the introduction of BIST, in section IV the BIST TPG for variable precision floating point multiplier is proposed, section V gives the implementation results of the proposed BIST for variable precision floating point multiplier and section VI concludes the paper and followed by the references.

II. EXISTING VARIABLE PRECISION MULTIPLICATION
The existing variable precision multiplication is based on the variable precision format shown below in the fig 1 [1]. Each variable precision number consists of exponent field (E) of 16 bit, a one bit sign bit (S), a type field (T) of two bits and a five bit length (L) field and significant field (F) which contains L+1 significant words (F (0) to F (L)).if the word is positive the sign bit is termed as zero and if the word is negative the sign bit is termed as one [1]. The type field contains whether the number is normalized, infinite, zero or not a number. The length bit shows the number of m bit words present in the significant. The words in the significant are stored in the format of most significant F (0) to least significant F (L) [5].

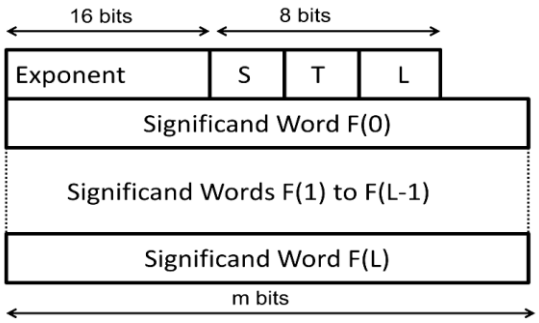

Figure 1:- Variable Precision Format.

The existing variable precision floating multiplier is based on the algorithm which can be implemented easily on any hardware [1]. The algorithm reduces the memory that is used to store the partial products that are generated during computation in classic multiplication method by adding the partial products as soon as they are computed. This algorithm only uses the memory of (n x 2m) bits instead of (n^2 x 2m) bits that are used in the classic multiplication. This algorithm splits the operands A and B and the result into m bits. Depending on the value of the m the size of the multiplier and the memory are considered [1].

III. INTRODUCTION TO BUILT IN SELF TEST (BIST)

The Built In Self Test (BIST) is the mechanism that allows the circuit to test itself. The main requirements of the BIST are high reliability and fault coverage with low number of test cycles [3]. The BIST is mainly used for testing the circuit faster and reduce the cost of the added test hardware.

The purpose of considering the BIST is to reduce the complexity of the testing hardware and thereby reducing the overall cost required for the testing process by not considering any external testing hardware to test the circuit[6]-[7],. The basic BIST architecture is shown in the fig 2 below

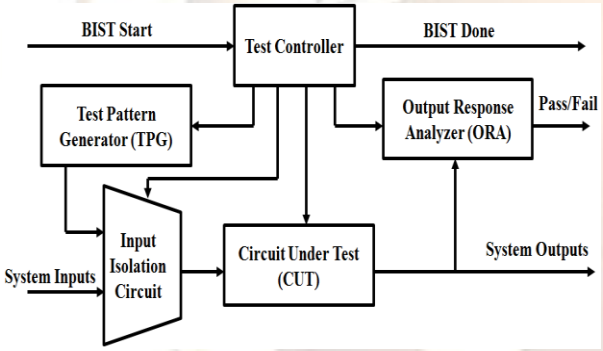

Figure 2:- Basic BIST architecture

The main essentials of the BIST are the test pattern generator (TPG) and the output response analyzer (ORA). While the TPG produces a sequence of patterns for testing the Circuit Under Test, the ORA compacts the output responses of the Circuit Under Test and shows the result as pass or fail, which indicates fault free and faulty circuits.

IV. PROPOSED BIST TPG FOR VARIABLE PRECISION FLOATING POINT MULTIPLIER

In digital circuits the BIST can be applied in two different approaches, namely deterministic and pseudo random. In the deterministic approach a pre defined test patterns are applied to the circuit with fault coverage based on the adopted model. In the pseudo random approach the circuit is applied with pseudo random test patterns and the fault simulation is used to calculate the test efficiency.

In this paper the pseudorandom approach is considered as this approach has an important advantage of low cost as the test patterns can be easily generated using the LFSR. The fig 3 shows the proposed BIST for variable precision floating point multiplier.

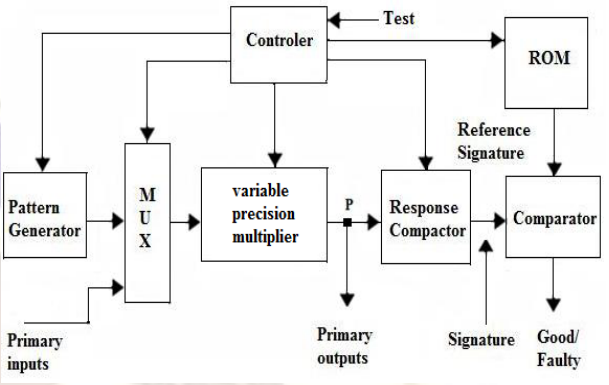

Figure 3:- Proposed architecture for BIST TPG for variable precision floating point multiplier.

The pattern generator used is the linear feedback shift register. The pseudo random test patterns that are generated using the LFSR are fed to the multiplexer unit, the primary inputs that are given from the outside world are also fed to the multiplexer unit. The controller is used to control the BIST operation, when the test signal is taken as high (1), then the test pattern that is generated by the LFSR are fed to the inputs of the circuit under test that is the variable precision floating point multiplier. If the test signal is low (0), then the primary inputs are fed to the variable precision floating point multiplier.

When the circuit is under test, the expected output response is calculated and stored in the ROM. When the actual response from the variable precision floating point multiplier is obtained then the response comparator compares both the responses and if both matches with each other then the flag is turned high (1) showing that the circuit is fault free. If the obtained response and expected response mismatches the flag is turned low (0), showing that the circuit under test is a faulty circuit.

As the pseudo random test vectors are used to test the variable precision floating point multiplier, BIST TPG will have a very high fault coverage value. The fault coverage of the proposed Built in self test is 99.8%. Also the delay characteristics of the variable precision floating point multiplier with BIST doesn't vary much, even after adding additional hardware for the BIST test pattern generation. Only a delay of one nano second is increased when compared with the actual delay of the variable precision floating point multiplier without BIST. The fig 4 shows the flow chart for the proposed BIST test pattern generator for variable precision floating point multiplier.

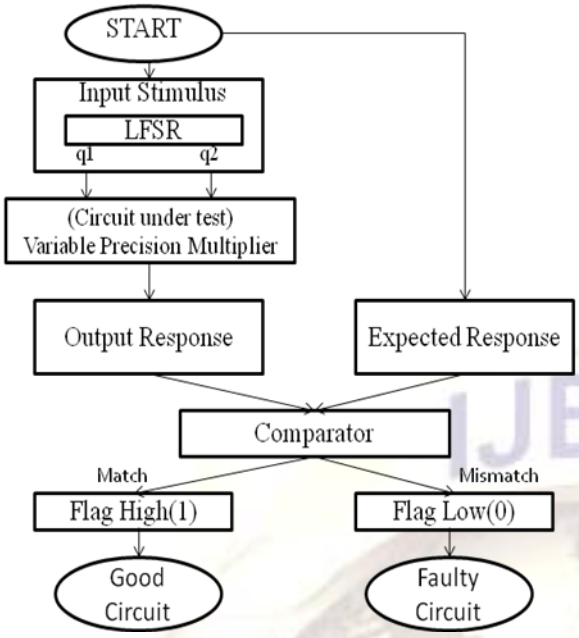

Figure 4:- Flow Chart for BIST TPG for variable precision multiplier.

V. IMPLEMENTATION RESULTS OF THE PROPOSED BIST TPG FOR VARIABLE PRECISION MULTIPLIER

The BIST architecture is implemented on 32- bit variable precision floating point multiplier using XILINX ISE 10.1. It has been mapped and routed on XILINX FPGA circuit of family Spartan 3E XC3S500E. The implementation results are shown below, the fig 5 shows the 32-bit simulation results of the BIST TPG for variable precision multiplier.

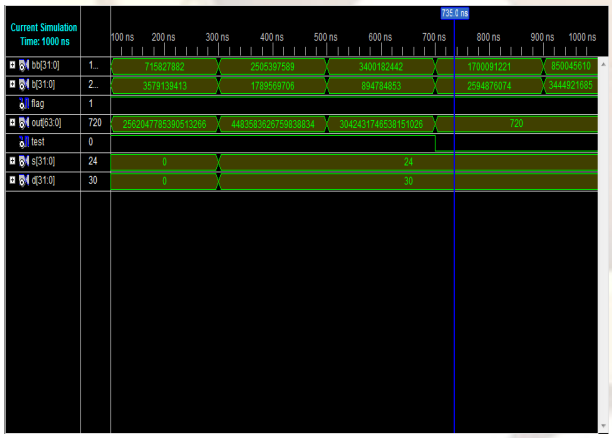

Figure 5:- 32-bit simulation output of BIST TPG for variable precision multiplier

In the simulation result shown in fig 5, s and d are primary inputs and b and bb are the pseudo random test vectors, out is the output response, the flag bit shows the BIST result and test is used as selection for the BIST control unit. The table 1 shows the synthesis results of the proposed BIST TPG architecture. The delay characteristics are also analysed and tabulated.

Table 1:- 32 bit variable precision multiplier simulation result of the proposed BIST architecture

Logic utilization	Used	Available	Utilization
No. of Slices	651	4656	12%
No. of 4-input LUT's	1198	9312	12%
Number of bonded IOB's	194	232	83%
Number of MULTI18X18SIO's	20	20	100%
Combinational path delay	58.010ns		

IV. CONCLUSION

A BIST TPG for variable precision floating point multiplier is proposed. Pseudorandom test patterns are considered to have very high fault coverage. The BIST included in the circuit doesn't affect the delay characteristics of the circuit under test ie., variable precision floating point multiplier, also the cost of the testing circuit is very low when compared with external testing circuits. The simulation and synthesis results are analysed using Xilinx ISE.

REFERENCES

[1] Rohit Sreerama, Paidi Satish, K Neelima. "An Algorithm for variable precision based floating point multiplication", *proc* International Conference on Advances in Information Technology and Mobile Communication, AIM 2012, page no-238-242

[2] D.Bakalistx. Kavousianos, H. T. Vergos D. Nikolos And G. Piq. Alexiou, "Low Power Built-In Self-Test Schemes for Array and Booth Multipliers" Vlsi Design 2001, Vol. 12, No. 3, Pp. 431-448

[3] Xilinx Application Note by Peter Alfke "Efficient Shift Registers, Lfsr Counters, And Long Pseudo-Random Sequence Generators" July 7,1996 (Version 1.1).

[4] Jutman, A.; Tsertov, A.; Ubar, R. "Calculation of LFSR Seed and Polynomial Pair for BIST Applications" Design and Diagnostics of Electronic Circuits and Systems, 2008. DDECS 2008. 11th IEEE Workshop16-18 April 2008.page no 1-4.

[5] Serdar S. Erdem ,Çetin K. Koç, "A Less Recursive Variant of Karatsuba-Ofman Algorithm for Multiplying Operands of Size a Power of Two", 16th IEEE Symposium on Computer Arithmetic, 2003

[6] Zhiquan Zhang Zhiping Wen ; Lei Chen "BIST Approach for testing Embedded Memory Blocks in System-on-Chips" Testing and Diagnosis, 2009. ICTD 2009. IEEE Circuits and Systems International Conference 28-29 April 2009, pg no 1-3.

[7] Shianling Wu; Furukawa, H.; Boryau Sheu; Laung-Terng Wang; Hao-Jan Chao; Lizhen Yu; Xiaoqing Wen; Murakami, M. "Practical Challenges in Logic BIST Implementation – Case Studies" Asian Test Symposium, 2008 Page(s): 265 – 265.

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