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48 pulse VSC control by using ISPWM

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ABSTRACT
In this thesis 48-pulse voltage source converter by using inverted sine pulse width modulation technique is modeled to eliminate the harmonic of the system produced by the non-linear load. For the harmonic elimination different methods are used. This thesis describes the operation of 48-pulse VSC with novel PWM technique. There are many Pulse Width Modulation Techniques are used to firing of Switching Devices like Sinusoidal Pulse Width Modulation, Space Vector Pulse Width Modulation, Delta Modulation etc. Here by using ISPWM technique we can achieve greater pulse area then conventional PWM techniques to reduce the harmonics and switching losses.

Keywords–**48-pulse VSC, ISPWM, PWM, IGBT,FACTS devices.**

I. INTRODUCTION
Traditional HVDC and FACTS installations have often provided economic solutions for special transmission applications. HVDC is well-suited for long-distance, bulk-power transmission, long submarine cable crossings, and asynchronous interconnections. Static var compensators (SVC) provide a reserve source of dynamic reactive power thereby raising power transfer limits. HVDC and FACTS technologies permit transmitting more power over fewer transmission lines.
Deregulated generation markets, open access to transmission, formation of RTO's, regional differences in generation costs and increased difficulty in siting new transmission lines, however, have led to a renewed interest in FACTS and HVDC transmission often in non-traditional applications. This is especially true with the lag in transmission investment and the separation in ownership of generation and transmission assets. HVDC and FACTS transmission technologies available today offer the planner increased flexibility in meeting transmission challenges. HVDC transmission and reactive power compensation with voltage source converter (VSC) technology has certain attributes which can be beneficial to overall system performance. HVDC Light™ and SVC Light™ technology developed by ABB employs voltage source converters (VSC) with series-connected IGBT (insulated gate bipolar transistor) valves controlled with pulse width modulation (PWM). VSC converters used for power transmission (or voltage support combined with an energy storage source) permit continuous and independent control of real and reactive power. Reactive power control is also independent of that at any other terminal. Reactive power control can be used for dynamic voltage regulation to support the interconnecting ac system following contingencies. This capability can increase the overall transfer levels. Forced commutation with VSC even permits black start, i.e., the converter can be used to synthesize a balanced set of three phase voltages much like a synchronous machine.
Mainly, two basic configurations of VSCs are used on HVDC transmission system. These are the two-level VSC converter, The two-level VSC, also known as the three phase, two level, six-pulses bridge, is the simplest configuration suitable for HVDC transmission. Such a converter consists of six valves (each valve consist of an IGBT and an anti-parallel diode) and is capable of generating two voltage levels 0:5 Vdc n and +0:5 Vdc n. In high power applications, the three-level VSC configuration), represents a reliable alternative to the two-level VSC configuration, because the phase potentials can be modulated between three levels, 0:5 Vdcn, 0 and +0:5Vdc n. In this configuration, one arm of the converter consists of four valves.

II. 48- PULSE, 3- LEVEL VSC
The 48-pulse VSC generates less harmonic distortion and, hence, reduces power quality problems in comparison to other converters such as (6, 12, and 24) pulse. This results in minimum operational overloading and system harmonic instability problems as well as accurate performance prediction of voltage and dynamic stability conditions.[6]
Two 24-pulse GTO-converters, phase-shifted by 7.5 from each other, can provide the full 48-pulse converter operation. Using a symmetrical shift criterion, the 7.5 are provided in the following way: phase-shift winding with -3.75'on the two coupling transformers of one 24-pulse converter and+3.75'on the other two transformers of the second 24-pulse converter. The firing pulses need a phase-shift of +3.75', respectively. The 48-pulse converter model comprises four identical 12-pulse GTO converters interlinked by four 12-pulse trans-formers with phase-shifted windings [9].

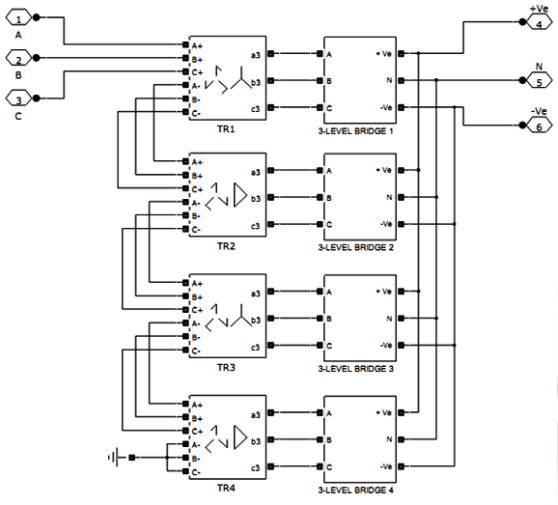


Figure 1. 48-pulse, 3-level VSC

Fig.1 depicts the schematic diagram of the 48-pulse VSC-GTO converter model. The transformer connections and the necessary firing-pulse logics to get this final 48-pulse operation are modeled. The 48-pulse converter can be used in high-voltage high-power applications without the need for any ac filters due to its very low harmonic distortion content on the ac side. The output voltage have normal harmonics n=48r+1 where r=0,1,2,3....i.e; 47th, 49th, 95th, 98th... with typical magnitudes (1/47th, 1/49th, 1/95th, 1/97th..), respectively, with respect to the fundamental; on the dc side, the lower circulating dc current harmonic content is the 48th . The phase-shift pattern on each four 12-pulse converter cascade is as follows.[6]

1st 12-Pulse Converter: It is shown in the equation at the bottom of the page. The resultant output voltage generated by the first 12-pulse converter is

$$v_{ab12}(t)_1=2[V_{ab1}\sin(\omega t+30°)+V_{ab11}\sin(11\omega t+195°)+V_{ab13}\sin(13\omega t+255°)+V_{ab23}\sin(23\omega t+60°)+V_{ab25}\sin(25\omega t+120°)+\cdots\cdots\cdots\cdots\cdots\cdots\cdots].\quad(1)$$

2nd 12-Pulse Converter: It is shown in the second equation at the bottom of the previous page. The resultant output voltage generated by the second 12-pulse converter is

$$v_{ab12}(t)_2=2[V_{ab1}\sin(\omega t+30°)+V_{ab11}\sin(11\omega t+15°)+V_{ab13}\sin(13\omega t+75°)+V_{ab23}\sin(23\omega t+60°)+V_{ab25}\sin(25\omega t+120°)+\cdots\cdots\cdots\cdots\cdots\cdots\cdots].\quad(2)$$

3rd 12-Pulse Converter: It is shown in the first equation at the bottom of the page. The resultant output voltage generated by the third 12-pulse converter is

$$v_{ab12}(t)_3=2[V_{ab1}\sin(\omega t+30°)+V_{ab11}\sin(11\omega t+285°)+V_{ab13}\sin(13\omega t+345°)+V_{ab23}\sin(23\omega t+240°)+V_{ab25}\sin(25\omega t+300°)+\cdots\cdots\cdots\cdots\cdots\cdots\cdots].\quad(3)$$

4th 12-Pulse Converter: It is shown in the second equation at the bottom of the page. The resultant output voltage generated by the fourth 12-pulse converter is

$$v_{ab12}(t)_4=2[V_{ab1}\sin(\omega t+30°)+V_{ab11}\sin(11\omega t+105°)+V_{ab13}\sin(13\omega t+165°)+V_{ab23}\sin(23\omega t+240°)+V_{ab25}\sin(25\omega t+300°)+\cdots\cdots\cdots\cdots\cdots\cdots\cdots].\quad(4)$$

These four identical 12-pulse converter provide shifted ac output voltages, described by (1)–(4), are added in series on the secondary windings of the transformers. The net 48-pulse ac total output voltage is given by

$$v_{ab48}(t)=v_{ab12}(t)_1+v_{ab12}(t)_2+v_{ab12}(t)_3+v_{ab12}(t)_4\quad(5)$$

$$v_{ab48}(t)=8[V_{ab1}\sin(\omega t+30°)+V_{ab47}\sin(47\omega t+150°)+V_{ab49}\sin(49\omega t+210°)+V_{ab95}\sin(95\omega t+330°)+V_{ab97}\sin(97\omega t+30°)+\cdots\cdots\cdots\cdots\cdots\cdots\cdots].\quad(6)$$

The line-to-neutral 48-pulse ac output voltage is expressed by

$$v_{an48}(t)=\frac{8}{\sqrt{3}}\sum_{n=1}^{\infty}V_{abn}\sin(n\omega t+18.75°n-18.75°i)\quad(7)$$

$$n=(48r\pm1),\ r=0,1,2\ldots\ldots\quad(8)$$

Voltages $v_{bn48}(t)$ and $v_{cn48}(t)$ have a similar near sinusoidal shape with a phase shifting of 120 and 240, respectively, from phase a $v_{an48}(t)$.

III. INVERTED SINE PWM SPWM

The basic single-phase full-bridge PWM inverter is shown in Fig. 2 in which S1 and S2 will be given PWM pulses for first (positive) output half cycle and S3 and S4 are gated for the next (negative) half cycle. The unipolar PWM pulse generation with resulting pattern is represented in Fig. 3 in which a triangular carrier wave is compared with sinusoidal reference waveform to generate PWM gating pulses.

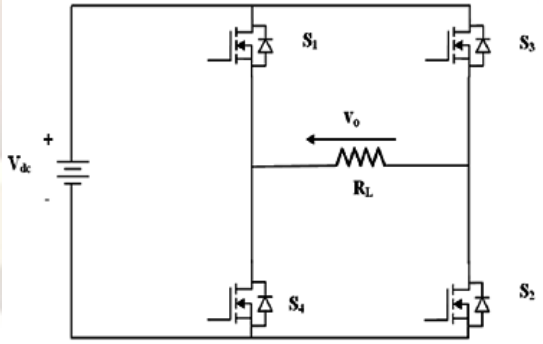


Figure 2 Single phase inverter

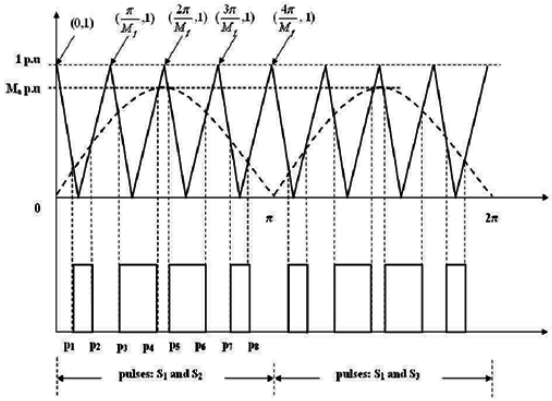


Figure 3. SPWM pulse generation

The harmonics present in the quasi square wave and their relative amplitudes always remain the same. With PWM, however, the relative amplitudes of the harmonics change with the modulation index. The use of SPWM in inverters, for all its technical benefits, renders most complex calculations relating to inverter behavior. It is generally accepted that the performance of an inverter with any switching strategy can be related to the harmonic content of its output voltage [7].

A precise value of the switching angle and hence duty cycle can be obtained through the triangular (carrier) and the sinusoidal (reference) equations. The modulation pattern of the SPWM control (Fig. 6) indicates the switching angles meeting points (p1, p2, p3…pi). The PWM control signal is obtained by comparing a high frequency triangular carrier of frequency fc and amplitude 1(per unit) and a low frequency sine wave of frequency fm and amplitude Ma (per unit). Equations for sinusoidal reference and triangular carrier are given by (1) and (2) respectively.

$$y = M_a \sin x, \qquad (1)$$

$$x \pm \left(\frac{\pi}{2M_f}\right), \quad y = \frac{r\pi}{2M_f}, \qquad (2)$$

Where: Ma - modulation index;

Mf - frequency ratio;

r -1 for first pair of triangular sections (straight lines), 3 for second pair, 5

for third pair and so on;

'+' - sign should be taken for odd number of line sections and

'-' - sign for should be taken for even number of line sections.

The equations describing the natural sampled switching angles are transcendental and have the general distinct solutions for odd and even meeting points. The condition for switching angles is given in (3) and (4) respectively for odd and even switching angles.

$$M_a \sin p_i + \frac{2M_f p_i}{\pi} = i, \quad i = 1,3,5\ldots, \qquad (3)$$

$$M_a \sin p_i - \frac{2M_f p_i}{\pi} = 1 - i, \quad i = 2,4,6\ldots, \qquad (4)$$

Where i is number of points and pi is i-th switching angle. The pattern represented in Fig. 3 does have eight switching angles and four PWM pulses. The duty cycle can be calculated by simply adding the width of the individual pulses. The width of any pulse can be found from subtracting one odd meeting point from immediate even successor. Since the inverter output irrespective of control methods exhibits equal positive and negative half cycles, which results in zero dc component (a0 =0), and also does not possess any even harmonics due to half wave symmetry. Equation (5) gives the generalized Fourier coefficients for the problem considered. In the equation p i′ represents switching angles corresponds to negative half cycle.

$$a_n = \frac{V_{dc}}{n\pi\sqrt{2}} \sum_{k=1}^{i-1} \{(\sin n p_{k+1} - \sin n p_k) - (\sin n p'_{k+1} - \sin n p'_k)\},$$

$$b_n = \frac{V_{dc}}{n\pi\sqrt{2}} \sum_{k=1}^{i-1} \{(\cos n p_{k+1} - \cos n p_k) - (\cos n p'_{k+1} - \cos n p'_k)\}, \qquad (5)$$

$$c_n = \sqrt{a_n^2 + b_n^2}.$$

ISCPWM

The control strategy uses the same reference (synchronized sinusoidal signal) as the conventional SPWM while the carrier triangle is a modified one. The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. Enhanced fundamental component demands greater pulse area. The difference in pulse widths (hence area) resulting from triangle wave and inverted sine wave with the low (output) frequency reference sine wave in different sections can be easily understood. In the gating pulse generation of the proposed ISCPWM scheme shown in Fig. 3, the triangular carrier waveform of SPWM is replaced by an inverter sine waveform.

Considering angle θ as an intersection angle of carrier and reference signals, the following equations can be calculated:

$$1 - Sin[m_f \theta_p - \frac{\pi}{2}(p-1)] = m_a Sin\theta_p, \quad for\ p = 1,3,5,\ldots$$

$$1 + Sin[m_f \theta_p - \frac{\pi}{2}(p-2)] = m_a Sin\theta_p, \quad for\ p = 2,4,6,\ldots$$

Based on Fourier analysis, all harmonics of output voltage waveform can be calculated. When mf is an odd number, the half cycles of the phase voltage Vao are the same but with opposite sign and each half cycle is symmetrical with respect to half cycle midpoint.

Therefore, (mf-1)/2 angles should be determined using following equations.

$$\frac{\pi}{2} - \theta_{(m_f-1)/2} = \theta_{(m_f+1)/2} - \frac{\pi}{2} = \frac{3\pi}{2} - \theta_{(3m_f-1)/2} = \theta_{(3m_f+1)/2} - \frac{3\pi}{2}$$

$$\frac{\pi}{2} - \theta_{(m_f-3)/2} = \theta_{(m_f+3)/2} - \frac{\pi}{2} = \frac{3\pi}{2} - \theta_{(3m_f-3)/2} = \theta_{(3m_f+3)/2} - \frac{3\pi}{2}, \ldots$$

$$\theta_{m_f} = \pi, \theta_{2m_f} = 2\pi$$

Fourier expansion of the output waveform when m is also an odd number consists of only odd harmonic orders.

$$V_{a0} = A_1 Sin\omega t + A_3 Sin3\omega t + A_5 Sin5\omega t + \ldots\ldots + A_n Sinn\omega t$$

Where,

$$A_n = \frac{4}{\pi}\int_0^{\pi/2} v_{AO} Sinn\omega t d\omega t$$

$$= \frac{4}{\pi}\frac{V_{DC}}{2}[\int_0^{\theta_1} Sin\omega t d\omega t - \int_{\theta_1}^{\theta_2} Sin\omega t d\omega t + ... \pm \int_{\theta_{m-1/2}}^{\pi/2} Sin\omega t d\omega t]$$

$$A_n = \frac{1}{n}.\frac{4}{\pi}.\frac{V_{DC}}{2}(1 - 2Cosn\theta_1 + 2Cosn\theta_2 - .... \pm 2Cosn\theta_{m-1/2})$$

Using the same method, Fourier series for Vbo can be expressed as follows:

$$V_{bo} = A_1 Sin(\omega t - \frac{2\pi}{3}) + A_3 Sin3(\omega t - \frac{2\pi}{3}) + A_5 Sin5(\omega t - \frac{2\pi}{3}) + ... + A_n Sinn(\omega t - \frac{2\pi}{3})$$

It is obvious that the line voltage Vab has no triple harmonics. In addition, if mf is equal to 3k for k =1, 2… then the line lowest harmonic orders are mf-2 , mf+2, 2mf-2 and 2mf+2 (e.g., for mf=9 the order of these harmonics are 7, 11, 17 and 19).

For the ISCPWM pulse pattern, the switching angles may be computed as the same way as SPWM scheme. The equations of inverted sine wave is given by (6) and (7) for its odd and even cycles respectively. The intersections (q1, q2, q3 …qi) between the inverted sine voltage waveform of amplitude 1 p.u and frequency fc and the sinusoidal reference waveform of amplitude Ma p.u and frequency 0f can be obtained by substituting (1) in both (6) and (7). The switching angles for ISCPWM scheme can be obtained from (8) and (9).

$$y = 1 - \sin\left(M_f x - \frac{\pi}{2}(i-1)\right) \quad (6)$$

$$y = 1 - \sin\left(M_f x - \frac{\pi}{2}(i-2)\right) \quad (7)$$

$$M_a \sin q_i + \sin\left(M_f q_i - \frac{\pi}{2}(i-1)\right) = 1, \quad i = 1,3,5... \quad (8)$$

$$M_a \sin q_i + \sin\left(M_f q_i - \frac{\pi}{2}(i-2)\right) = 1, \quad i = 2,4,6... \quad (9)$$

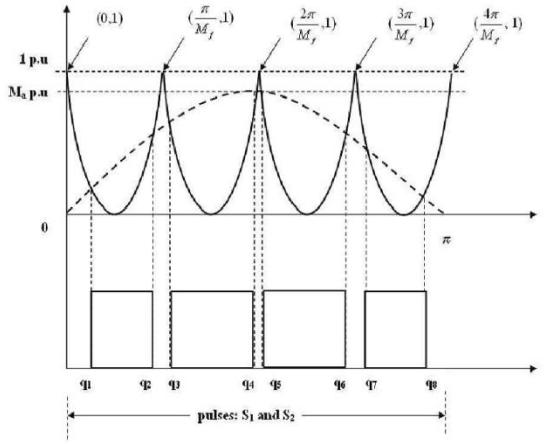


Figure 4. Inverted sine wave PWM pulse generation

It is worthwhile to note that both in SPWM (considered) and ISCPWM schemes, the number of pulses will be equal to Mf and hence the constant switching loss is guaranteed. To have conceptual understanding of wider pulse area and hence the dexterous input dc utilization in the ISCPWM, location of switching angles, duty cycle and their dependence on Ma and Mf are discussed. Fig. 5 depicts the influence of Ma on different switching angles (four angles considered in both cases) at constant Mf of 6. From this figure, it is observed that the odd switching instants vary with negative slope and even switching instants have positive slope. Variation of all the switching instants against Ma is a straight line and slope of each one is more than its previous one. All the odd switching angles of ISCPWM method happen earlier than similar angles of PWM method, while the situation is reverse in case of even switching angles and hence higher pulse area. Fig. 6 gives the position of first switching angle, p1/q1 for various Mf at two Mavalues 0.4 and 0.8. Influence of Mf over the switching angles for Mf value above 20 is negligible while for the range below 20 it largely depends on Mf. Both SPWM and ISCPWM upshots nonlinear relationship in the lower Mf range. Fig. 7 shows the variation of duty cycle for different Mawith constant Mf. The figure demonstrates that duty cycle is higher for ISCPWM throughout the entire range of Maand the austere linear relationship of duty cycle in SPWM is violated in ISCPWM for lower values of Ma. In addition, in ISCPWM causes Mf dependency of duty. The ISCPWM gives higher duty cycle without any pulse dropping at given modulation index while makes the dependency a little non-linear. Fig. 8 shows that the dependence of duty cycle on Mf at any Ma value is a constant for even the lowest typical carrier frequency of application.

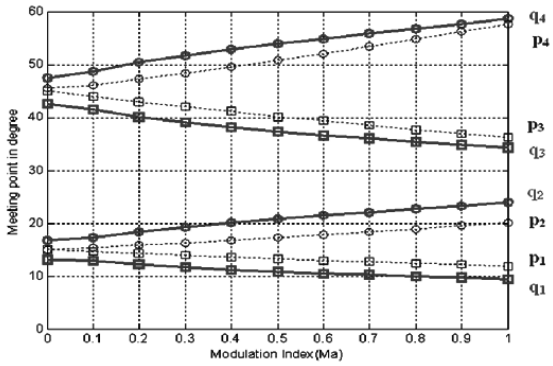


Figure 5 Influence of Ma on different switching angles

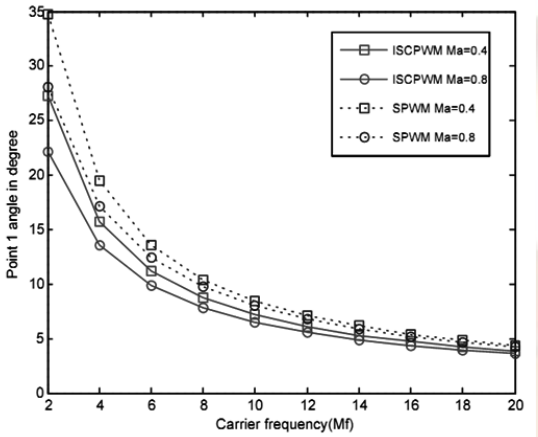


Figure 6 Position of first switching angle

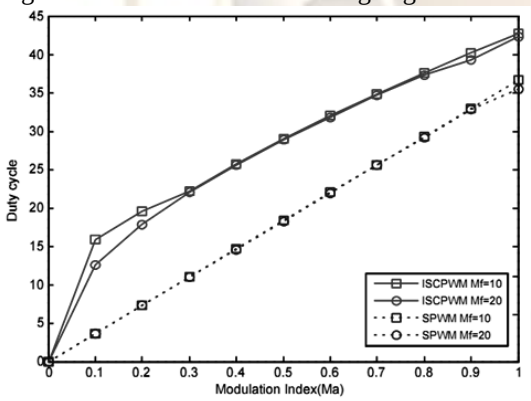


Figure 7 Variation of duty cycle for different Ma with constant Mf

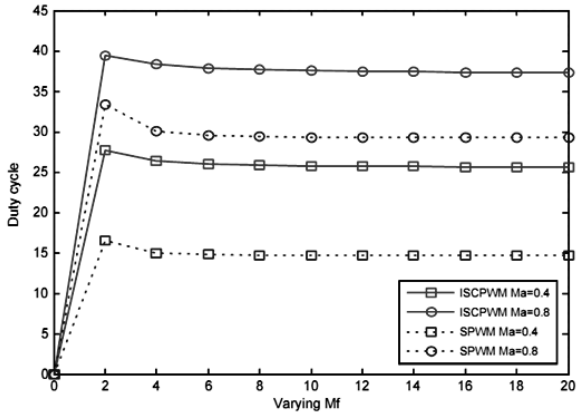
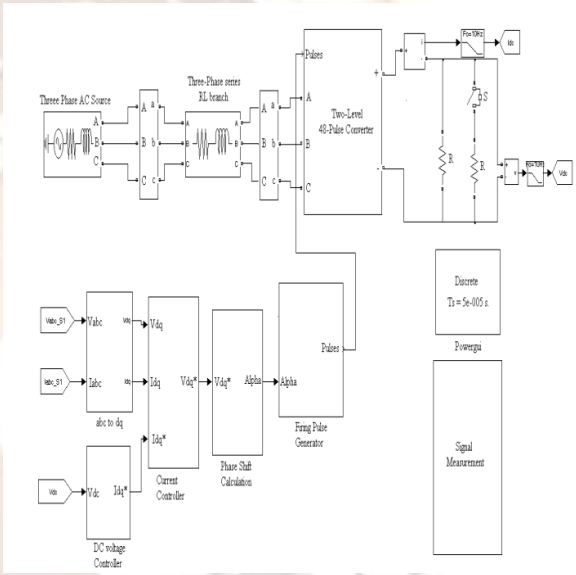


Figure 8 Dependence of duty cycle on Mf at any Ma value

IV. CONTROL SCHEME



The objective of the control algorithm of VSC is to maintain the DC voltage at the given reference value and to control the active power flow from AC grid to DC side, along withsupplying required reactive power to the AC mains. A set of capacitors is used at the DC bus to support the DC bus voltage at the required value to make the real power balance between the two sides of the converter, which is most important for the successful operation of the VSC based HVDC system. The stored energy in the capacitors reduces or increases if theactive power is not balanced between two sides of converter stations. It consists of two controllers, one is the DC voltage controller and other one is the current controller

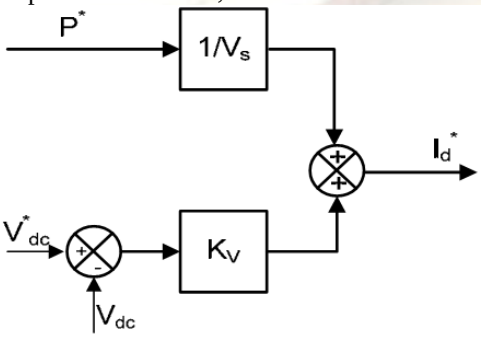
A. DC Voltage Controller

The DC voltage control is shown in shown in Fig. in which reference currents (id*, iq*) are achieved by the DC voltagecontroller from the reference real power and reference DC voltage as given below.

$i^*d = (P^*/Vs) + KV (V^*dc - Vdc)$ ……(a)

i*q = (Q*/3Vs) …….(b)

Where P* is the reference real power to be transmitted from one side to another side, KV is proportional gain constant, Vsisrms supply voltage, and V*dcis reference DC voltage. The reference value of the reactive current (Iq) is supplied directly to the inner current loops and is regulated equal to zero in this study. The first term in (2) decides the power flow in the system and second term achieves DC voltage regulation by means of controlling the additional amount of active power flowing from AC side to DC side. When Vdc is lower than the V*dc,then i*dis increased as shown in (2), so that a small amount of additional active power flows into the DC link capacitor through rectifier, thus Vdc rises up to V*dc . When Vdcis higher than the V*dc,then i*dis decreased so that an amount of active power flows into the DC link capacitor is reduced, thus Vdc is lowered to V*dc.



B. Decoupled Current controller

The decoupled current controller shown in Fig. The output of the DC voltage controller is fed to the current controller. The voltage and current relation of the converter is given by

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - \begin{bmatrix} v_{1a} \\ v_{1b} \\ v_{1c} \end{bmatrix} = (R + L_1 \frac{d}{dt}) \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \quad \text{……(c)}$$

Three phase to two phase transformation can be applied to (c)

AsHere v1d, v1q are the d-axis and q-axis components of v1, while id, and iq are the d-axis and q-axis components of is. vd is the d-axis component of vs whereas vq is always zero because the supply voltage vector is aligned with the d-axis. The instantaneous active power P, and the reactive power Q are drawn from the utility grid as

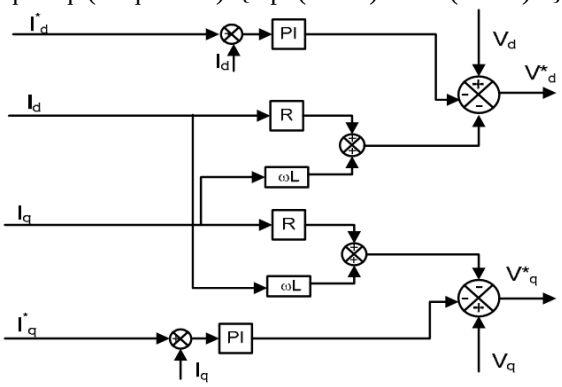
P = vd.id + vq.iq …….(d)

Q = vd.iq - vq.id …….(e)

The control of id and iqdecides P and Q independently. This decoupled current control is applied to the system in order to achieve an independent control of id and iq. The AC voltage commands in the d and q axes, are as vd*, and vq*. The inner current controller includes a feedback PI-controller. The reference currents (id*, iq*) from dc voltage controller are given as inputs to the current controller, and these provide reference voltages (vd*, vq*). The operation of the current controller can be explained by using (e) and (f) as

vd*=vd–(R.id+ZL.iq)–{Kp1(id*-id)+KI1∫ (id*-id)dt}

vq*=vq–(R.iq+ZL.id)–{Kp2(id*-id)+KI2∫ (id*-id)dt}



Where Kp1 and Kp2 are proportional gain, KI1 and KI2areintegral gain, id, vd and vq are d-q values of supply voltage vs,and id, iq are d-q values of the supply current (is).Here id* and iq* are the current commands in the d and q axes.

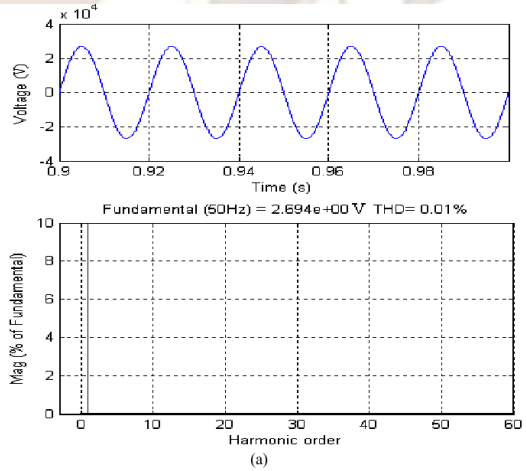
The first and second terms of the right hand side cancel the steady state voltage appearing across the AC-link inductor L1.The third term constitutes feedback control loops of the currents id and iq. The phase shift is calculated by using the (g) as

$$\delta^* = \tan^{-1}\left(\frac{v_q^*}{v_d^*}\right)$$

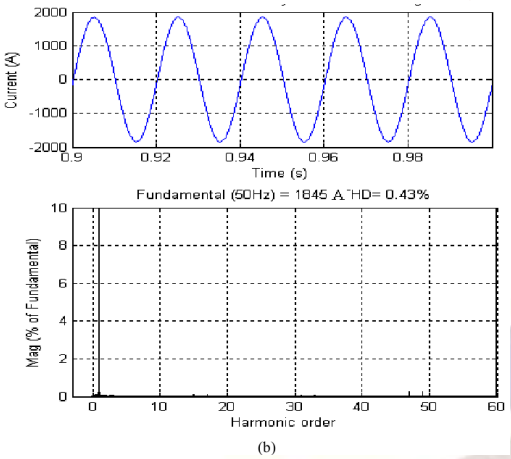
Where δ* is the angle at which the converter devices are gated.

It is the phase shift angle from the fundamental supply voltage.

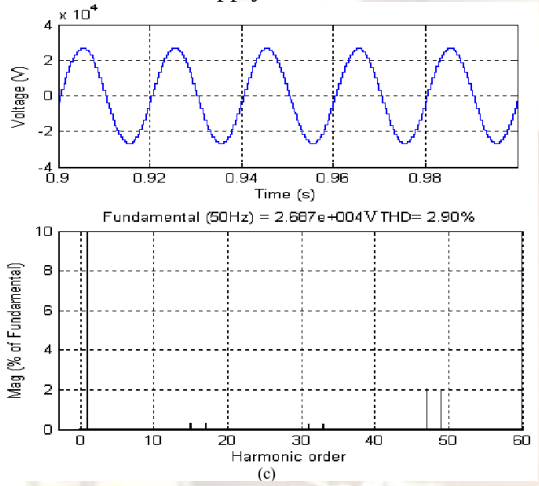
V. SIMULATION AND RESULT



Supply voltage



Supply current



Converter voltage

VI. CONCLUSION

A 48-pulse three-level voltage source converter has been designed, modeled and controlled for back-to-back HVDC system. The transformer connections with appropriate phase shift have been used to realize 48-pulse converter along with a control scheme using a set of three level twelve pulse converters. The operation of the designed converter configuration has been simulated and tested in steady sate and transient conditions which have demonstrated the quite satisfactory converter operation. The characteristic harmonics of thesystem has also improved by the proposed converter configuration.

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