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High Speed and Low Power Dynamic Latched Comparator for Air Craft Application

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ABSTRACT

Comparators are basic building elements for designing modern analog and mixed signal systems. Speed and resolution are two important factors which are required for high speed applications. This paper presents a design for an on-chip high-speed dynamic latched comparator for high frequency signal digitization. The dynamic latched comparator consists of two cross coupled inverters comprising a total of 9 MOS transistors. The measured and simulation results show that the dynamic latched comparator design has higher speed, low power dissipation and occupying less active area compared to double tail latched and pre-amplifier based clocked comparators. These comparators are used in aircraft applications. The simulation results of three comparators show that the dynamic latched comparator will occupy less active area and also having higher speed and consumes less power. So by using the dynamic latched comparator in the application of aircraft is more efficient when compared to other two comparator designs. The comparator schematics and corresponding layouts are implemented using spice tool.

Keywords – **Double Tail Latched Comparator,** Dynamic Latched Comparator, **digitization, on-chip, Pre-amplifier based comparator**

1. INTRODUCTION

The comparator compares the voltages that appear at their inputs and outputs a voltage representing the sign of the net difference between them. The comparator is a circuit that compares an analog signal with another analog signal or reference and outputs a binary signal based on the comparison. If the +, VP, the input of the comparator is at a greater potential than the -, VN, input, the output of the comparator is a logic 1 and vice versa. Comparators are important elements in modern mixed signal systems. Speed and resolution are two important features which are required for high speed applications such as on-chip high frequency signal testing, data links, sense amplifiers and analog-to-digital converters. On-chip testing of high frequency pseudo random binary sequences (PRBS) requires a high speed comparator at the electrical interface stage [1], [2].

A clocked comparator generally consists of two stages. In that first stage is to interface the input signals. The second (regenerative) stage consists of two cross coupled inverters, where each input is connected to the output of the other. In a CMOS based latch, the regenerative stage and its following stages consume low static power since the power ground path is switched off either by a NMOS or PMOS transistor [10].

In many applications comparator speed, power dissipation and number of transistors are more important. If comparator speed is a priority, the regenerative stage could be designed to start its operation from midway between power supply and ground [6], for example, pre-amplifier based clocked comparator [4].

However, the static power consumption is relatively high. If comparator was designed with priority given to power reduction, then number of transistors increases thereby reducing the speed, for example double tail latched comparator[4].

Comparator design largely depends on the target application. However, an input-referred latch offset voltage (hence offset voltage), resulting from the device mismatches such as threshold voltage V_{th}, current factor β (=μ*CoxW/L)* and parasitic node capacitance and output load capacitance mismatches, limits the accuracy of such comparators [8], [9].

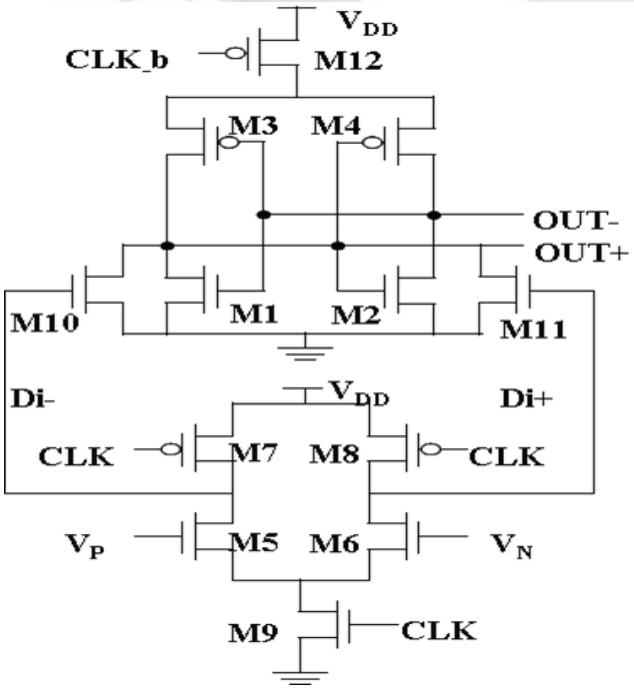
In this paper, we present a design of high-speed and low power dissipating clocked comparator for aircraft applications. This comparator is attractive for the applications where both speed and power consumption is of the highest priority.

The rest of the paper is organized as follows. The speed and power limitations of the double tail latched, pre-

amplifier based clocked comparators design and areas for improvements are investigated in Section II. An overview of the dynamic latched comparator design is given in Section III. Application of dynamic latched comparator in aircraft was given in Section IV. The simulation results, comparisons are given in Section V.

2.DOUBLE TAIL LATCH AND PREAMPLIFIER BASED CLOCK COMPARATORS

The circuit and schematic diagrams of the comparator presented in [3] are shown in Fig. 1. This comparator is compared with dynamic latched comparator design because of its speed and suitability for low supply voltage applications. It operates in 2 phases 1)Reset phase 2)Regeneration phase .While the clock is low(reset phase), M7 and M8 transistors are ON. M9 transistor is off. As M7 and M8 transistors are ON Di+ and Di- nodes are pre-charged to Vdd. So M10 and M11 become ON and discharge the output nodes OUT+ and OUT- to ground. While the clock is high (regeneration phase), M9 and M12 transistors are in ON condition. M7 and M8 transistors are in OFF state. So Di nodes start discharging as M9 is ON. The difference between voltages of Di+ and Di- (ΔVDi) are given to M10 and M11 transistors. As Di nodes starts discharging, M10 and M11 are initially in ON condition and gradually M10 and M11 becomes OFF. Output nodes OUT+ and OUT- starts regenerating when M10 and M11 are unable to ground the outputs. The intermediate stage formed by M10 and Mll passes ΔVDi to the cross-coupled inverters and also provides additional shielding between the input and output, with less kickback noise as a result[8].



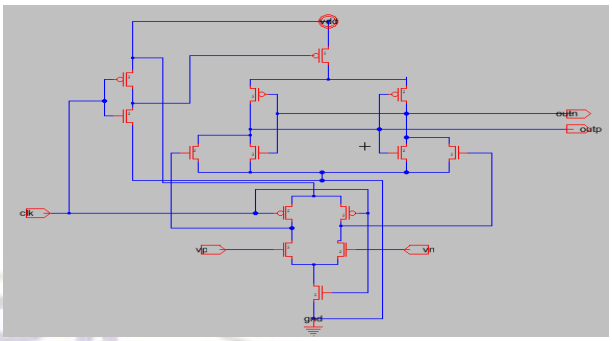


Fig 1 Circuit diagram and Schematic of double tail latched comparator

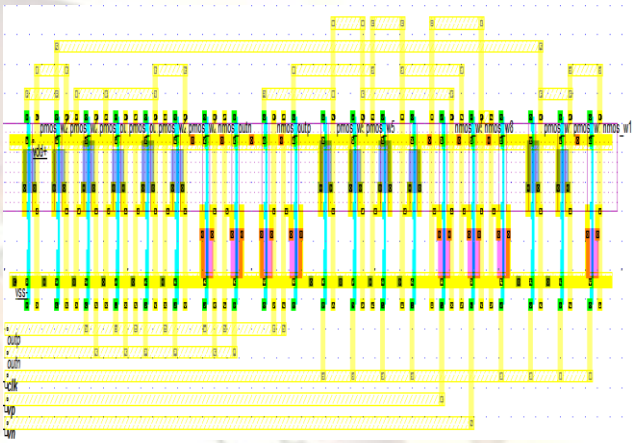


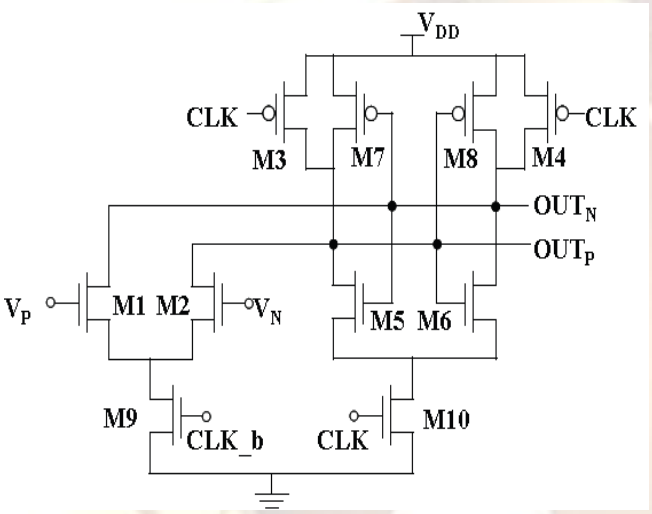
Fig 2 Layout of double tail latched comparator

The pre-amplifier based clocked comparator is composed of two stages as shown in Fig. 3. The first stage is the amplification stage, which consists of the transistors M1–M4 and M9. More practically, the input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output latch stage. It can amplify a small input voltage difference to a large enough voltage to overcome the latch offset voltage. The second stage is the regenerative stage that is comprised of the transistors M5–M8 and M10. The circuit works in two phases, namely the amplification phase and the regenerative (evaluation) phase. When the clock (CLK) is low (amplification phase), the tail transistor M9 turns ON and M10 turns OFF. When CLK is LOW only amplification stage works here. In addition, the amplification stage is designed to produce its output close to VDD-|Vthp| which can effectively reduce the charging time. In this stage Vp-Vn is amplified and fed to regenerative stage. When the clock (CLK) is high (regeneration phase), M10 turns ON and M9 turns OFF. Only regenerative stage works here.

There is a reduction of the delay time in the pre-amplifier based clocked comparator over the double tail latched comparator. But the pre-amplifier based clocked comparator uses an amplification stage, it consumes static

power during the amplification period and hence the energy consumption in the pre-amplifier based clocked comparator becomes higher than the double tail latched comparator. However, the preamplifier based comparators suffer not only from large power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain-to-source resistance rds due to the continuous technology scaling

There is a reduction of the power dissipation in the double tail latch comparator over the pre-amplifier based clocked comparator. In order to avoid these drawbacks in double tail latch and pre-amplifier based clocked comparators, dynamic latched comparator was introduced in the subsequent section.



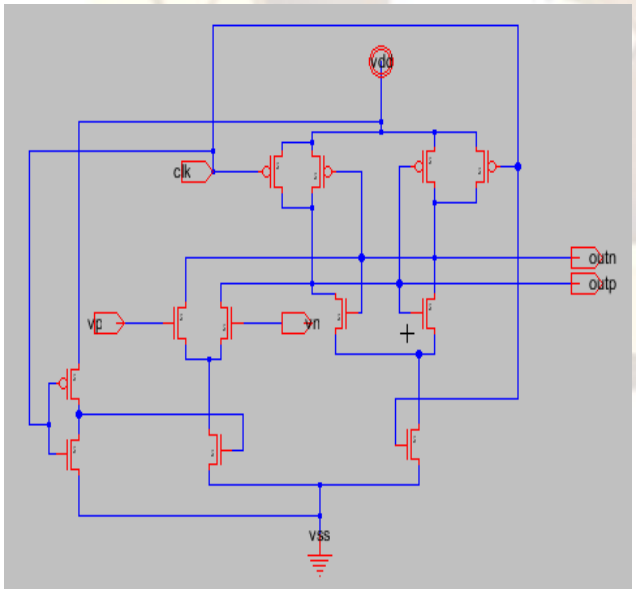


Fig 3 Circuit diagram and Schematic of pre-amplifier based clocked comparator

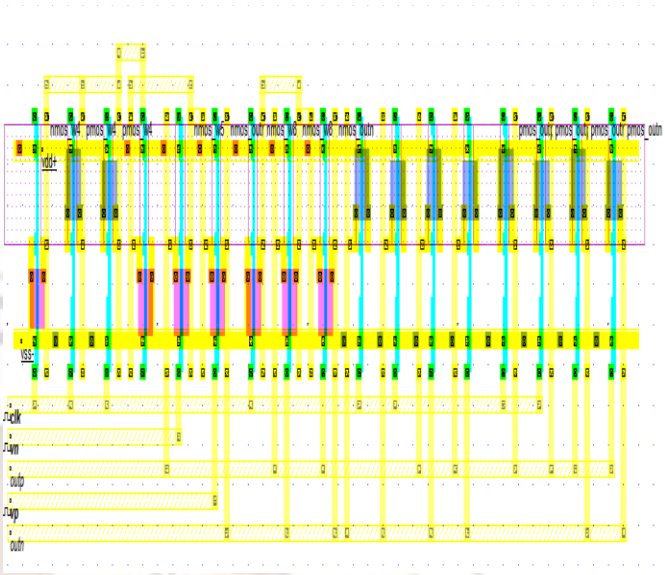


Fig 4 Layout of pre-amplifier based clocked comparator

3. DYNAMIC LATCHED COMPARATOR

The dynamic latched comparator is composed of two stages as shown in Fig. 5. The first stage is the interface stage which consists of all the transistors except two cross coupled inverters. The second stage is the regenerative stage that is comprised of the two cross coupled inverters, where each input is connected to the output of the other. It operates in two phases.1) Interface phase and 2) Regeneration phase. It consists of single nmos tail transistor connected to ground. When clock is low tail transistor is off and depending on Vp and Vn output reaches to VDD or gnd. When clock is high tail transistor is on and both the outputs discharges to ground.

There is reduction of both power and delay in dynamic latched comparator circuit over the double tail latched and pre-amplifier based clocked comparators. Double tail latched comparator has less power consumption but low speed because of more transistor count and pre-amplifier based clocked comparator has high speed because of less transistor count but power consumption is more because it uses an amplification stage, it consumes static power during the amplification period However, since the pre-amplifier based clocked comparator is to work at high frequency, the energy consumption of the pre-amplifier based clocked comparator becomes comparable to the double tail latched comparator. Hence the performance of the pre-amplifier based clocked comparator is limited by the static power dissipation in the evaluation or regeneration phase.

Due to fast speed, low power consumption, high input impedance and full-swing output, dynamic latched comparators are very attractive for many applications such as high-speed analog-to-digital converters (ADCs), memory

sense amplifiers (SAs) and data receivers. They use positive feedback mechanism with one pair of back-to-back cross coupled inverters (latch) in order to convert a small input-voltage difference to a full-scale digital level in a short time.

Thus dynamic latched comparator is suitable for both high speed and low power dissipation because of decrease in transistor count which overcomes the problem of double tail latch and pre-amplifier based clocked comparators.

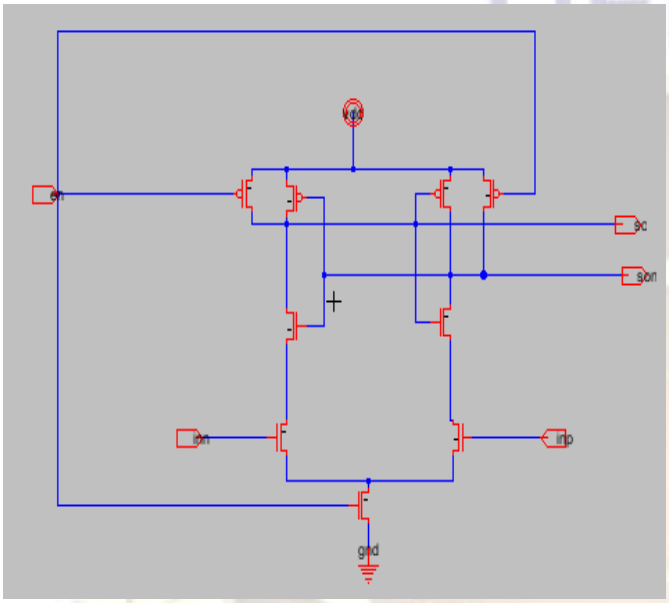


Fig 5 Schematic of Dynamic latch comparator

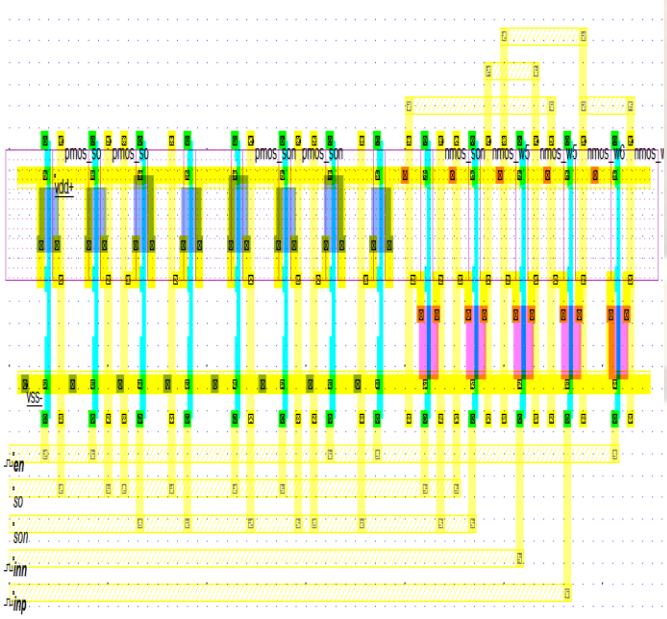


Fig 6 Layout of dynamic latch comparator

TABLE I

Comparison of 3 Clocked Comparators

Clocked Comparator	Transistor count	Voltage(v)	Power(mw)	Delay(ns)
Double tail Latched comparator	12	1.2	0.006	0.038
Preamplifier based clocked comparator	10	1.2	0.269	0.014
Dynamic latched comparator	9	1.2	0.003	0.011

Since the comparator offset [11] can be reduced by using known techniques [3], the main focus of this paper is the comparator speed and power dissipation. Simulation comparing the delay versus the supply voltage and power dissipation versus the supply voltage of the comparator at 1.2V supply has been done. The results show that the dynamic latched comparator outperforms the other 2. Hence the 3 comparators will be compared. The layouts are automatically extracted and simulated with a microwind simulator. Fig. 16, 17 shows simulation results of the power dissipation, delay versus supply voltages (V_{dd}) respectively for the 3 designs. The results show that the dynamic latched comparator circuit has less delay time and less power dissipation than the other 2 designs.

As in the dynamic latched comparator circuit design, both the power dissipation and delay will be less as shown in table1. This makes the dynamic latched comparator circuit more attractive for the low power and high speed applications such as SAPTL [5], [13], [14] and aircraft.

4. APPLICATION

Both double tail latched and preamplifier based clock comparators and dynamic latched comparator can be used in the application of aircraft [12] to check whether the aircraft was flown outside its performance. If the aircraft was flown outside its performance no sudden damage may occur but its structure might be permanently weakened.

3 conditions that are harmful for aircraft are

1) Exceeding maximum permissible speed Vne.

2) Extending flaps above flap limiting speed i.e. flaps must not be lowered if aircraft was going faster than Vfl.

3) Exceeding maximum acceleration Gmax.

The basic architecture and schematic of comparator based aircraft is shown in the Figure7. It consists of

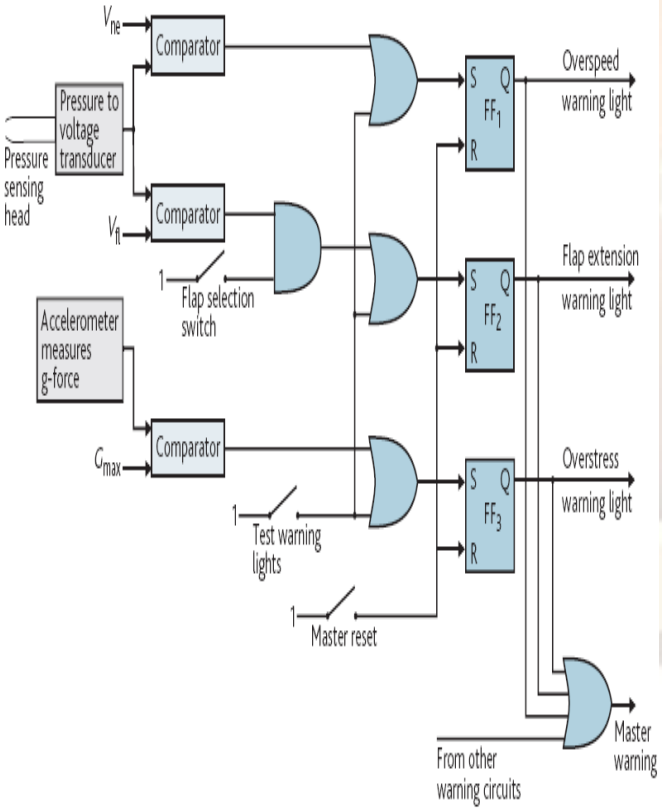
1) Comparator which was replaced with clocked comparator to perform comparison whenever it is clocked so that extra computations will be reduced and power consumption decreases, speed increases and area decreases because of less transistor count.

2) Transducers function is to

a) Convert acceleration or speed in to voltage.

b) Measure acceleration and speed.

3) RS flip-flop is mainly used for recording of short lived events.



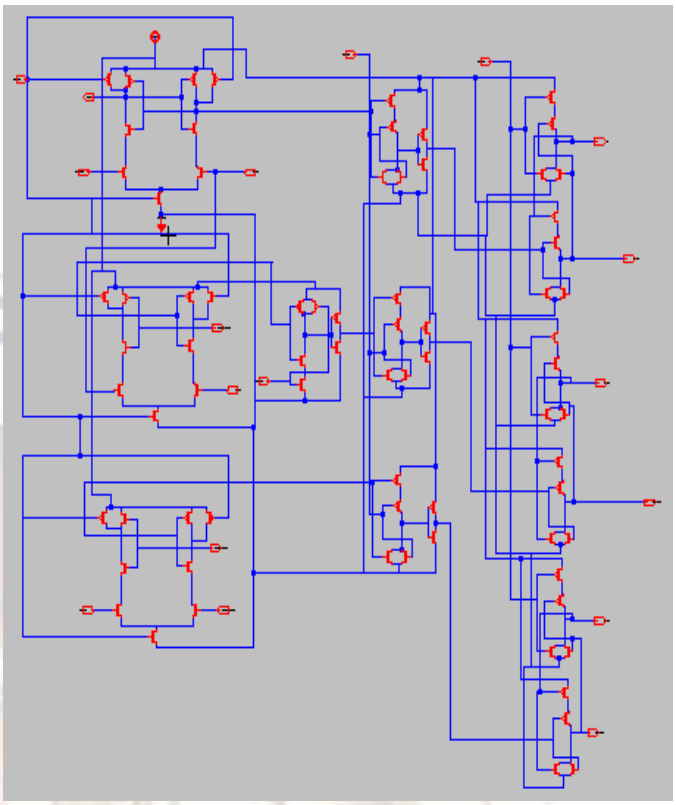


Fig 7 Architecture and Schematic of dynamic latch comparator based Aircraft

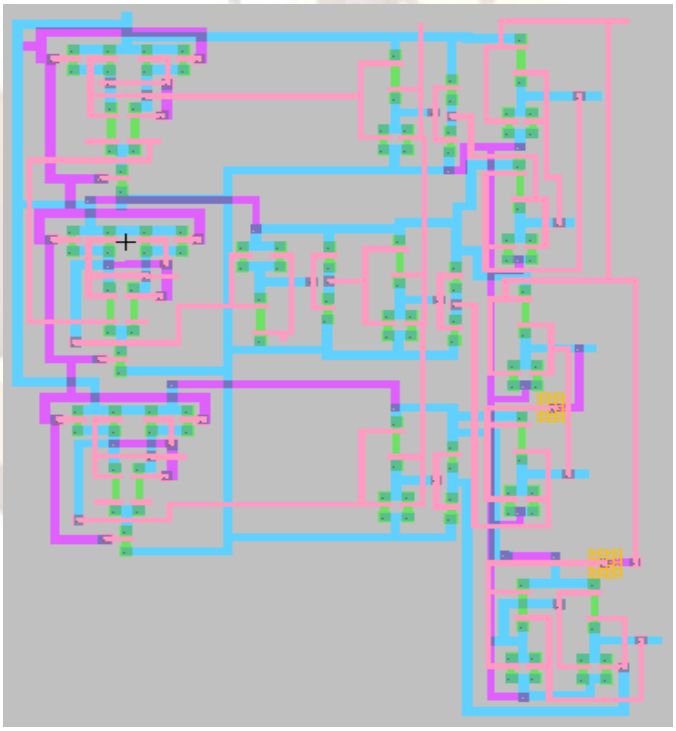
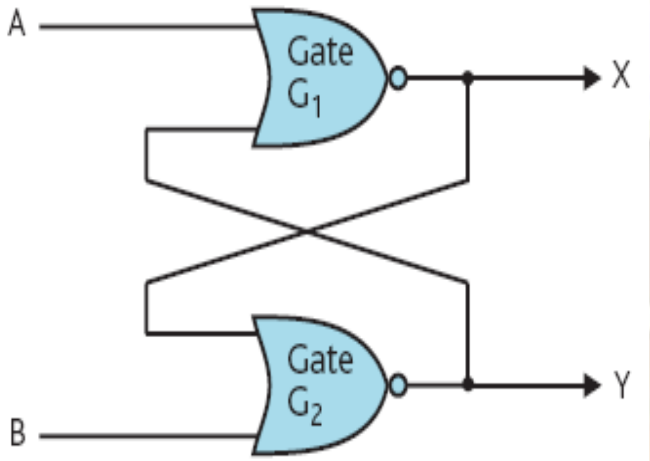


Fig 8 Layout of dynamic latch comparator based Aircraft

4.1 RS flip-flop:

The RS flip-flop consist of 2 NOR gates. Inputs are provided to the RS flip-flop and outputs are obtained after performing the logic function. Fig 9 shows the circuit and schematic of RS flip-flop that consists of cross coupled NOR gates. It can also be implemented by using cross coupled NAND gates.



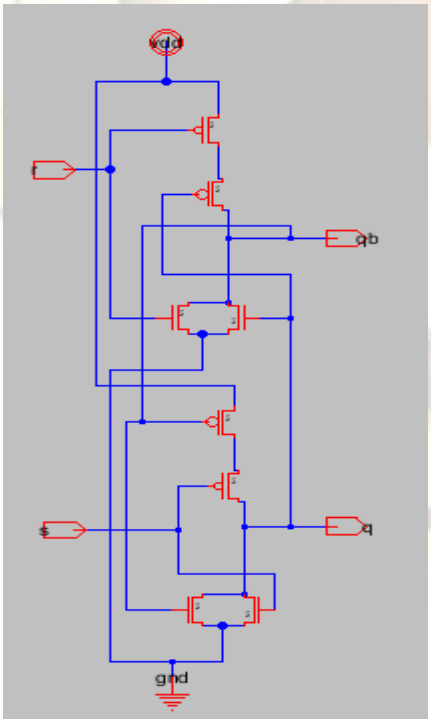


Fig 9 Circuit and Schematic of two cross-coupled NOR gates (RS flip-flop).

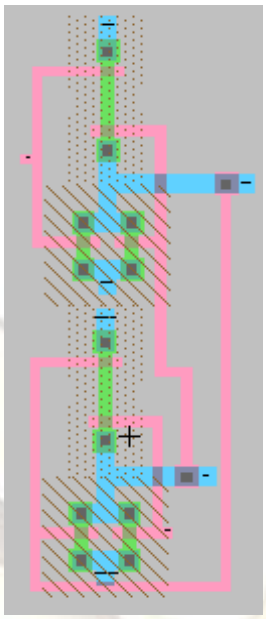


Fig 10 Layout of two cross-coupled NOR gates (RS flip-flop)

This RS flip-flop is different from combinational circuit that the gates are cross coupled and output of gate is fed back to its input. A, B(R, S) are inputs. X, Y (Q, Qbar) are outputs.

Boolean equations for NOR gate with inputs and outputs are:

$$1.\ X = \overline{A + Y}$$

$$2.\ Y = \overline{B + X}$$

Characteristic equation is one which can be obtained by analyzing its circuit. From truth table also we can derive characteristic equation. Truth table of RS flip-flop was shown in TableII.

TABLEII

Truth Table Of Nor Gate In Fig 9

A	B	Inv(A+B)
0	0	1
0	1	0
1	0	0
1	1	0

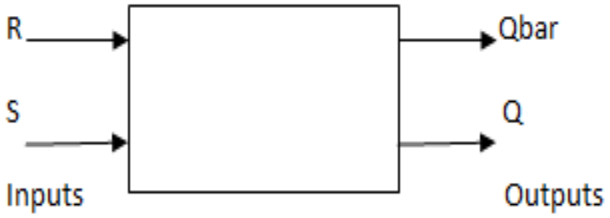


Fig.11 Circuit representation of the RS flip-flop as a black box

TABLEIII

Truth Table for the Rs Flip-Flop

Inputs		Output	Description
R	S	Q+	
0	0	Q	No change
0	1	1	Set output to '1'
1	0	0	Reset output to '0'
1	1	X	Forbidden

4.2. Building of RS flip-flop from NAND gates

RS flip-flop can also be constructed from cross coupled NAND gates instead of NOR gates as shown in fig 12. Only difference between NAND and NOR gate flip-flop is that inputs to NAND gate are active low.

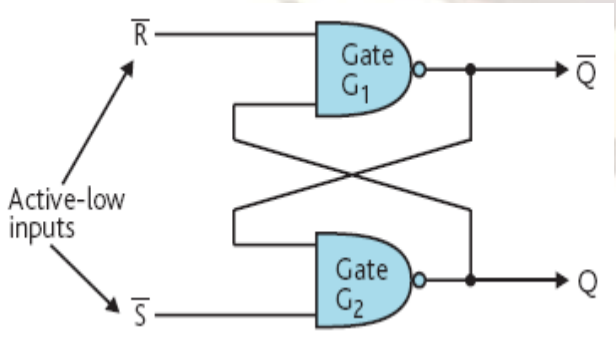


Fig12 RS flip-flop constructed from two cross-coupled NAND gates

TABLEIV

Truth Table For An Rs Flip-Flop Constructed From Nand Gates

Inputs		Outputs	Comment
R	S	Q+	
0	0	X	Forbidden
0	1	1	Reset output to '0'
1	0	0	Set output to '1'
1	1	Q	No change

Problem arises when initial R, S=0, 0 and changes to R, S=1, 1(No change). In practical applications the gate that provides simplest solution will be used. In most applications we use NAND gate RS flip-flop because in most circuits active low signals are used.

4.3. Clocked comparator

In fig7 comparator was used to compare transducer output with aircraft speed limit. If we place any of the 3 clocked comparators in place of comparator, it is useful to perform 2 operations depending on clock.

a) To compare the Vne and Vfl voltages with voltage Vtr from transducer.

b) To compare the Gmax (gmax) with gforce (atr) measured by accelerometer

As shown in Fig 7, when transducer output exceed voltage limits Vne and Vfl of aircraft last recording of event must be made and the output of comparator will be '1', otherwise output will be '0'. Warning lights are used here if any of 3 limits are exceeded.

Output of 2nd comparator is ANDed with flap actuator circuit signal from flap selection switch (fss) that provides '1' when flaps are down. Comparator outputs are sent through OR gate and then given to 's' input of RS flip-flop. Test warning light (twl) is used to check whether all warning lights are working or not.

Assume that initially 'Q' output of flip-flop is '0' when R='1' and S='0'. When R='0' and S='1' then 'Q' output reaches to '1'. 'Q' output remains '1' until 'R' input resets 'Q'. RS flip-flop was found in indicator circuit.

In the same way when switching ON the system if we provide Master Reset (mr) as '1' to all RS flip-flops then all the flip-flops will be in RESET condition. Alarm will be triggered if any one of the's' input is set to '1'.

If we use double tail latched comparator power consumption will be less but delay will be more and if we use preamplifier based clock comparator delay will be less but power will be more because of more static power consumption. So we use dynamic latched comparator in aircraft application which has both less delay and less power consumption.

In case of clocked comparator applications such as clocked comparators based aircraft, dynamic latched comparator based aircraft has less delay time and less power consumption than the other two comparators based aircrafts because of less transistor count.

5. SIMULATION RESULTS

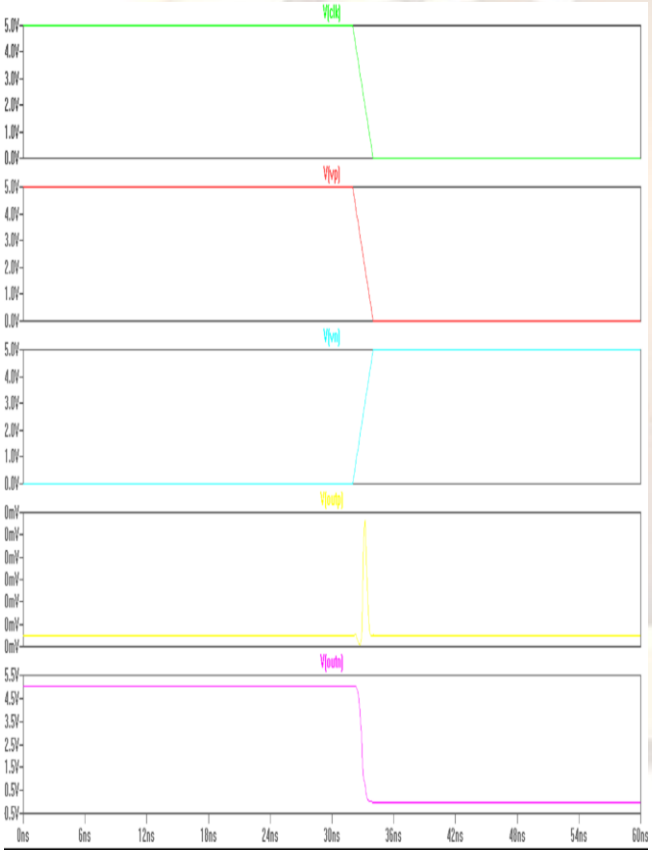


Fig 13 Waveforms of double tail latched comparator

In fig 13 double tail latched comparator compares 2 .inputs, when inputs 'vp' > 'vn', then output will be 'outn' > 'outp' ('clk'='1').

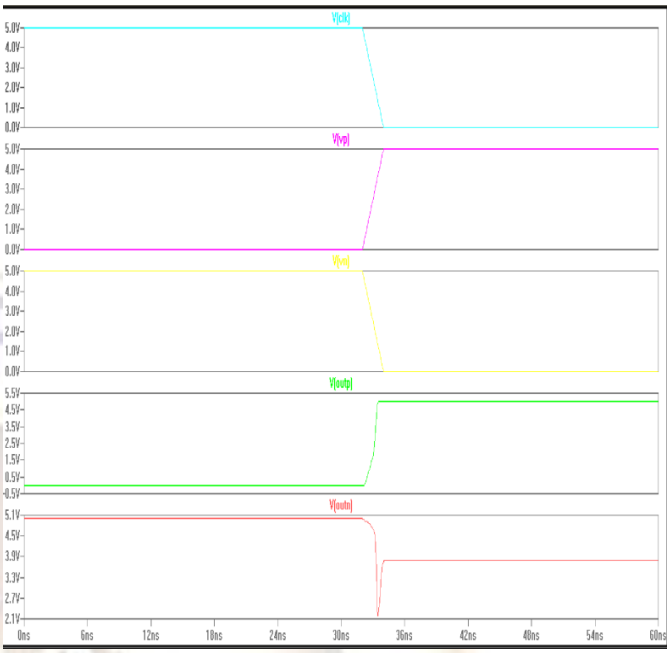


Fig 14 Waveforms of pre-amplifier based clocked comparator

In fig 14 pre-amplifier based clocked comparator compares 2 inputs, when inputs 'vp' < 'vn', then output will be 'outp' < 'outn' ('clk'='1').

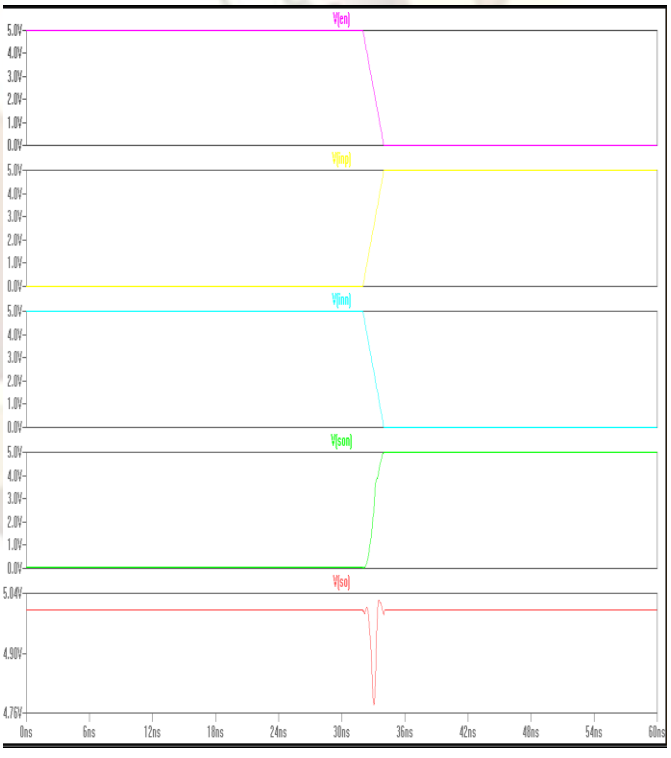


Fig 15 Waveforms of dynamic latched comparator

In fig 15 dynamic latched comparator compares 2 inputs, when inputs 'inp' < 'inn', then output will be 'son' < 'so' ('en'='1').

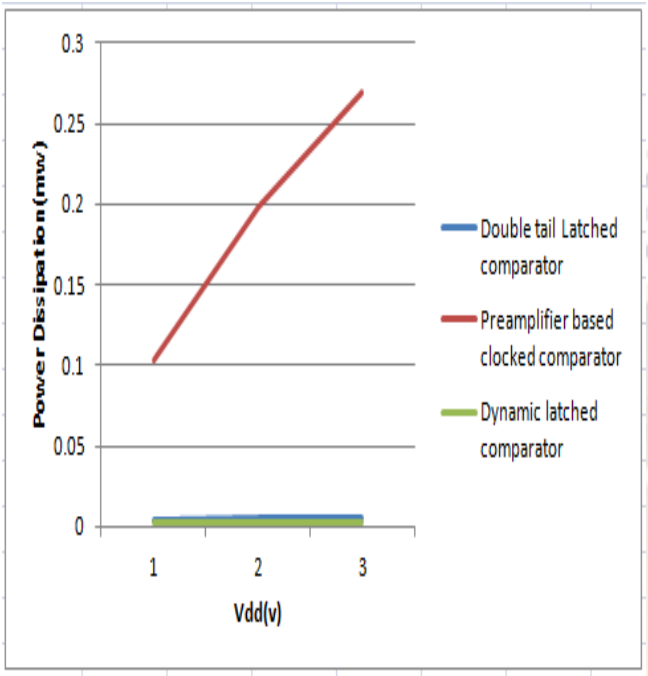


Fig 16 Comparison of Power Dissipation of the three clocked comparators

Fig 16 shows that preamplifier based comparator has more power dissipation than double tail latched comparator because of static power consumption. Dynamic latched comparator has less power consumption than the double tail latch and pre-amplifier based clocked comparators.

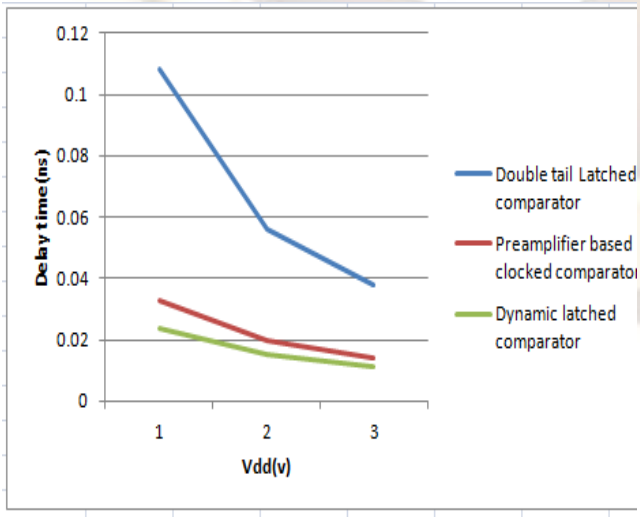


Fig 17 Comparison of delay time of comparators

Fig 17 shows that dynamic latched comparator has less delay time than the double tail latch and pre-amplifier based clocked comparators.

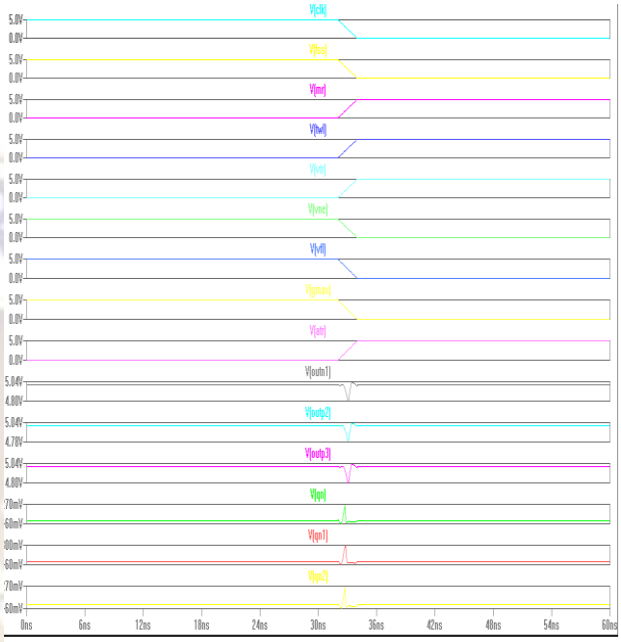


Fig 18 Waveforms of aircraft using dynamic latch comparator (when vtr < (vne, vfl) and atr < gmax)

Fig 18 shows that when transducer output (Vtr) is less than aircraft limits (Vne, Vfl) then there is no hazard and the aircraft warning lights (qn, qn1, qn2) will be low.

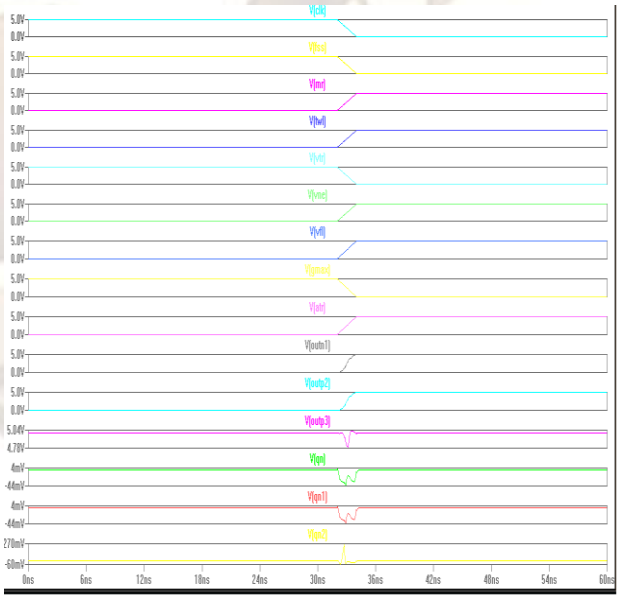


Fig 19 Waveforms of aircraft using dynamic latch comparator (when vtr > (vne, vfl))

Fig 19 shows that when transducer output (Vtr) is greater than aircraft limits (Vne, Vfl) then there is hazard and the aircraft over speed, flap extension warning lights (qn, qn1) will be high.

Fig 20 Waveforms of aircraft using dynamic latched comparator (when atr > gmax)

Fig 20 shows that when accelerometer output gforce (atr) is greater than aircraft limits Gmax (gmax) then there is hazard and the aircraft overstress warning light (qn2) also reaches high state. (Here also Vtr > (Vne, Vfl))

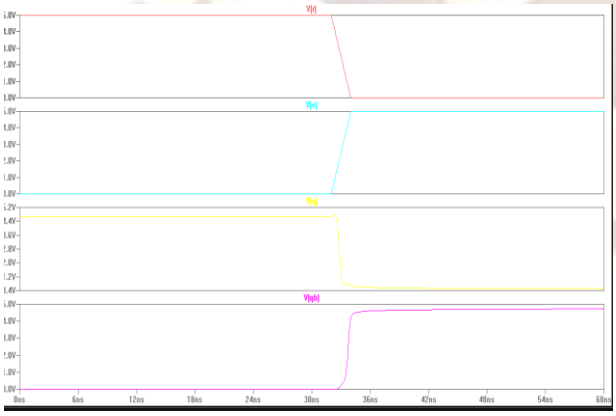


Fig 21 Waveforms of RS flip-flop

6. CONCLUSION

Dynamic latched comparator was designed that works with high speed and low power consumption when compared to double tail latched comparator and pre amplifier based clocked comparator. For comparison we provide analog input to the comparator and the output will be digital. The simulation results show that the proposed circuit can operate at higher speed with low power dissipation than the other two comparators. Similarly in case of clocked comparator applications such as clocked comparators based aircraft, dynamic latch comparator based aircraft has less delay time than the other two comparators based aircrafts. Clocked comparator schematics are implemented in spice and the corresponding layouts are implemented using microwind tool. Dynamic latched comparator based aircraft, RS flip-flop schematic and corresponding layouts are implemented in spice.

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