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# Design and Performance Analysis of Analog Sub circuits for Multiplying DAC used in Image Compression

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## ABSTRACT

**Image compression is one of the prominent signal processing areas for multimedia applications. Compressed images when transmitted are affected by noise and thus reconstruction of images at the receiver becomes complex. Very recently Artificial Neural Networks are being used for image compression and decompression. One of the building blocks in ANN is the multiplying DAC. In this paper, we present the design and analysis of sub circuits for multiplying DAC using 180nm CMOS technology. The DA, current reference and op-amp are design, modelled and analysed for its performances using Cadence Virtuoso and HSPICE. The optimum geometries for sub circuits are computed and schematic captured is carried out. The results obtained show that the designed sub circuits are suitable for multiplying DAC implementation.**

*Keywords* - **Multiplying DAC, Artificial Neural Networks, Synapse**

## I. INTRODUCTION

**V**LSI neural networks are becoming more popular because of providing real-time solutions to many real world problems [1]. The Artificial Neural Networks (ANNs) are inspired by biological learning systems.

Typically a human brain consists of $10^{11}$ neurons each with an average of $10^3$ to $10^4$ connections. It indicates that the computing speed of the brain is said to be the parallel and distributed computing performed by the neurons. The communication between neurons through synapse is very complicated chemical process where in specific transmitter substances are released from sending side of the synapse [2].

Neural Networks are built of very complex network of web of neurons which are interconnected to each other. The first artificial neuron was the Threshold Logic Unit (TLU) proposed by Warren McCulloch and Walter Pitts in 1943.

They are two critical issues in analog neural networks they are weight storage and multiplication [3]. The multiplication plays very vital role in realizing a neural network and this is commonly known as "synapse". Their role is to multiply an input current with binary coded digital weights as shown in fig: 1. several research attempts to implement synapses. Some use numeric implementation whereas others use analog circuit. Each is having its own advantage and disadvantage. Numeric multipliers are used where high accuracy is needed and analog multipliers are used where an efficient area and high frequency is needed [2].

Storage of weights can do by either analog or digital circuit techniques. Analog weight storage is

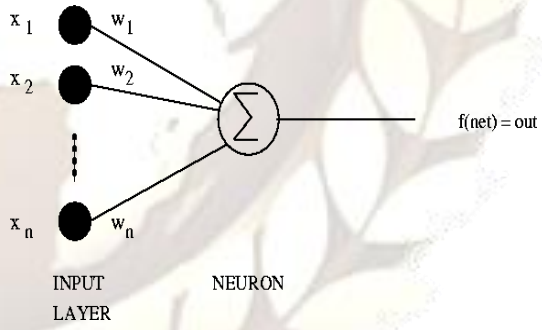



**Fig 1: An Artificial Neuron**

$$\text{Out} = \sum_{i=1}^{n} x_i \; w_i \qquad (1)$$

Where

$x_i$ = input currents ;
$w_i$ = digital weights.

typically implemented by storing charge on a capacitor. This charge must be refreshed periodically and therefore requires additional programming

circuitry that is constantly operating. The floating-gate synapses offer an alternative to capacitive analog memory, but require special high-voltage programming circuitry on chip. Furthermore, additional feedback circuitry is usually required for accurate programming. These analog memories have an advantage of small layout area [3].

Digital weight storage has been less popular, but it has the advantage of a simple programming interface. Digital weights can be stored in all of the familiar digital memory structures: DRAM, SRAM, or EEPROM. Since all computation is performed in the analog domain, digital weights must be converted to analog signals through the use of DACs [4]. However, efficient weight storage and multiplication are important design challenges which must be addressed in analog neural network implementations.

In this paper we described a synapse circuit that integrates the weight storage and multiplication into single, compact Multiplying Digital-to-Analog Converter (MDAC) circuit.

## 2. MDAC Synapse

Ryan and D. Beer proposed MDAC synapse with compact current-mode circuit which multiplies an input current by a digital weight [3].

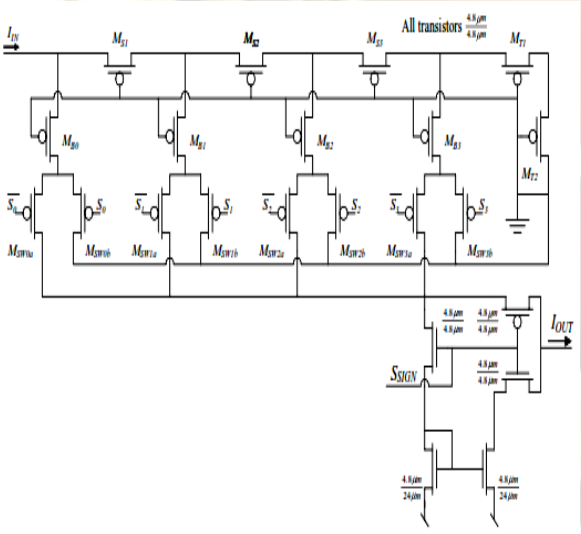



**Fig 2: Circuit diagram of 5-bit R-2R PMOS MDAC [3]**

The circuit diagram of R-2R PMOS based MDAC is shown in Fig 2. The operation of the circuit is based on the familiar *R*-2*R* resistive current divider. Here PMOS transistors are used in place of poly-silicon resistors to save chip area [3].

Vittoz and Arreguit introduced the concept of a pseudo Ohm's law for MOSFETs. Simply stated, a Network of MOSFETs sharing the same gate voltage is linear with respect to currents but not voltages. Further, the current through each transistor is determined only by its geometry. This allows one to borrow resistive current division networks and incorporate them directly into VLSI circuits without using large resistors [5].

The widths and lengths of each transistor are identical. The pseudo-resistance of a MOS transistor is determined only by its width-to-length ratio. The pseudo-resistance of each transistor is denoted by *R*. The specific value of *R* is not important. The 2*R* 'resistance' is provided by series combination of the switching transistor ($M_{SWxa}$ *or* $M_{SWxb}$) and the branch transistor ($M_{Bx}$).

Note that, here each branch at a time only one switching transistor will "ON", because the pair is driven with complementary signals. Therefore, each downward branch of the ladder provides a 'resistance' of 2*R* to ground. Negative weights are realized by directing the output current of the MDAC into an NMOS current mirror, reversing the current flow. An additional set of switching transistors controlled by a digital input, $S_{SIGN}$, is used to direct the output of the MDAC either through an NMOS mirror or directly to the output node

$$I_{OUT} = D * I_{IN} \quad (1)$$

$$D = (-1)^{S_{SIGN}} \sum_{i=0}^{3} \frac{S_i}{2^i} \quad (2)$$

From equation (2) it is clear that weight magnitudes are always less than one. So additional current gain may be added before or after the MDAC circuit if larger weights are desired. This is accomplished by increasing the size of the current mirror supplying $I_{IN}$ [3].

## 3. Design and Analysis of Sub Circuits for Multiplying DAC

The R-2R ladder MDAC is composed of an R-2R ladder network that performs as a current divider with the function the same as the weighted current sources play in the weighted current steering MDAC.

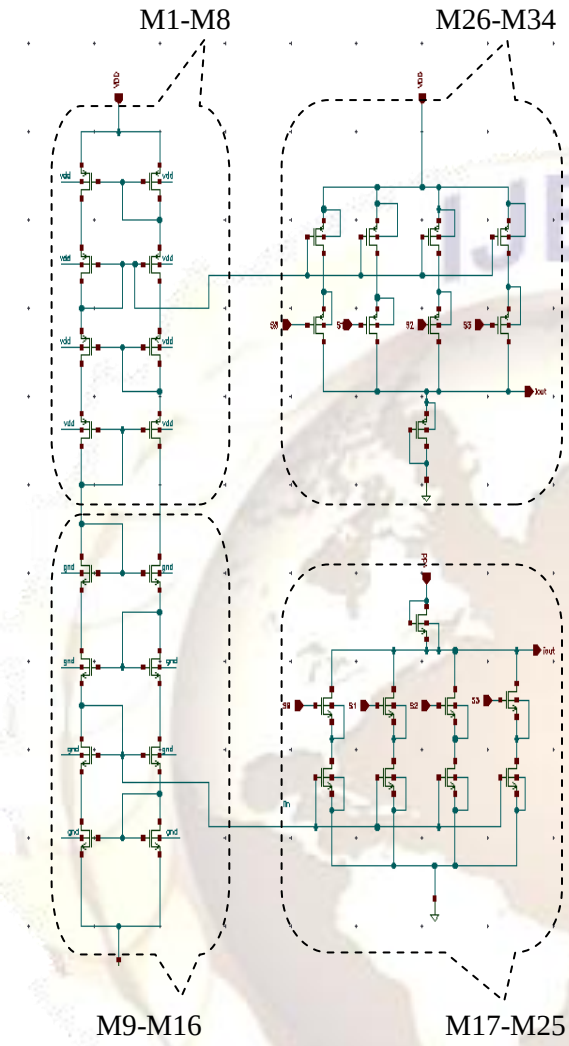



**Fig 3: Wilson based 4bit Weighted Current steering MDAC**

In this paper we design current reference circuit, differential amplifier and Op-Amp for MDAC. The Wilson based 4bit weighted current steering MDAC circuit is shown in Fig 3. In this circuit the transistors M1 – M16 acting as current reference circuit which was formed by cascading of no of Wilson current mirrors. The width and length of each transistors used for the reference circuit is given in Table (1),the transistors M17 – M25 is acting as NMOS based current steering circuit and M26– M34 is acting as PMOS based current steering circuit. The widths and currents that flow in each branch of NMOS current steering circuit are given in the Table 2. From the table we can understand the current doubles by doubling the geometric widths of successive transistors. The transistors M21 – M24 is used here is to assign the binary weights S0, S1, S2, S3 and M25 acting as load resistor to measure the total currents for different binary weights. The currents for different weights are practically measured and given in the Table 3 and its graph is given in Fig 7. When S0 S1 S2 S3= 0011 the total current at M25 is 18.99µA. similarly for S0 S1 S2 S3 =1010 current is 63µA. The output wave forms are shown in fig 5 and Fig 6.

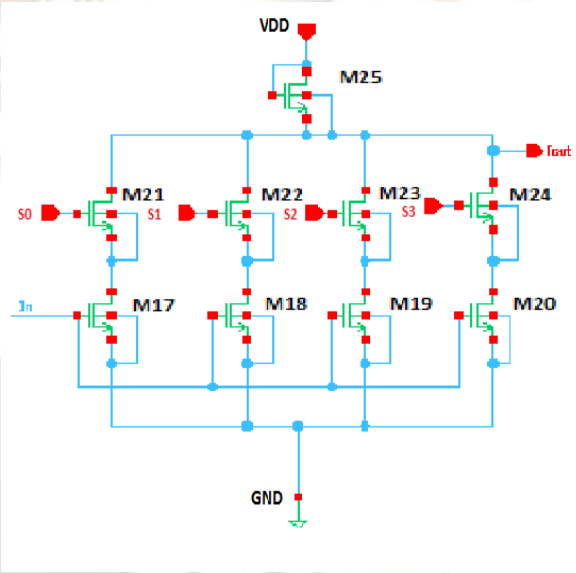



**Fig 4: 4bit Weighted Current steering MDAC**

**Table 1: Widths and Lengths of Current Reference Circuit**

| Transistor NO | Width | Length |
|---|---|---|
| M1- M8 (PMOS) | 24 mm | 0.36 µm |
| M9- M16(NMOS) | 5.5 mm | 0.36 µm |

**Table 2: Measured currents for different widths**

| Transistor NO | Width | Length | Current (Amp) |
|---|---|---|---|
| M17 | 0.822 mm | 0.36 µm | 50.436µ |
| M18 | 0.411 mm | 0.36 µm | 25.218µ |
| M19 | 0.205 mm | 0.36 µm | 12.609µ |
| M20 | 0.102 mm | 0.36 µm | 6.3045µ |

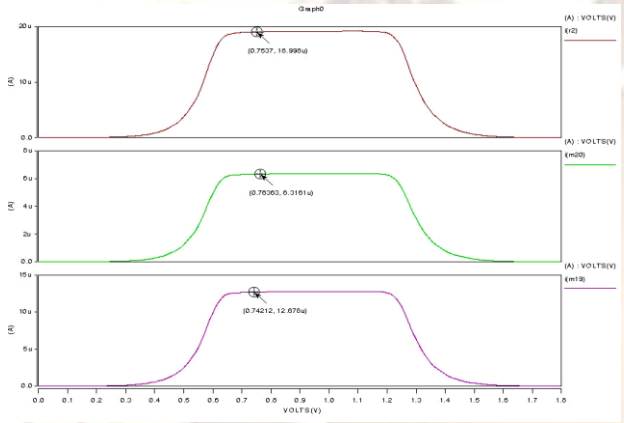


**Fig 5: Total current18.99µA for S0 S1 S2 S3 = 0011**

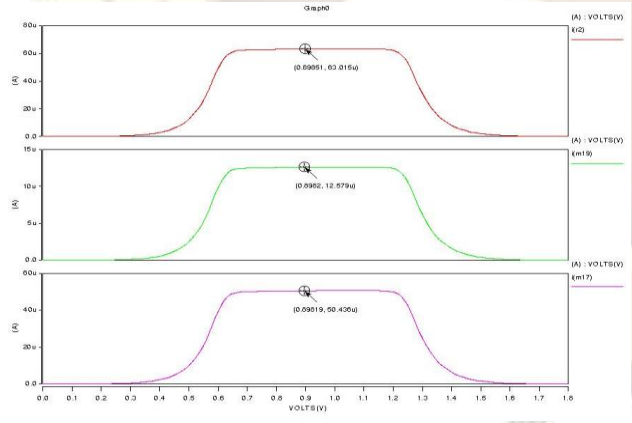


**Fig 6: Total current 63µA for S0 S1 S2 S3 = 1010**

**Table 3: Output Current for Different Binary Weights**

| W | S0 S1 S2 S3 | Total Current(amp) |
|---|---|---|
| 0 | 0 0 0 0 | 0 |
| 1 | 0 0 0 1 | 6.3045µ |
| 2 | 0 0 1 0 | 12.609 µ |
| 3 | 0 0 1 1 | 18.99 µ |
| 4 | 0 1 0 0 | 25.218 µ |
| 5 | 0 1 0 1 | 31.522 µ |
| 6 | 0 1 1 0 | 37.827 µ |
| 7 | 0 1 1 1 | 44.131 µ |
| 8 | 1 0 0 0 | 50.436 µ |
| 9 | 1 0 0 1 | 56.740 µ |
| 10 | 1 0 1 0 | 63.045 µ |
| 11 | 1 0 1 1 | 69.349 µ |
| 12 | 1 1 0 0 | 75.654 µ |
| 13 | 1 1 0 1 | 81.958 µ |
| 14 | 1 1 1 0 | 88.263µ |
| 15 | 1 1 1 1 | 94.567 µ |

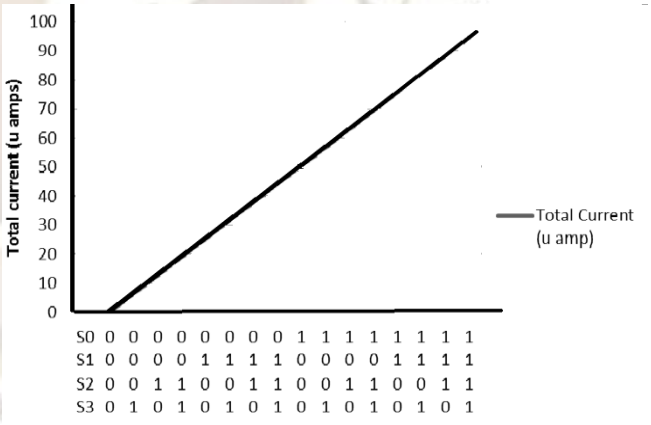



**Fig 7: Measured Current Response for Different Binary Weights.**

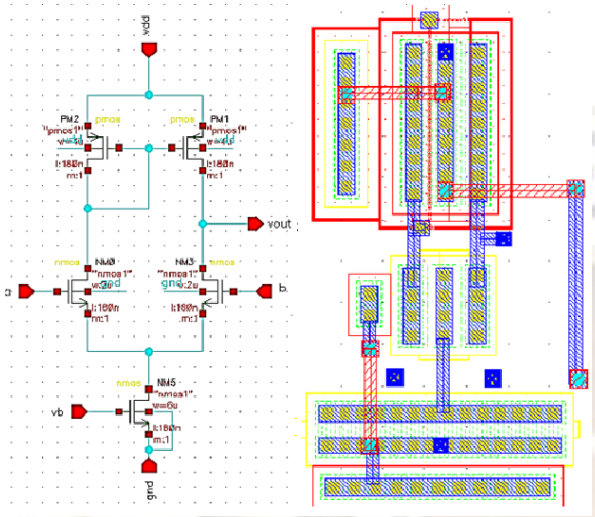



**Fig 8: Differential Amplifier Circuit and Its Layout**

The block *tan* in is the final schematic for neural architecture. Differential amplifier when design to work in sub-threshold region acts as neuron activation function. To understand this considers a simple differential pair. Now the currents in sub-threshold region are given in equation **(3)** and assuming source and base to shorted and both transistors have same W/L

$$I_{ds} = I_o e^{q\,[Vg - nVs]\,/nKT} \qquad (3)$$

$$I_{out} = I_b I_a \frac{1 - e^{-2\frac{q[V_2 - V_1]}{2nKT}}}{1 + e^{-2\frac{q[V_2 - V_1]}{2nKT}}} \qquad (4)$$

Thus

$$I_{out} = I_b I_a \tanh\left(\frac{q[V_2 - V_1]}{2nKT}\right) \qquad (5)$$

Equation **(5)** proves the functionality of the differential amplifier as a *tan* sigmoid function generator. As is evident from equation **(5)** $I_{out}$ is the combination of bias current and the voltage input. Thus this can also be used as a multiplier when one input is current and the other is voltage. [6]

The DA circuit and its layout are shown in Fig 8 and its transient response is given Fig 9.

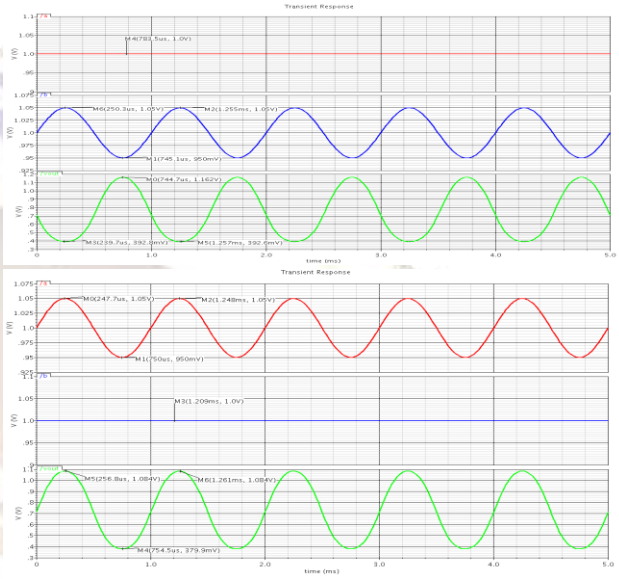



**Fig 9: Transient response of Differential Amplifier**

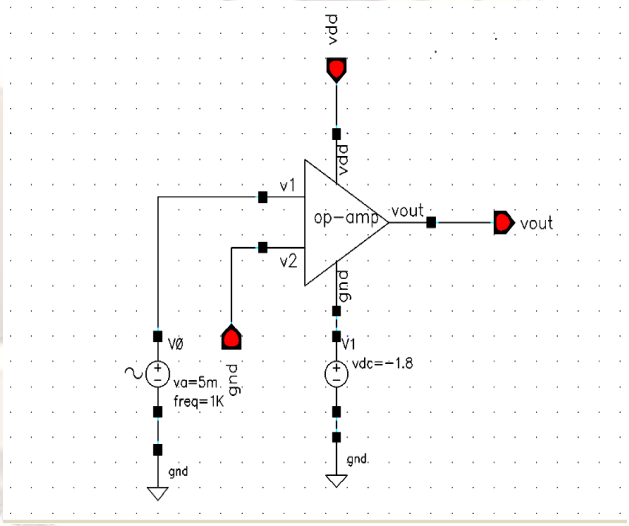



**Fig 10: Op- Amplifier Test-bench**

The op-amp plays very important role in neural network based image compression it used as voltage follower, adder etc. Designed Op- Amp as shown in Fig 10 that provides an open –loop gain of 40.972dB. The op-amp layout, Transient response

and its gain is shown Fig 11- Fig 12.

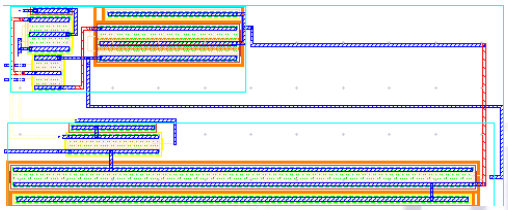
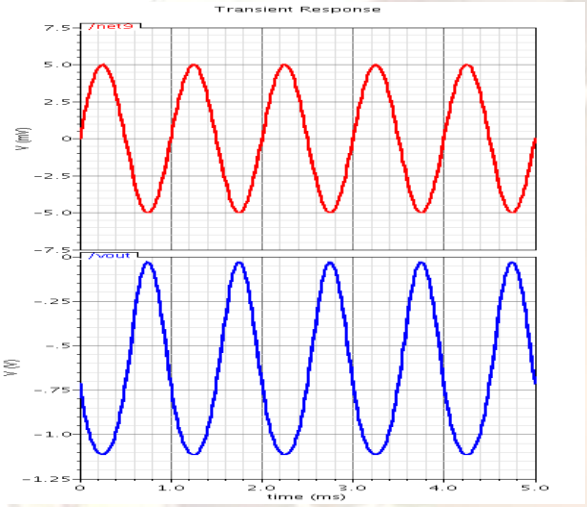


**Fig 11: Op- Amplifier layout**



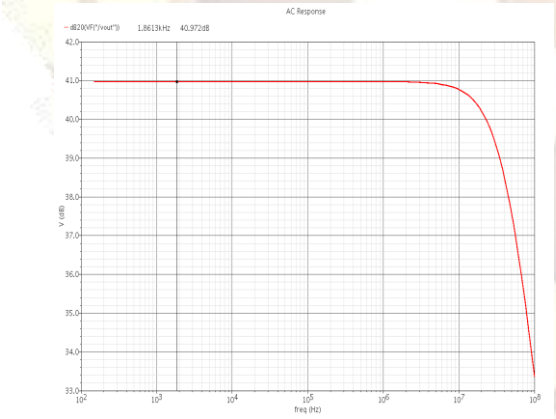




**Fig12: Output response of Op-Amplifier**

## CONCLUSION:

The design and analysis has been carried out in Cadence Virtuoso and HSPICE.

(a) Designed current reference circuit that takes 16 transistors and produces a maximum current for design 4-bit current steering

(b) circuit is 94.567 µA when all the binary weights are high.

(c) The area occupied by DA is 85.355 $\mu m^2$ and its power dissipation is 58.29pW.

(d) The op-amp area is 1187.56 $\mu m^2$, power dissipation is 41.836mW and its gain is 40.972dB.

So finally the results of designed sub-circuits like DA**,** current reference and Op-Amps are suitable for implementation of Multiplying DAC for neural network based image compression and decompression.

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