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Design of a Low-Voltage, Low-Power, High-Gain Operational Amplifier for Data Conversion Applications

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ABSTRACT
The objective of this paper is to design a Low-Voltage, Low-Power and High-Gain Operational Amplifier used for Data Conversion process. These Data Converters are used in Biomedical and Telecommunication applications. This work presents the optimized architecture of an operational amplifier, The characteristics are verified by using 0.18µm CMOS technology and also outlines the performance of an op-amp at supply voltage 1.2V.
The simulation results show that the Open Loop Gain≥79dB, Unity Gain Frequency≥110MHz, Slew Rate=175v/µs, CMRR≥89dB, PSRR≥75dB, ICMR=0 to 1.2v(Rail to Rail), Settling Time≤10ns, Output Swing= close to rail and Input Offset Voltage=0.001µv.

Keywords:- CMRR, High-Gain, ICMR, Low-Voltage, Low-Power.

1. INTRODUCTION
In this paper a Low voltage, Low power, High gain CMOS operational amplifier is presented. The design of operational amplifiers puts new challenges in low power applications with reduced channel length devices. In the design fully differential topology has been employed for high gain and high bandwidth applications. In order to obtain an input stage with a rail-to-rail input range, a n- and p-channel pair has to be driven in parallel. Without precautions the small signal transconductance **(gm)** of such a combination depends on the common input voltage because the differential pairs will cutoff nearby one of the supply rails [6].
Biasing voltage sources have been used for biasing purpose. Simulation result shows that the DC differential gain of 79 dB, 110 MHz unity gain frequency, and 175 V/µS slew rate are some of the quantitative figure of operational amplifier designed. High gain in operational amplifiers is not the only desired figure of merit for all kind of signal processing applications. Simultaneously optimizing all parameters has become mandatory now a days,in operational amplifier design. In past few years various new topologies have evolved and have been employed in various applications.

Most of them have been also integrated with the existing ones, thus the combination of two or more resolved the problems which had been noticed earlier in the designs.

2. DESIGN SPECIFICATIONS
If the signal magnitude is large, the sampling capacitor can be made smaller (for a fixed **SNR),** thereby reducing the load of the OTA, which then can be designed for a lower bias current and hence consume less power [14]. Since the supply voltage is rather low and since a large signal swing might result in increased distortion in the switches, a maximum full-scale signal swing is found to be a good compromise [14].

2.1 Signal levels and sampling capacitor
The operational amplifier is used for the front-end of an A/D converter; the sampling capacitor should be chosen in order to reduce its k_BT/C – noise [14]. The value of the sampling capacitor was calculated by

Let Signal to noise ratio (SNR) = 66dB

$$SNR = 10\log_{10}\left[\frac{V^2_{out\ .rms}}{1.26\times 2\times\frac{K_BT}{C_S}}\right] \quad (1)$$

Where

$$V_{out\cdot rms} = \frac{V_{out\ .pp\ ,min}}{2\sqrt{2}} \quad (2)$$

By substituting $V_{out\cdot rms}$ we get C_s=0263pf (0.5 pf)

2.2 Slew Rate (SR)
Finding the slewing time states that the time allocated for slewing should be about ¼ of half the sampling period (Ts/8), which is 5ns when fs= 25MS/s. The outputs of the operational amplifier should be able to deliver a $1.2V_{pp}$ signal and this is also the highest voltage step allowed. Hence, slew rate can be calculated as follows:

$$SR = 8\frac{V_{PP}}{T_S} = 8V_{pp}f_s \quad (3)$$
$$= 200v/\mu s$$

2.3 Unity Gain Frequency (f_T)
The requested accuracy (P) was calculated by assuming that the signal should lie within 1LSB after the settling time. This is equal to

$$P = ½\times 2^{-10} = 2^{-11} \quad (4)$$

The unity gain frequency is given as

$$f_T > \frac{2f_S\ln(2^{11})}{2\pi\times 0.8\times 0.75} = 4.05f_s \quad (5)$$
$$= 102\ MHz$$

2.4Settling Time (T_s)
The settling time is the time it takes for the signal to settle within a certain wanted range. It is illustrated below, where T_S is the settling time.

$$T_s = 1/f_T \quad (6)$$
$$= 8ns$$

2.5 DC-Gain (A0)
The following expression is the linear settling error coefficient (f=β).

$$e_0 = \frac{1}{1+\beta A_0} \quad (7)$$

This error should be less than ½LSB, giving

$e_0 = \frac{1}{\beta A_0} < \frac{1}{2} 2^{-10}$ (8)

L et β= 0.25 to 0.57. Let β=0.5

$A_0 > \frac{2^{11}}{\beta}$ (9)

=72dB

In general this becomes

$\mathbf{A_0 > \frac{2(N+1)}{\beta}}$ (10)

Where N= NOB (Number Of Bits)

2.6 Common Mode Rejection Ratio (CMRR)

Common-mode rejection ratio, CMRR, is defined as the ratio of the differential voltage amplification to the common-mode voltage amplification, A_{DIF}/A_{COM}. It is expressed in dB.

CMRR = 20log (A_{DIF}/A_{COM}) dB (11)

Ideally this ratio would be infinite with common mode voltages. A_{COM} is very small. Hence CMRR is very high.

2.7 Power Supply Voltage Rejection Ratio (PSRR)

PSRR gives how well the Operational amplifier filters out the noise coming through the power pins. In this application the PSRR should be high.

2.8 Phase Margin

Phase margin at unity gain is the difference between the amounts of phase shift a signal experiences through the Operational amplifier at unity gain and 180° phase. This value lies between 45° to 60°. In this consideration phase margin is taken as 60º.

2.9 Input Offset Voltage

The apparent voltage difference between the inputs even when the inputs are shorted together is termed as input offset voltage. This is due to unavoidable imbalances inside the Operational amplifier and by applying a small voltage at the input terminals makes the output voltage zero.

3. PROPOSED MODEL

3.1 Input Stage

The input stage is shown in the Fig 1. The input stage mainly comprises of the CMOS complementary stage which consists of an N-differential pair (M1-M2) and a P-differential pair (M3-M4). The current bias transistors are used to keep the current flowing in the differential stage constant. The transistors M7-M10 are used for keeping the g_m constant. The remaining transistors in the cascode stage are used as the current summing stage. The transistors M11, M12, M17, and M18 are used to avoid the current to become zero at the output of the input stage.

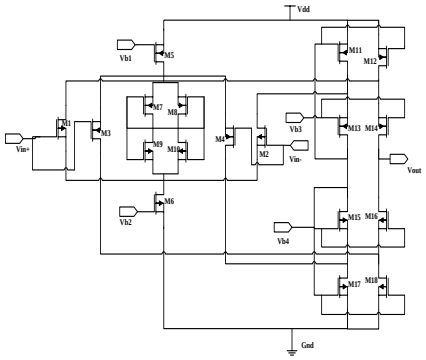

Fig.1: Input Stage

If there are no transistors M13, M14, M15, M16 then the output of the input stage is dependent on the constant g_m circut. So to avoid such situation the transistors M11, M12, M17, and M18 are included.

3.1.1 W/L Calculation

The Iss (current through NMOS bias transistor) is

$$Iss = 2\times SR \times C_L \quad (12)$$

Calculation of W/L ratio by using the formula

$$(W/L)= 2 \times Ids/(K' \times V^2_{deff}) \quad (13)$$

$$(W/L)_{M1,M2\ nmos}=(W/L)_{M6\ nmos}/2 \quad (14)$$

$$(W/L)_{M3,M4\ Pmos}=2.5*(W/L)_{M1\ nmos} \quad (15)$$

$$(W/L)_{M5\ Pmos}=2.5*(W/L)_{M6\ nmos} \quad (16)$$

$$(W/L)_{M6\ nmos}=2 \times Iss/(K' \times V^2_{deff}) \quad (17)$$

$$(W/L)_{M7,M8,M11.M12\ Pmos}=3*(W/L)_{M3\ Pmos} \quad (18)$$

$$(W/L)_{M9,M10nmos}=3*(W/L)_{M1\ nmos} \quad (19)$$

$$(W/L)_{M13,M14\ Pmos}=3.5*(W/L)_{M5\ Pmos} \quad (20)$$

$$(W/L)_{M15,M16\ Nmos}=(W/L)_{M13\ Pmos/2.5} \quad (21)$$

Where $\mu_n=2.5\mu_p$

K' is the technology dependent factor.

The W/L ratios are calculated for each transistor by using the above formulae which are shown in the Table 1below.

Name of the Transistor	W/L Ratio's(µm/µm)	M
M1, M2	72/1	1
M3, M4	181/1	1
M5	361/1	1
M6	145/1	1
M7, M8	542/1	1
M9, M10	217/1	1
M11, M12	551/1	1
M13, M14	734/1	1
M15, M16	289/1	1
M17, M18	361/1	1

Table 1: W/L ratios of input stage

3.2 Output Stage

The output stage shown in Fig.2 was introduced. It consists of a push-pull pair, M_N and M_P, and a driver circuit made up of transistors M1-M6 and two current generators, I_B and I_Q. The stage exhibits high linearity provided that the driver structure is symmetrical that is, transistors MiA and MiB must have the same aspect ratio [16].

If all the transistors operate in the saturation region and the circuit is under quiescent state, assuming a first-order model for MOS transistors and defining

$n=W_N/W_5=W_P/W_6$ *(22)*

$m=W_1/W_3=W_2/W_4$ (23)

$\gamma=W_1/W_5$ (24)

$\lambda=W_2/W_1$ (25)

We get for I_Q, I_{TOT}, and G_{mout}

$I_Q = n \times m \times I_B$ (26)

$I_{TOT} = \left[1 + \frac{2(m+1)}{m \times n}\right] \times I_Q$ (27)

$G_{Mout} = \frac{2n \times g_{m1}}{1+\sqrt{\mu_n/\lambda\mu_P}} = \frac{2\sqrt{\gamma} \times g_{mN,P}}{1+\sqrt{\mu_n/\mu_P}}$ (28)

By using the $g_{mN,P}$ we calculate the W/L's of output transistors

$W/L = g^2_{mN,P}/(K' \times V^2_{deff})$ (29)

Where the latter term is expressed as a function of the transconductance of output branch transistors, $g_{mN,P}$. From (22), (23) and (24) it is easy to compute Quality Factors *QC*, *QB* and *QD*, respectively, which result

$Q_C = \frac{2(m+1)}{m \times n}$ (30)

$Q_B = \frac{\sqrt{\gamma}}{\left[(1+\sqrt{\mu_n/\lambda\mu_P})\left(\sqrt{1+\frac{2(m+1)}{m \times n}}\right)\right]}$ (31)

$Q_D = \frac{1}{96}\left(1 + \sqrt{\mu_n/\lambda\mu_P}\right)\left(1 + \frac{2(m+1)}{m \times n}\right)$ (32)

If we set m= 5, this means setting *n* to a value higher than 12. A good choice for parameter λ is setting $\lambda = \mu_n/\mu_P$.

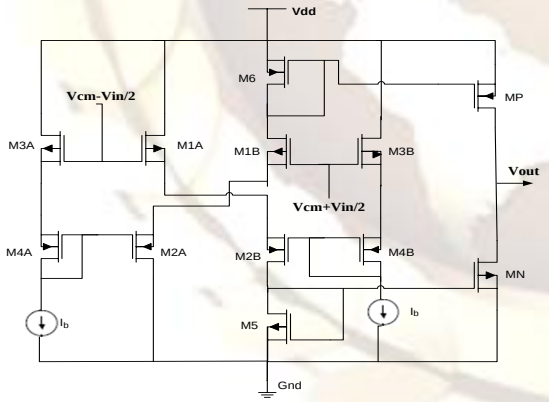

Fig 2: Schematic of the output stage

The W/L ratios for the output stage are done by using the formulas given in the Table 2 below.

Name of the Transistor	W/L Ratio's(µm/µm)	M
MN	127/1	2
MP	322/1	2
M3A,M3B	9/1	1
M4A, M4B	26/1	1
M1A, M1B	42/1	1
M2A, M2B	127/1	1
M5	9/1	1
M6	22/1	1

Table 2: W/L ratio's of output stage transistors

The Quality factors of the output stage is given in the Table 3

Quality Factors	Value
Q_B	1.03
Q_C	0.16
Q_D	0.24

Table 3: List of Quality factors values

3.3 complete opamp

By combining the two stages (input and output) the Operational amplifier for this application is obtained and the circuit for the complete Operational amplifier is given in the figure 3 below.

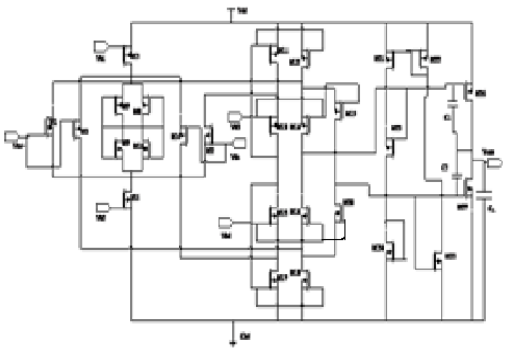

Fig 3: Schematic of the complete op amp

The fig.3 shows the schematic representation of operational amplifier. Basically it is having three stages. The first stage is differential P-pair and N-pair with constant g_m circuit and second stage consists of folded current summing stage and the third stage is class AB push-pull amplifier with driving circuit.

The W/L ratios of the complete Operational amplifier are calculated by modifying the output stage. They are listed in the below Table 4.

Name of the Transistor	W/L Ratio's(µm/µm)	M
M1, M2	72/1	1
M3, M4	181/1	1
M5	361/1	1
M6	145/1	1
M7, M8	400/1	1
M9, M10	217/1	1
M11, M12	551/1	1
M13	734/1	1
M14, M19	367/1	1
M15	289/1	1
M16, M20	195/1	1
M17, M18	361/1	1
M21,M22,M23	15/1	1
M24	6/1	1
M25	0.3/1	1
M26	322/1	2
M27	127/1	2

Table 4: W/L ratio's of complete Operational amplifier transistors

SIMULATION RESULTS

4.1 Input stage

The schematic edit for the input stage is shown in below fig 4.

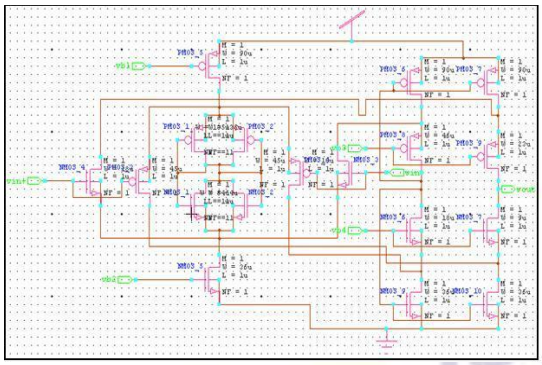

Fig 4: Input stage of the Operational amplifier

4.2 Output Stage

The schematic edit of the output stage is given in the fig 5 below.

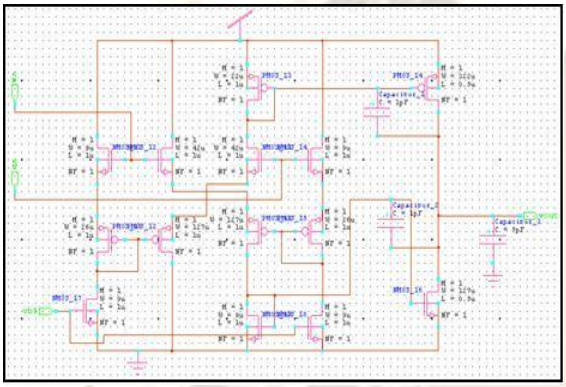

Fig 5: Output stage of the Operational amplifier

4.3. Complete Operational Amplifier

The schematic edit for the complete Operational amplifier is given in the fig 6 below.

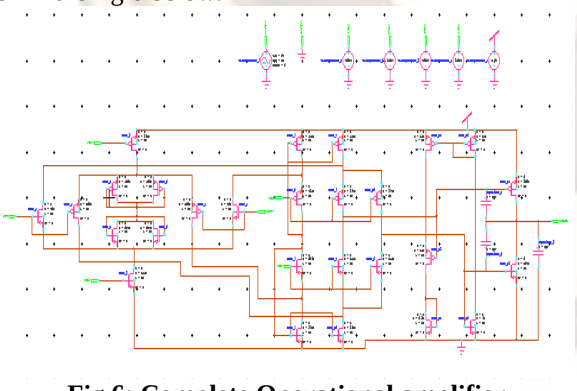

Fig 6: Complete Operational amplifier

4.4 Results and discussions

4.4.1 Open Loop Gain

The input Vin+ is connected to ground and Vin- is connected to 1mV AC supply. The output is taken at output terminal (Vout). The open loop is the ratio between vout and Vin-.

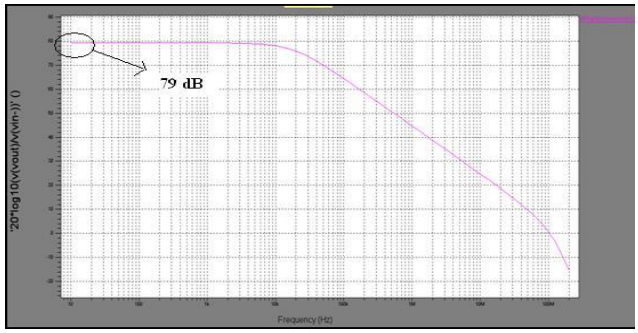

Fig 7: Output waveform of Open loop gain

The output waveform obtained in Fig 7 is the open loop gain configuration. The Y-axis represents the gain in dB and X-axis represents the frequency in Hz. The open loop gain is 79dB.

4.4.2 CMRR

The differential input signal (Vd) is applied between the operational amplifier terminals Vin+ and Vin- and the required output is obtained at the output terminal (Out). The ratio between Vd and output voltage is known as CMRR.

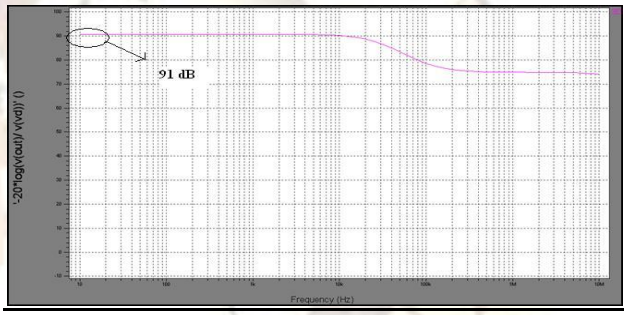

Fig 8: Output waveform of Common Mode Rejection Ratio

The output waveform obtained in Fig 8 is the CMRR. The Y-axis represents the gain in dB and X-axis represents the frequency in Hz. The CMRR value is 91dB up to 10 KHz and it decreases further with increase in the frequency.

4.4.3 Slew Rate

The input Vin+ is connected to pulse signal with 1V amplitude and Vin- is connected to output terminal (out). The output is taken at output terminal (out). Slew rate is the ratio of change in the output voltage to the change in the time.

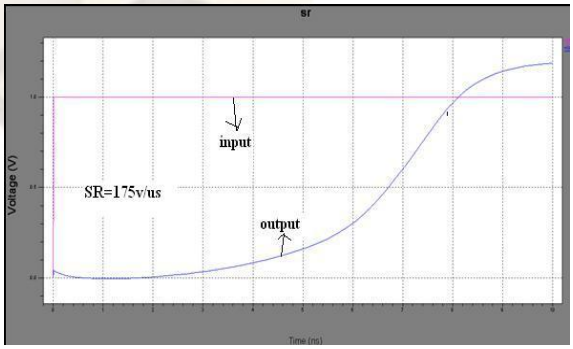

Fig 9: Input and Output waveforms for Slew rate

The Fig 9: represents the input and output waveforms for slew rate configuration. The blue line is the output signal and the pink line is the input signal. The Y-axis represents

the voltage in volts and the X-axis represents time in ns. The Slew rate value is 175V/µs.

4.4.4 Settling Time

The input Vin+ is connected to pulse signal with 1V amplitude and Vin- is connected to output terminal (out). The output is taken at output terminal (out). Settling time is the time required for the output voltage to settle within a specified percentage of the final value given pulse input.

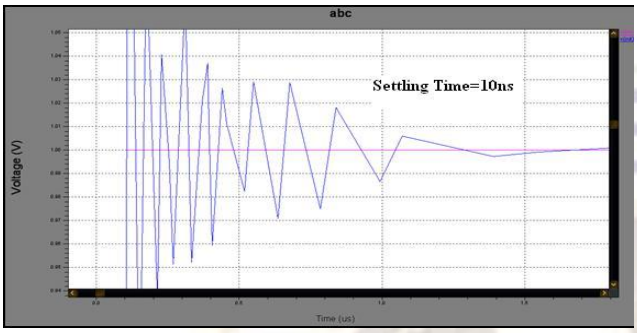

Fig 10: Input and Output waveforms for settling time

The Fig 10: represents the input and output waveforms for settling time configuration. The pink line is the input signal and the blue line is the output signal. The Y-axis represents the voltage in volts and the X-axis represents time in µs. The value of settling time is 150ns.

4.4.5 ICMR

The input Vin+ is connected to Vd with 700mV DC supply and Vin- is connected to output terminal (out). The output is taken at output terminal (out). ICMR is the range between maximum value of the output to the minimum value of the output.

Fig 11: Output waveform of Input Common Mode Range

The Fig 11: shows the output of ICMR. The Y-axis represents the voltage in volts and X-axis represents the voltage in volts. The ICMR value is 0 to 1.2V

4.4.6 Output Swing

The input Vin- is connected to Vd of 700mV DC supply with a resistor of value 1KΩ and Vin+ is connected to ground. There is a feedback resistor of 10KΩ and a output resistor of value 50Ω. The output is taken at output terminal (out). The output swing represents the maximum rail (1.2V) to rail (0V) value.

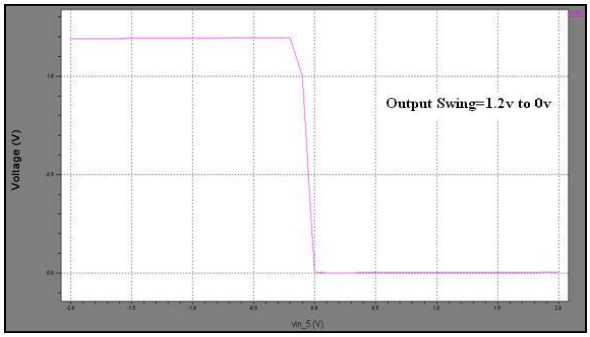

Fig 12: Output waveform of Output Swing

The Fig 12: shows the output swing. The Y-axis represents the voltage in volts and X-axis represents the voltage in volts. The output swing is 1.2V to 0V

4.4.7 PSRR

A small sinusoidal voltage is inserted in series with the Vdd to measure PSRR. PSRR is the ratio of Vdd to output voltage. A resistor of value 10KΩ is inserted at the output and ground. Vin+ is connected to ground.

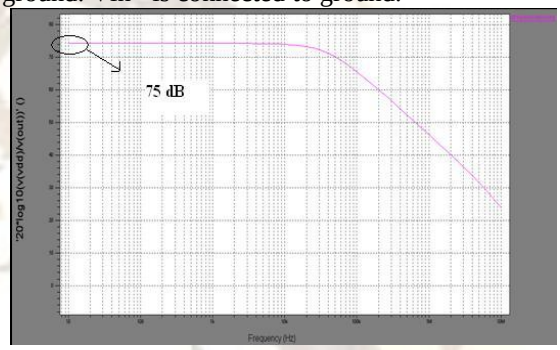

Fig 13: Output waveform of Power Supply Rejection Ratio

The output waveform obtained in the Fig 13: is for the PSRR. The Y-axis represents the gain in dB and X-axis represents the frequency in Hz. The PSRR value is 75dB up to 11 KHz and it decreases further with increase in the frequency.

3.4.8 Unity Gain Frequency

The input Vin+ is connected to ground and Vin- is connected to 1mV AC supply. The output is taken at output terminal (Vout). The unity gain frequency is the frequency at which the decibel magnitude is 0dB.

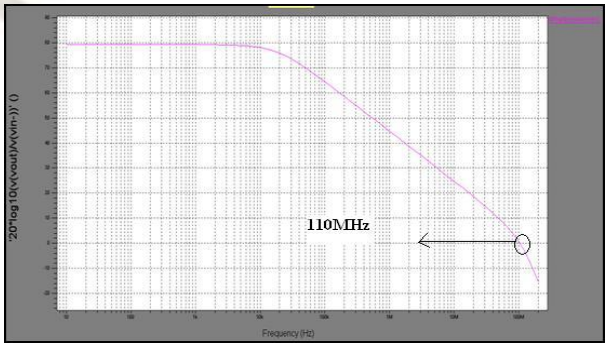

Fig 14: Output waveform of Unity Gain frequency

The output waveform shown in the Fig 14: is for the unity gain frequency. The Y-axis represents the gain in dB and X-axis represents the frequency in Hz. The unity gain frequency is 110MHz.

3.4.9 Input Offset Voltage

The input Vin+ is connected to Vd with 700mV DC supply and Vin- is connected to output terminal (out). The output is taken at output terminal (out). Input offset voltage can be measured at zero crossing point on Y-axis.

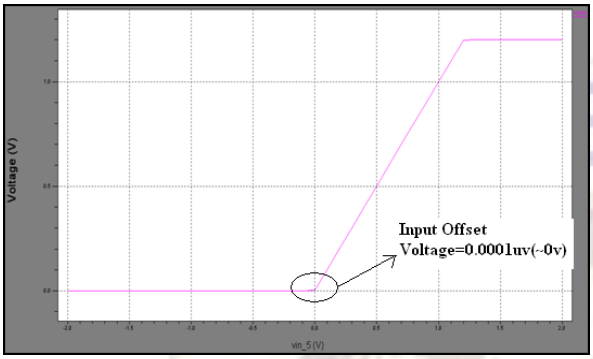

Fig 15: Output waveform of Input offset voltage

The Fig 15: shows the output of Input offset voltage. The Y-axis represents the voltage in volts and X-axis represents the voltage in volts. The Input offset voltage value is 0.0001µv

4.5 Comparison Table

Calculated parameters and simulation results are listed in the below Table 5.

Performance parameter	Design goal	Practical values
Output swing	Close to rails	0 to 1.2V
Total power consumption	Low	3.34mW
0.1%Settling Time	8ns	20ns
Slew rate	200V/µs	175V/µs
Gain(DC)	72db	79db
Phase margin	45 to 60	60
Unity gain frequency	102MHz	110MHz
CMRR	80dB	91dB
PSRR+	70dB	75dB
Input Offset Voltage	0v (ideal)	0.0001uv

Table 5: Comparison Table

4. CONCLUSION

Low-voltage operational amplifiers are extremely limited in dynamic range. Therefore, efficient topologies are needed. Voltage efficient rail-to-rail input stage and voltage and current efficient rail-to-rail class-AB output stages have been presented.The proposed model contains 3 stages. First stage is differential P-pair and N-pair with constant g_m circuit, second stage consists of folded current summing circuit and the third stage is class AB push-pull amplifier with modified driver circuit. The circuit characteristics have been verified by using 0.18µm technology. The simulation results are compared with the theoretical calculations.

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