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IMPLEMENTATION OF LMS ALGORITHM TO REDUCE NON LINEARITY IN A PIPELINED ADC

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Abstract—The performance of a pipelined ADC is mainly influenced by errors like gain error, op amp non linearity and capacitor mismatches. The operational amplifier non linearity can be reduced by calibration techniques to achieve high accuracy.The least mean squared (LMS) calibration is used to estimate the error parameters in the digital domain. It is data-driven and operates in the background to remove the non linearity of a system. This adaptive digital technique can be used to calibrate pipelined analog-to-digital converter. In this work, LMS algorithm will be implemented on an12 bit pipelined ADC, mainly to reduce the effects of op amp non linearity on the performance of ADC. The performance evaluation will be done with extensive circuit simulations. It is also a major concern to replace the sample-and- hold amplifier of the ADC with the multiplying DAC for eliminating the additional noise and power consumption. Strong tradeoffs between the accuracy and speed of pipelined ADCs are greatly relaxed in this approach with the aid ofdigital correction technique.

Keywords :Non linearity, LMS calibration, Digital correction

I.INTRODUCTION

Pipelined ADCs are most popular topology among the other ADC due to their resolution and the speed and also reduces the hardware complexity among the other ADCs. The design of the high speed and resolution ADCs is a challenge as the device dimensions and supply voltage are scaled down. In the ADC the generic issues are the nonlinearity, capacitor mismatch and the Gain error. And the issues are corrected by the calibration.With the use of pipelinedADCs in many consumer products, research in improving the performance of pipelinedADCs has attracted much attention over the past decade, where the most popular areas ofresearch have been: linearity enhancement

This paper introduces the blind calibration algorithm that enhances the linearity in the ADC .In this calibration used to enhance the linearity using least mean square (LMS). As the many Pipelined architecture is mainly used in the Mobile stations, digital receivers, CCD Imaging, medical applications etc. In the above applications linearity is the main theme so the LMS calibration in ADCs enable more cost effective integrated circuits for both mobile and wired systems.

II.ADC MODELLING

In order to suppress the thenon linearity in the opamp ,offset and mismatch problems we are trying to reduce nonlinear so we have to choose the calibration i.e nothing but modeling of the ADC.

$$V_{out} = \alpha_1 Vin^1 + \alpha_2 Vin^2 + \alpha_3 Vin^3 \quad (1)$$

and the inverse function to the above eqn is

$$V_{in} = \beta_1 {V_{out}}^1 + \beta_2 {V_{out}}^2 + \beta_3 {V_{out}}^3 \quad (2)$$

We substitute

$$\beta_1 = \frac{1}{\alpha_1} \quad (3$$

$$\beta_2 = -\frac{\alpha_2}{{\alpha_1}^2} \quad (4)$$

$$\beta_3 = \frac{2{\alpha_2}^2}{{\alpha_1}^5} - \frac{\alpha_3}{{\alpha_1}^4} \quad (5)$$

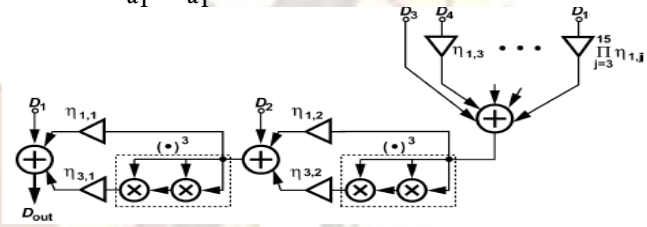

Fig 1: ADC modeling

In the First and the Second stages of the pipelined ADC the above model is used to reduce the nonlinearity and other stages in the pipelined ADC considered to be as the ideal backend and suppressing the non linearity in the first two stages and assumes as the other stages as an ideal .

III.ADC ARCHITECTURE.

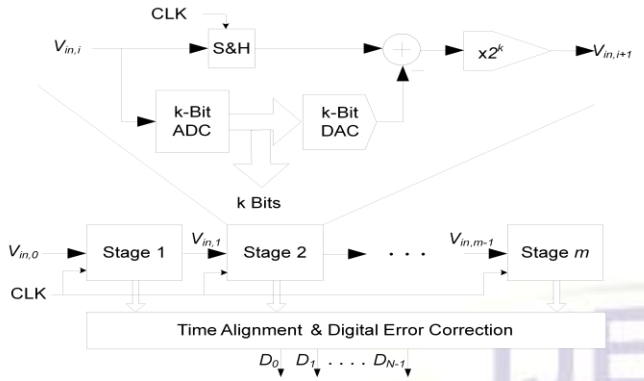

Fig 2: Architecture of pipelined ADC

To implement the twelvebit pipelined ADC we require the nine stages. Each stage contains the sub ADC, MultiplyingDAC(MDAC or 1.5bitperstage).Each stage resolves the two bits with a sub ADC,subtracts this value from the input and amplifies the resulting residue by a gain of two. The stages are arranged by the switched capacitor gain blocks that provide an SHA at each stage.The implementation of each pipeline stage is shown below in fig 2. In the MDAC it contains the operational amplifier, comparator, and the MUX. in the pipelined Architecture we need the opamp should have high gain bandwidth and the fast setting to achieve the high speed.

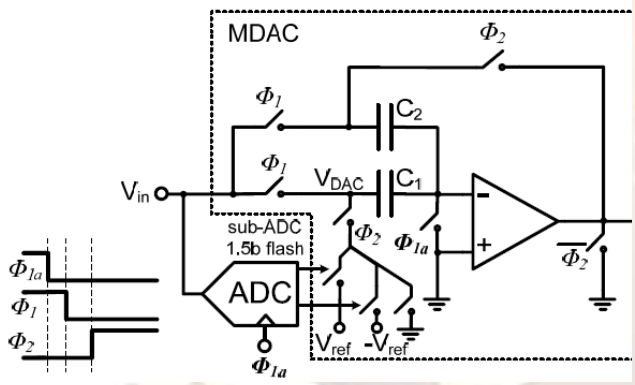

Fig 3: MDAC(1.5bit/stage)

In the 1.5b stage in the pipelined architecture when Φ1 is On the capacitors c1,c2 are sampled.During Φ2 a gain of two is implemented by discharging thecharge stored in C1 to C2, and DAC operation by connecting VDAC to a voltage set by the sub-ADC. In the phase Φ2the c2 forms closes a negative feedback around the op –amp while the top plate of c1 is switched to digital- to- analog converter output ths voltage is called the residue voltage Vo.

$$Vo = \begin{cases} \left(1+\frac{c1}{c2}\right)Vi - Vref, & if Vi > \frac{Vref}{4} \\ \left(1+\frac{c1}{c2}\right)Vi, & if \ -\frac{Vref}{4} \le Vi \le \frac{Vref}{4} \\ \left(1+\frac{c1}{c2}\right)Vi - Vref, & if Vi < -\frac{Vref}{4} \end{cases} \quad (5)$$

And to obtain the ADC linearity a precise interstage gain is required in the op-amp.And the op amp required is (>80 db)to reduce the finite gain error in the pipelined ADC.

IV.SUB ADC

The sub ADC is designed by using the comparators to define the resolution of the ADC. The sub ADC mainly consists of the preampifier,Decision circuit (Latch)and the buffer as shown in fig

Fig 8: Comparator Block Diagram

The input pre-amplifier, a positive feedback or decision stage and an output buffer. The pre-amp stage amplifies the input signal to improve the comparator sensitivity (i.e. increases the minimum input signal with which the comparator can make a decision) and isolates the input of the comparator from switching noise coming from the positive feedback stage. The positive feedback stage is used to determine which of the input signal is larger. The output buffer amplifies this information and outputs a digital signal. The sub ADC digital signal is fed to the MDAC for based on the reference signal it give only three states to the MDAC.

Operational amplifier:

The topology used in the piplined ADC is gain boosting to achieve the linearity we require the high op amp dc gain and to settle them with less accuracy.The gain-boost technique is based on increasing the cascoding effect of *T2* by adding an additional gain stageas shown in Fig. 1. This stage reduces the feedback from the output to the drain of the input transistor. Thus, theoutput impedance of the circuit is increased by the gain of the additional gain stage, Aadd:

$$Rout = (gm2.r02(Aadd+1)+1)r01 + r02$$

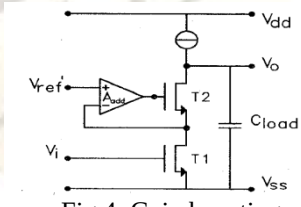

Fig 4: Gain boosting

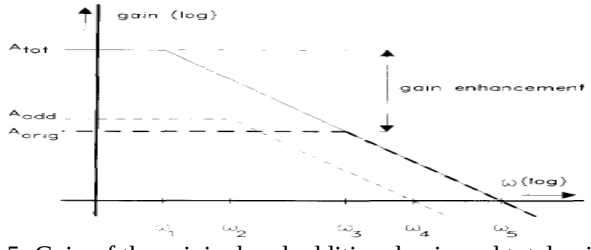

Fig 5: Gain of the original and additional gain and total gain

In this way, the dc gain can be increased several orders ofmagnitude:

$$Ao = gm1.r01(gm2.r02(Aadd + 1) + 1) \quad (7)$$

deals with the high-frequency behavior of this circuit and discusses what happens if the gain of the additional stage decreases as a function of frequency. If the additional stage is implemented as a cascade stage, the gain-enhancement technique as described above can also be applied to this additional stage. In this way, arepetitiveimplementation of the gain enhancement technique can be obtained.

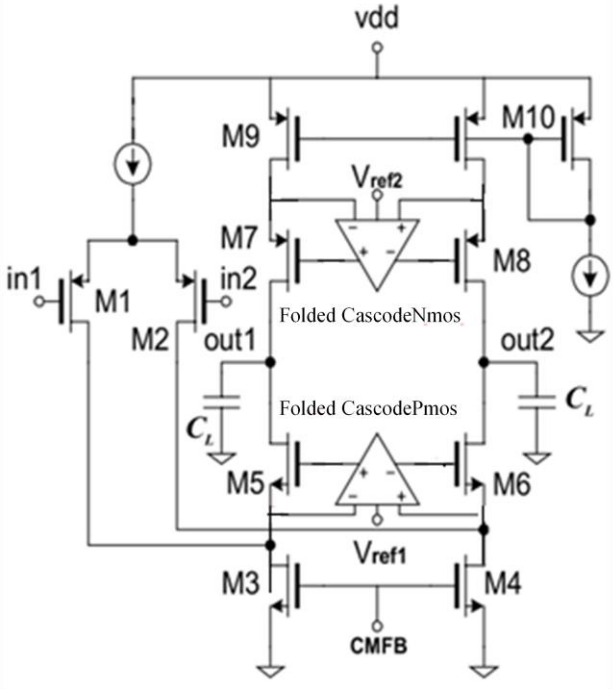

Fig 6: Gain Boosting Folded Cascode op amp

In this work fully folded cascode amplifiers are used to obtain the high DC gain for the fast settling and low power consumption.As the settling time is directly related to the Unity gain frequency.

Supply volatage	1.8V
Technology	0.18µ
Gain	90 db
Voltage swing	1Vp-p
UGB	600Mhz
Load capacitor	2pf
Power disspation	24mW
Slew rate	10V/µsec

Table 1:Op amp specifications

OUTPUT WAVEFORM:

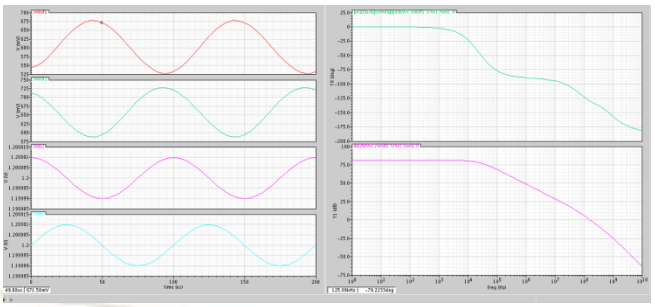

Fig 7:Swings and the Gain of the operational amplifier

CALIBRATION CONCEPT

The calibration algorithm begins the fore ground mode and moves in the background and the calibration goes with the conceptual FIR filter to correct the coefficients of the INL and DNL

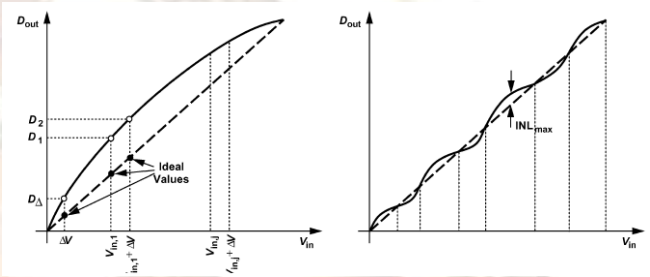

Fig 8:Before and after the calibration of ADC

DIGITAL CORRECTION :

In the pipelined adc comparator has some offsets so as to reduce the offsets digital correction block contains the array of the flip flops to obtain the data values with out error and also the adder block for the correction i.e, nothing but implementation of LMS algorithm by keeping the adders and multipliers serially for the analog signal to get the digital signal.

Fig 9:Digital correction block with array of flip flops

V.CONCLUSION

In this work, the schematic design and simulation of the sub-blocks and full circuit of a 12-bit pipelineADC were completed in 0.18u Technology and to implement in lower order technology to improve the speed and efficiency of theADC. In this work LMS algorithm we would try improve the linearity and suppresses the third order harmonics and by the ADC modeling but with this we have

to minimize the capacitor mismatch and the gain error with the better algorithms .

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