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Power reduction on clock-tree using Energy recovery and clock gating technique

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Abstract— Power consumption of the clock tree dominates over 40% of the total power in modern high performance VLSI designs, measures must be taken to keep it under control. Hence, low power clocking schemes are promising approaches for low-power design. We propose four novel energy recovery clocked flip-flops that enable energy recovery from the clock network, resulting in significant energy savings. These flip-flops operate with a single-phase sinusoidal clock which can be generated with high efficiency. In the Tanner 250nm CMOS technology, we implemented these energy recovery clocked flip-flops through an H-tree clock network driven by a resonant clock-generator to generate a sinusoidal clock. The proposed flip-flops exhibit more than 80% delay reduction, power reduction of up to 47%, as compared to the conventional energy recovery flip-flop. Simulation results show a power reduction of 90% on the clock-tree and total power savings of up to 83% as compared to the same implementation using the conventional square-wave clocking scheme and flip-flops. In this paper, we also propose clock gating solutions for energy recovery clocking. Applying our clock gating to the energy recovery clocked flip-flops reduces their power by more than 1000 times in the idle mode with negligible power and delay overhead in the active mode. A pipelined array multiplier is designed which show a total power savings of 25%–69% as compared to the same multiplier using conventional square-wave clocking scheme and corresponding flip-flops.

Index Terms—Clock Tree, energy recovery, clock gating, low power, sinusoidal clock.

I. INTRODUCTION

Clock signals are synchronizing signals that provide timing references for computation and communication in synchronous digital systems. The increase in demand for high-performance VLSI System-on Chip (SOC) designs is addressed by increasing the clock frequency and integrating more components on a chip, enabled by the continuing scaling of the process technology. With the continuing increase in the clock frequency and complexity of high performance VLSI chips, the resulting increase in power consumption has become the major obstacle to the realization of high-performance designs. The major fraction of the total power consumption in highly synchronous systems, such as microprocessors, is due to the clock network. Increase in the complexity of synchronous SOC systems, increases the complexity of the clock network and hence increases the clock power even if the clock frequency may not scale anymore. Hence, the major fraction of the total power consumption in highly synchronous systems, such as microprocessors, is due to the clock network.

Energy recovery is a technique originally developed for low power digital circuits. Energy recovery circuits achieve low energy dissipation by restricting current to flow across devices with low voltage drop and by recycling the energy stored on their capacitors by using an AC-type (oscillating) supply voltage. In this paper, we apply energy recovery techniques to the clock network since the clock signal is typically the most capacitive signal. The proposed energy recovery clocking scheme recycles the energy from this capacitance in each cycle of the clock. For an efficient clock generation, we use a sinusoidal clock signal.

In this paper, we propose four high-performance and low-power energy recovery flip-flops that operate with a single-phase sinusoidal clock. The proposed flip-flops exhibit significant reduction in delay and power as compared to the conventional four-phase transmission gate energy recovery flip-flop. The energy recovery clocked flip-flops are clocked through a H-tree clocking network. A resonant clock generator circuit was designed to generate a sinusoidal clock and drive the clock network and the flip-flops. For comparison, we implemented the same clock-tree using square-wave clocked flip-flops.

Clock gating is another popular technique for reducing clock Power. Even though energy recovery clocking results in substantial reduction in clock power, there still remains some energy loss on the clock network due to resistances of the clock network and the energy loss in the oscillator itself

due to non-adiabatic switching. In this paper, we propose clock gating solutions for the energy recover clock. We modify the design of the existing energy recovery clocked flip-flops to incorporate a power saving feature that eliminates any energy loss on the internal clock and other nodes of the flip-flops. Applying the proposed clock gating technique to the flip-flops reduces their power by a substantial amount (1000X) during the sleep mode. Moreover, the added feature has negligible power and delay overhead when flip-flops are in the active mode.

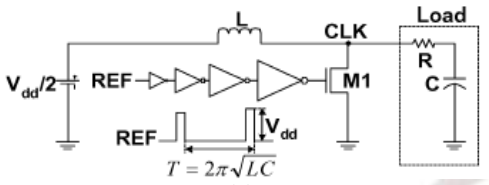
The remainder of this paper is organized as follows. Section II includes clock generation. In section III, the conventional four-phase pass-gate is reviewed and the proposed energy recovery flip-flops are described. In section IV, extensive simulation results of individual flip-flops and their comparisons are presented and clock-tree implementation. In section V energy recovery clock gating is described ad section VI shows the pipelined array multiplier. Finally, the conclusion of the paper in Section VII.

II. ENERGY RECOVERY CLOCK GENERATION

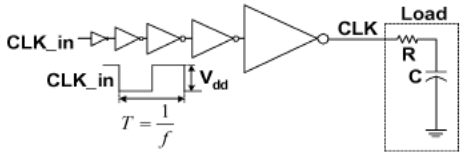
The energy recovery clock generator is a single phase resonant clock generator as shown in Figure 1(a). Transistor M1 receives a reference pulse to pull-down the clock signal to ground when the clock reaches its minimum; thereby maintaining the oscillation of the resonant circuit. This transistor is a fairly large transistor, and therefore, driven by a chain of progressively sized inverters. The natural oscillation frequency of this resonant clock driver is determined by:

$$f = \frac{1}{2\pi\sqrt{LC}} \quad (1)$$

where C is the total capacitance connected to the clock-tree including parasitic capacitances of the clock-tree and gate capacitances associated with clock inputs of all flip-flops.



(a)



(b)

Fig 1(a): Resonant energy recovery clock generator
(b) Non-energy recovery clock driver

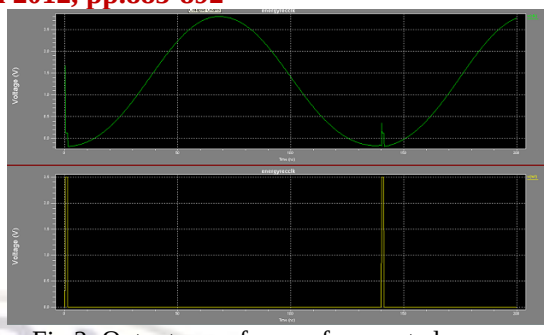


Fig 2: Output waveforms of generated energy recovery clock

In order to have an efficient clock generator, it is important that the frequency of the REF signal be the same as the natural oscillation frequency of the resonant circuit. In order to compare with the square wave clocking, three flip-flops that operate with the square-wave clock were also designed. These flip-flops are Hybrid Latch Flip-Flop (HLFF) and Conditional Capturing Flip-Flop (CCFF) which are high-speed flip-flops, and Transmission-Gate Flip-Flop (TGFF), which is a low-power flip-flop. For square wave clocking, the clock-tree is driven by a chain of progressively sized inverters as shown in Fig 1(b). Figure 2 shows the typical waveform of the generated energy recovery clock.

III. ENERGY RECOVERY FLIP-FLOPS

In this section, our proposed flip-flops, as well as the conventional energy recovery flip-flop, are presented and their operations are discussed. Figure 3 shows the schematic of a conventional Four-Phase Transmission-Gate (FPTG) energy recovery flip-flop . The energy recovery clock is a four-phase sinusoidal clock (CLK0, CLK1, CLK2, and CLK3) as shown in Figure 4. FPTG is a master-slave flip-flop with the master controlled by CLKO and CLK2 and the slave controlled by CLKl and CLK3. The main disadvantage of this flip-flop is its long delay.

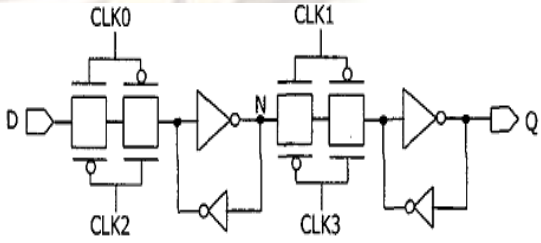


Fig 3: Conventional Four-Phase Transmission Gate(FPTG) energy recovery flip-flop

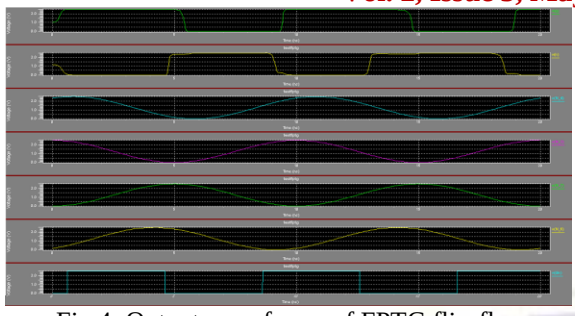


Fig 4: Output waveforms of FPTG flip-flop

As shown in Figure 4, the delay from D to Q (t_{D-Q}) takes roughly half the effective clock period (T_{eff}). In addition, transistors required for the pass-gates are large, resulting in large flip-flop area.

Another approach for energy recovery flip-flops is to locally generate square-wave clocks from a sinusoidal clock . This technique has the advantage that existing square-wave flip-flops could be used with the energy recovery clock. However, extra energy is required in order to generate and possibly buffer the local square waves. Moreover, energy is not recovered from gate capacitances associated with clock inputs of flip-flops.

Recovering energy from internal nodes of flip-flops in a quasi- adiabatic fashion would also be desirable. However, storage elements of flip-flops cannot be energy recovering because we assume that they drive standard (non-adiabatic) logic. Due to slow rising/falling transitions of energy recovery signals, applying energy recovery techniques to internal nodes driving the storage elements can result in considerable short-circuit power within the storage element.

Taking these factors into consideration, we developed flip-flops that enable energy recovery from their clock input capacitance, while internal nodes and storage elements are powered by regular supply. Employing our flip-flops in system designs enables energy recovery from clock distribution networks and clock input capacitances of flip-flops.

The first proposed energy recovery flip-flop, Sense Amplifier Energy Recovery (SAER) flip-flop, is shown in Figure 5. This flip- flop, which is based on the sense amplifier flip-flop, is a dynamic flip-flop with pre-charge and evaluate phases of operation. This flip-flop is used to operate with a low-voltage-swing clock. We use this flip-flop to operate with an energy recovery clock. When the clock voltage exceeds the threshold voltage of the clock transistor (MN l), evaluation occurs. At the onset of evaluation, the difference between the differential data inputs (D and DB) is amplified and either SET or RESET switches to low and is captured by the set-reset latch. The SET and RESET nodes are pre-charged high when the clock voltage falls below V_{dd}-V_{tp}, where V_{tp} is the threshold voltage of the precharging transistors (MP1 and MP2).

Although the SAER flip-flop is fast and uses fairly low power at high data switching activities, its main drawback is that either the SET or RESET node is always charged and discharged every cycle, regardless of the data activity. This leads to substantial power consumption at low data switching activities where the data is not changing frequently. We consider two approaches to address this problem. One approach is to use a static flip-flop, and the other is to employ conditional capturing.

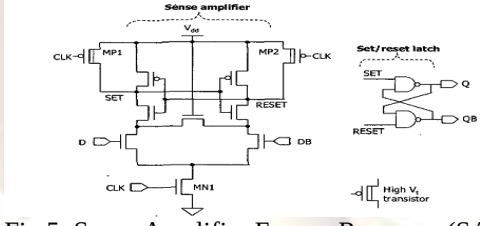


Fig 5: Sense Amplifier Energy Recovery (SAER) flip-flop

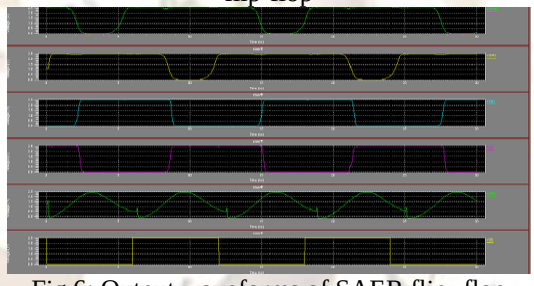


Fig 6: Output waveforms of SAER flip- flop

Figure 7 shows the Static Differential Energy Recovery (SDER) flip-flop. The energy recovery clock is applied to a minimum-sized inverter skewed for fast high-to-low transition. The clock signal and the inverter output (CLKB) are applied to transistors MN l and MN2 (MN3 and MN4). The series combination of these transistors conducts for a short period of time during the rising transition of the clock when both the CLK and CLKB signals have voltages above the threshold voltages of the NMOS transistors. Since the clock inverter is skewed for fast high-to-low transitions, the conducting period occurs only during the rising transition of the clock, but not on the falling transition. In this way, an implicit conducting pulse is generated during each rising transition of the clock. Figure 8 shows typical simulated waveforms of the SDER flip-flop. In this flip-flop, when the state of the input data is the same as its state in the previous conduction phase, there are no internal transitions. Therefore, power

consumption is minimized for low data switching activities.

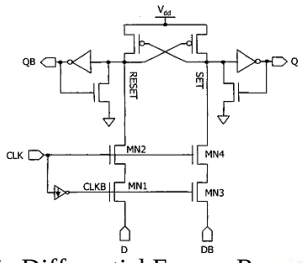


Fig 7: Static Differential Energy Recovery (SDER) flip-flop

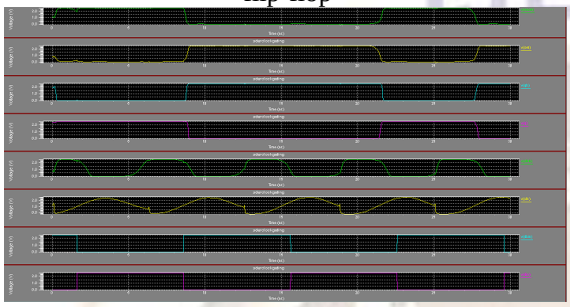


Fig 8: Output waveforms of SDER flip-flop

The second approach for minimizing flip-flop power at low data switching activities is to use conditional capturing to eliminate redundant internal transitions. Figure 9 shows the Differential Conditional-Capturing Energy Recovery (DCCER) flip-flop. Similar to a dynamic flip-flop, the DCCER flip-flop operates in a precharge and evaluate fashion. However, instead of using the clock for precharging, small pull-up PMOS transistors (MP1 and MP2) are used for charging the precharge nodes (SET and RESET). The DCCER flip-flop uses a NAND-based Set/Reset latch for the storage mechanism. The conditional capturing is implemented by using feedback from the output to control transistors MN3 and MN4 in the evaluation paths. Therefore, if the state of the input data is same as that of the output, SET and RESET are not discharged. Figure 10 shows typical simulated waveforms of the DCCER flip-flop.

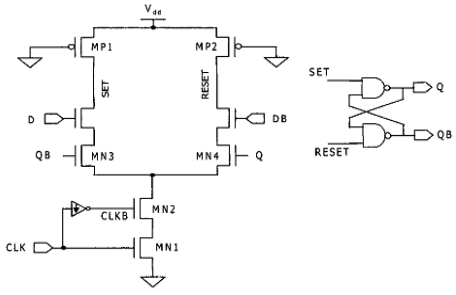


Fig 9: Differential Conditional Capturing Energy Recovery (DCCER) flip-flop

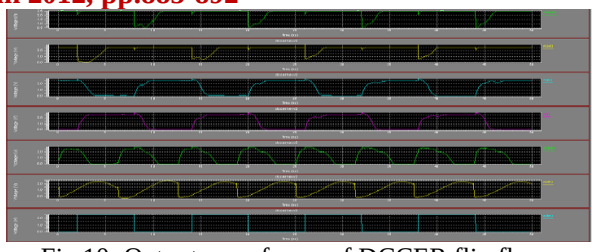


Fig 10: Output waveforms of DCCER flip flop

As can be seen in Figure 10, CLK is generally less than Vdd/2 during a significant part of the conducting window. Therefore, a fairly large transistor is used for MN1. Moreover, since there are four stacked transistors in the evaluation path, significant charge sharing may occur when three of them become ON simultaneously. Having properly sized pull-up PMOS transistors (MP1 and MP2) instead of clock controlled precharge transistors ensures a constant path to Vdd, which helps to reduce the effect of charge sharing. Another property of the circuit that helps reduce charge sharing is that the clock transistor (MNl), which is the largest transistor in the evaluation path, is placed at the bottom of the stack.

Figure 11 shows a Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop. SCCER is a single-ended version of the DCCER flip-flip. The transistor MN3, controlled by the output QB, provides conditional capturing. The right hand side evaluation path is static and does not require conditional capturing. Placing MN3 above MN4 in the stack reduces the charge sharing. Typical simulated waveforms of the SCCER flip-flop are shown in Figure 12.

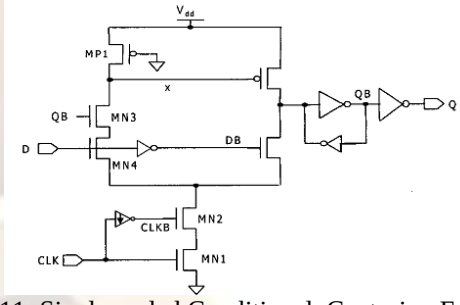


Fig.11: Single-ended Conditional Capturing Energy Recovery (SCCER) flip-flop

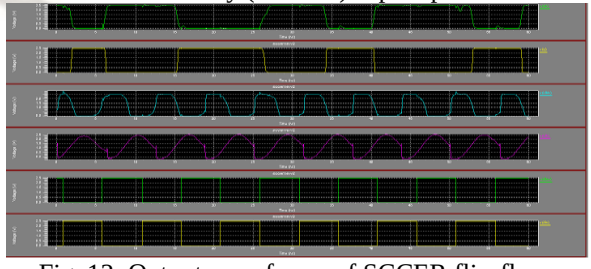


Fig. 12: Output waveforms of SCCER flip-flop

IV. SIMULATION RESULTS AND COMPARISONS

All the flip-flops are simulated using 250nm process technology with a supply voltage of 2.5V in Tanner EDA. Netlists were extracted from schematic and simulated using TSPICE. However, since the FPTG flip-flop is a dual-edge triggered flip-flop, it was designed to operate at a clock frequency of 100MHz. Figure 13 illustrates our timing definitions. Delay is measured between 50% points of signal transitions. Setup time is the time from when data becomes stable to the rising transition of the clock. Hold time is the time from the rising transition of the clock to the earliest time that data may change after being sampled.

The proposed flip-flops are compared with the FPTG flip-flop. For individual flip-flop simulations, an ideal sinusoidal clock was used. Figure 14 shows clock-to-output (CLK-Q) delay and data-to- output (D-Q) delay vs. setup time for all the flip-flops. It is apparent that the delays of the FPTG flip-flop are much larger as compared to the proposed flip-flops. The SCCER flip-flop exhibits the smallest minimum D-Q delay, while the SAER flip-flop shows the smallest CLK-Q delay.

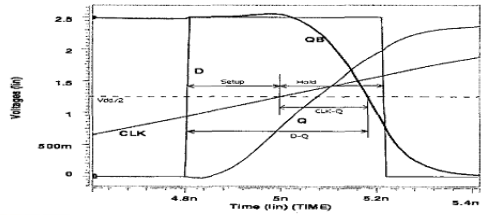


Fig 13: Sample waveforms illustrating timing definitions

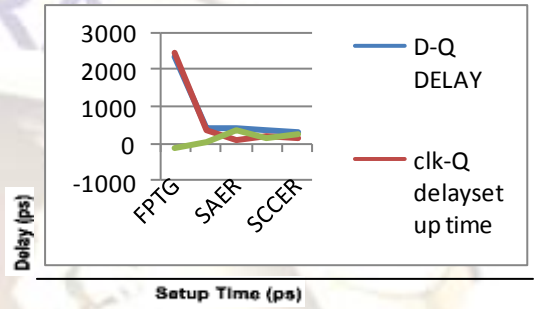


Fig 14: Setup time vs. delay for all flip-flops

Flip-flop	Min D-Q delay (pS)	Setup time (pS)	Hold time (pS)	CLK-Q delay (pS)	Power (µW)	PDP	Normalized PDP	Transistor count
FPTG	2350	-130	830	2470	286.1	673.3	1	16
SDER	405	45	355	340	197.4	79.9	0.11	14
SAER	441	375	-170	81.5	185.2	81.6	0.121	18
DCCER	395	128	165	176.3	142.7	56.3	0.083	18
SCCER	320	285	15	123.5	135.6	43.3	0.064	17

Table 1: Summary of numerical results of flip-flops

Flip-flop	Square wave clock power(µW)	Energy recovery clock power(µW)	% of power reduction by energy recovery clock compared to square clock
SDER	323.1	197.4	38.9
SAER	289.4	185.2	36
DCCER	274.2	142.7	47.9
SCCER	261.8	135.6	48.2

Table 2: Summary of power consumption of flip-flops with different inputs

Flip-flop	Min. D-Q delay (pS)	Setup time (pS)	Hold time (pS)	CLK-Q delay(pS)	Power (µW)	Transistor count
TGFF	415	145	155	246	283	18
HLFF	320	-65	235	255	351	20
CCFF	287	-27	210	210	272	26

Table 3: Summary of numerical results of square wave flip-flops

The energy recovery clock shows the lowest power with all the flip-flops compared to the square wave and sine wave clock. In order to compare with the square wave clocking, three flip-flops that operate with the square-wave clock were also designed. These flip-flops are Hybrid Latch Flip-Flop (HLFF)

and Conditional Capturing Flip-Flop (CCFF), which are high-speed switching activities. The HLFF system has the highest power consumption at low switching activities, and the CCFF system shows the highest power consumption at high switching activities. Table 3 shows the results of square wave flip-flops.

The energy recovery systems show less power consumption as compared to the square-wave clocking. The energy recovery clocking scheme reduces the power due to clock distribution (clock-tree) by more than 90% compared to non-energy recovery (square-wave) clocking. As compared to the HLFF system, the SCCER system shows power savings of 61.3%. Figure 15 shows the H-tree clock network, Table 4 shows the clock tree power comparisons on the clock tree, the energy recovery flip flops are driven by a single phase sinusoidal clock and the square wave flip flops are driven by a square wave clock through a chain of inverters.

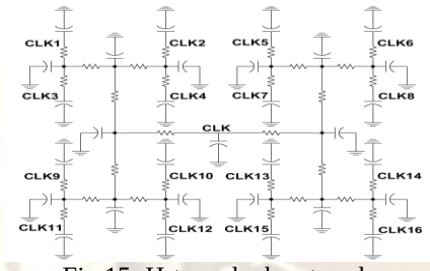


Fig 15: H-tree clock network

Flip-flop	Clock-tree power (mW)
HLFF	50.54
CCFF	52.51
TGFF	55.18
SAER	2.954
SDER	4.154
DCCER	3.096
SCCER	2.894

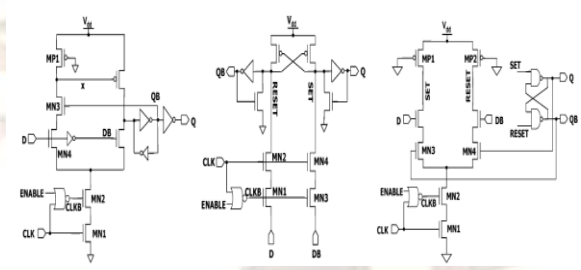
Table 4: Clock tree power comparisons

V. ENERGY RECOVERY CLOCK GATING

The clock power in idle periods can be reduced by the application of the clock gating technique to the energy recovery clock. In this section, we propose techniques for applying clock gating to the energy recovery clocking system in order to obtain additional power savings in the idle mode.

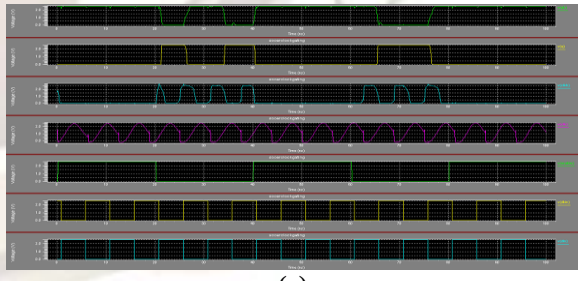
The energy recovery clocked flip-flops cannot save power during sleep mode if the clock is still running. There are two components of power dissipation inside flip-flops: internal clock circuit power (power of logic gates connected to the clock) and the remaining circuit power (power of the rest of the flip-flop circuit). We separated the clock circuit power from the remaining circuit power in our power measurements. Disabling the clock circuit (inverter gates connected to the clock input in Figs. 3–5) in the idle state can eliminate both the clock circuit and remaining circuit power. Hence, disabling of the inverter gates is the proposed approach to implementing clock gating inside energy recovery clocked flip-flops. This can be done by replacing the inverter gate with a NOR gate as shown in Fig. 16. Notice that this clock gating approach is not applicable to the SAER flip-flop since it does not use an inverter in the clock path.

The NOR gate has two inputs: the clock signal and the enable signal. In the active mode, the enable signal is low so the NOR gate be-haves just like an inverter and the flip-flop operates just like the original flip-flop. In the idle state, the enable signal is set to high which disables the internal clock by setting the output of the NOR gate to be zero. Figure 17 shows the output waveforms of the energy recovery clock gating flip flops.

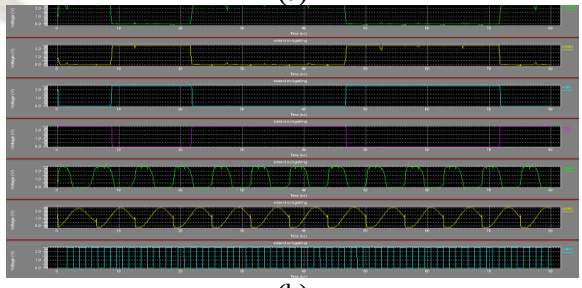


(a) (b) (c)

Fig 16: (a) clock gating SCCER (b) clock gating SDER (c) clock gating DCCER



(a)



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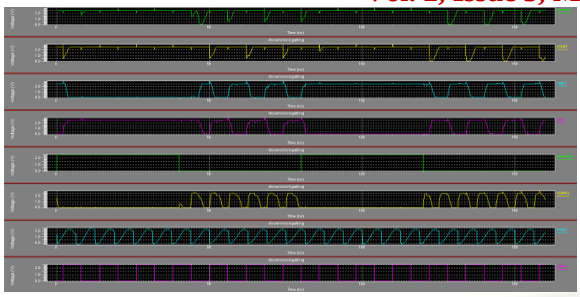

(c)

Fig 17: Output waveforms of (a) clock gating DCCER (b) clock gating SDER (c) clock gating SCCER flip flops

Original Flip flops in Active Mode				Flip flops with clock gating in Active Mode		
	Rema-ining circuit power (µW)	Inter-nal clock power (µW)	Total flip flop power (µW)	Remaini-ng circuit power(µW)	Internal clock power (µW)	Total flip flop pow-er(µW)
SCCER	56.5	11.3	67.8	56.3	11.3	67.8
DCCER	60.2	11.1	71.3	60.5	11.1	71.3
SDER	78.9	19.8	98.7	79.4	19.8	98.7

Table 5: Power consumed by Flip flops with Active mode

Original Flip flops in Sleep Mode				Flip flops with clock gating in Sleep Mode		
	Rema in-ing circuit power (µW)	Intern al clock power (µW)	Total flip flop power (µW)	Remai-ning circuit power(nW)	Intern -al clock power (nW)	Total flip flop power (nW)
SCCER	56.5	11.3	67.8	5.3	3.0	8.3
DCCER	60.2	11.1	71.3	1.3	3.5	4.8
SDER	78.9	19.8	98.7	11.8	2.7	14.5

Table 6: Power consumed by Flip flops with Sleep mode

Table 6 shows results for the power consumed during the sleep (clock gated) mode. Power results show significant savings when the clock gating is applied to the flip-flop during the idle state. Power savings of more than 1000 times are obtained during the idle state when compared to the power consumed without clock gating. The power savings increase with increase in the data switching activity.

VI. PIPELINED ARRAY MULTIPLIER

To demonstrate the feasibility and effectiveness of the proposed energy recovery clocking scheme and flip-flops, a pipelined array multiplier has been designed using the pro-posed clocking scheme. The multiplier is 8x8-bit pipelined multiplier pipelined with SCCER flip flops. The clock inputs of all the flip-flops are connected together through an H-tree type of clock. The logic part of the design is composed of AND and full-adder gates. A similar multiplier has been designed using transmission gate flip-flops and square-wave clock. The clock tree in this multiplier was also H-tree; however, buffers were inserted to properly propagate the square-wave clock through the clock network.

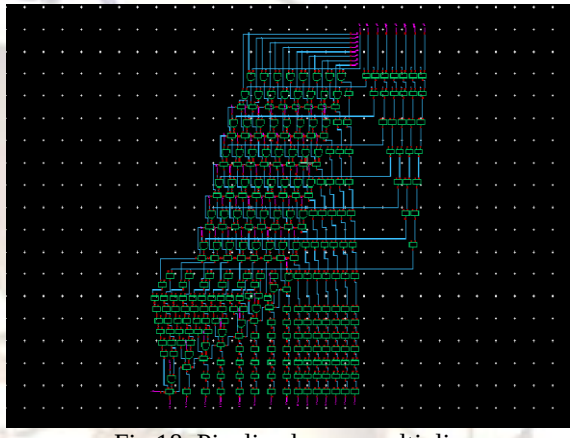

Fig 18: Pipelined array multiplier

Results show a power reduction of 70% on the clock-tree and total power savings of 25%–69% as compared to the same multiplier using conventional square-wave clocking scheme and corresponding flip-flops.

VII. CONCLUSION

We proposed four novel energy recovery flip-flops that enable energy recovery from the clock network, resulting in significant total energy savings compared to the square-wave clocking. The proposed flip-flops operate with a single-phase sinusoidal clock. Results show a power reduction of 90% on the clock-tree and total power savings of up to 81.3% as compared to the same implementation using conventional square-wave clocking scheme and flip-flops. Clock gating in energy recovery clocked flip-flops result in significant power savings during the idle state of the flip-flops. The results demonstrate the feasibility and effectiveness of the energy recovery clocking scheme in reducing total power consumption. Energy recovery clocked pipelined multiplier is designed, results show a total power savings of 25%–69% as compared to the same multiplier using conventional square-wave clocking scheme and corresponding flip-flops.

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