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# A NOVEL CASCADED SERIES/PARALLEL VOLTAGE SOURCES MULTILEVEL INVERTER FOR HIGH POWER DRIVE APPLICATION

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**Abstract— In this paper, a new topology of cascaded multilevel inverter with a high number of steps associated with a low number of switches is presented. A multilevel voltage is obtained by cascading two H-bridges and an inverter. Voltage sources are connected in series/parallel by the switching devices. The size, complexity and power consumption in the gate driving circuits is also reduced. Reduction of rating of the switches is another advantage. The total harmonic distortion (THD) is reduced with more number of steps in output voltage without using pulse width modulation techniques. In this paper a novel topology is proposed to get high 31 levels. The proposed setup configures theoretical approach along with simulations carried on MATLAB/SIMULINK environment. Simulation results are shown and compared with theoretical results.**

**Keywords-component: Multilevel inverter; series/parallel voltage sources; H-bridge**

## I. INTRODUCTION

In the last few years electric vehicles (EVs), hybrid Electric vehicles (HEVs) are studied all over the world due to several advantages like increased fuel efficiency, lower emissions and better vehicle performance. These vehicles that have large electric drives require advanced power electronic inverters to meet the high-power demands.

One of the limitations in these studies when the switching devices are operated at high voltage, switching frequency is restricted. With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices.The multilevel inverter has gained much attention in recent years due to its advantages in high power with low harmonics applications. Multilevel inverters overcome this problem because their individual devices have a much lower voltage per switching and they operate at high efficiencies because they can switch at a much lower frequency than PWM-controlled inverters. A multilevel inverter can reduce the device voltage and the output harmonics by increasing the number of output voltage levels. For this reason, multilevel inverters can easily provide the high power required of a large electric drives. The inverter can be used in hybrid electric vehicles (HEV) and electric vehicles (EV). Several multilevel inverter topologies have been developed like flying capacitor, neutral point clamped, Cascaded H-bridge (CHB). Among these topologies, the cascaded H bridge inverter has received much attention. To increase the output voltage levels, the number of H bridges must be connected in cascade, hence greater number of power semiconductor switches are required. Each switch requires a related gate drive and protection circuits. This may cause the overall system to be more expensive and complex.

Asymmetrical multilevel converters are an alternative to minimizing the harmonic distortion of the output voltages without increasing the number of switching devices. This paper suggests a new topology for multilevel inverters with a high number of steps associated with a low number of gate driver and protection circuits for switches. Reduction of rating of the switches is another advantage. The harmonic content is also reduced. A desired high output voltage is synthesized from several levels of dc voltages that can be batteries, capacitors, fuel cells etc.

## II. PROPOSED TOPOLOGY

The topology of the modified multilevel inverter is shown in Fig. 1. It consists of three bridges, that is two upper H-bridges and the lower H-bridge with series/parallel circuit, which are cascaded. DC voltage sources are connected in series when the switches Sa1-San-1 becomes ON and Sb1-Sbn-1, Sc1-Scn-1 becomes OFF. In parallel when the switches Sb1-Sbn-1 and Sc1- Scn-1 becomes ON, Sa1- San-1 becomes OFF. In series/parallel when the switches, Sa2-San-1, Sb1, Sc1 becomes OFF, current flows in switches Sb2-Sbn-1, Sc2-Scn-1 via the switch Sa1. By using this principle high numbers of steps are obtained at output

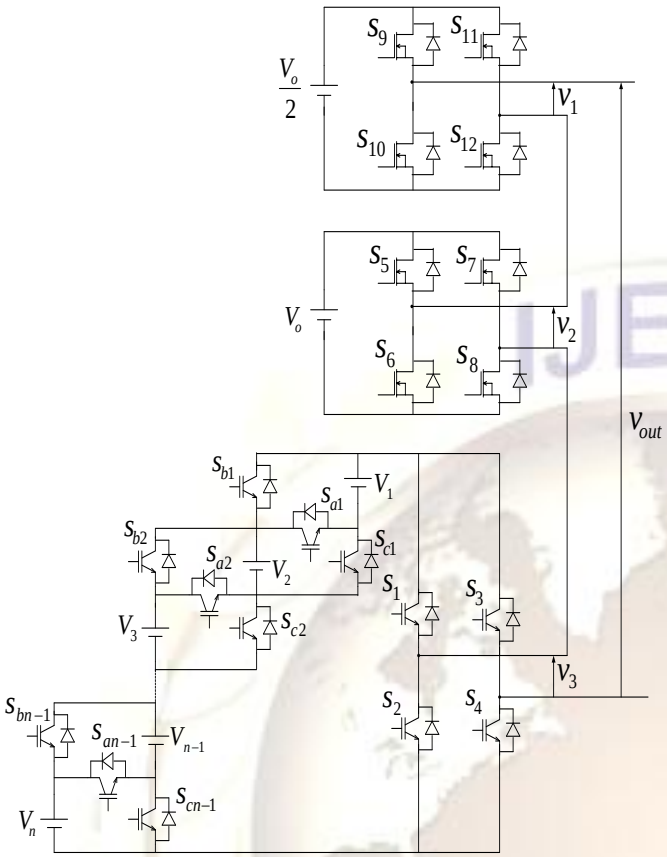


Fig. 1. Proposed topology.

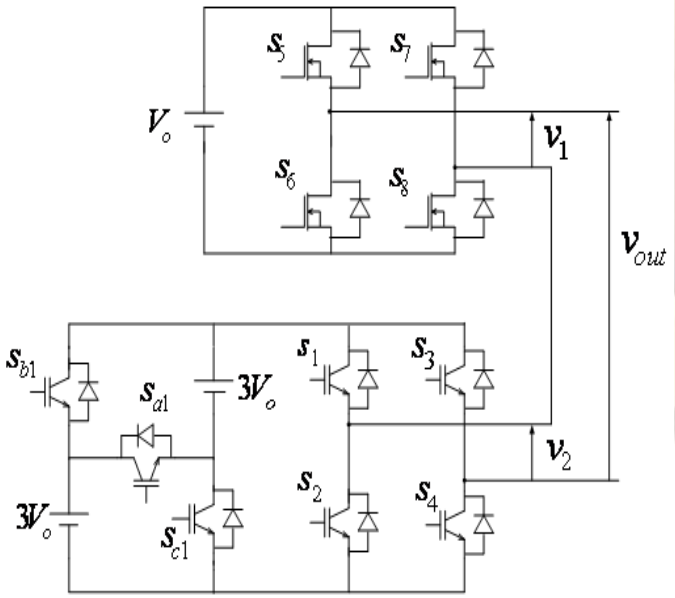


Fig. 2. Proposed topology for 15 Level output.

Fig. 2 shows the proposed topology for 15 level output. Here two H-Bridges are cascaded. One H-Bridge has additional series parallel circuit. Here the voltage ratio of low voltage h-Bridge to high voltage H-bridge is 3 to get fifteen levels.

Table 1 Switching sequence for 15 level output

| | |
|---|---|
| Sa1,S1,S4,S5,S8 | 7Vo |
| Sb1,S1,S4,S5,S8 | 4Vo |
| Sc1,S1,S4,S5,S8 | 4Vo |
| Sa1,S3,S2,S5,S8 | -5Vo |
| Sb1,S3,S2,S5,S8 | -2Vo |
| Sc1,S3,S2,S5,S8 | -2Vo |
| Sa1,S1,S4,S6,S7 | 5Vo |
| Sb1,S1,S4,S6,S7 | 2Vo |
| Sc1,S1,S4,S6,S7 | 2Vo |
| Sa1,S3,S2,S6,S7 | -7Vo |
| Sb1,S3,S2,S6,S7 | -4Vo |
| Sc1,S3,S2,S6,S7 | -4Vo |
| S5,S7,S1,S3 OR S6,S8,S1,S3 | 0 |

The number of output phase voltage levels in a conventional cascade inverter is defined by, m = 2s +1, where s is the number of dc sources. Each H-bridge requires dc source and 4 switches. 12 switching devices are needed for 7 levels, 16 switching devices are needed for 9 levels, 20 switching devices are needed for 31 levels, which makes an inverter complicated.

But the proposed inverter outputs 12n +7 levels, where n is number of voltage sources in series/parallel circuit. Total number of switches devices required are 3n + 9, which makes the output voltage of the inverter almost sinusoidal.

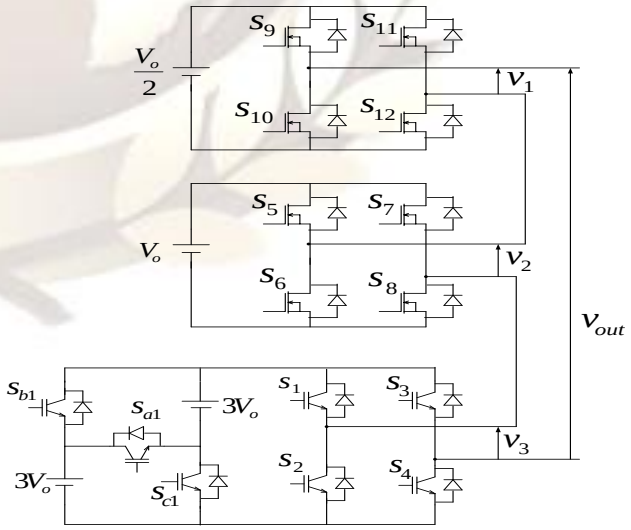


Fig. 3. Proposed topology for 31 level circuit

When the voltage ratio of 1:2:6 is assumed in the H-bridges, the inverter requires 15 switching devices for 31 levels, which is shown in Fig. 3. Two voltage sources are required in series/parallel circuit, levels are obtained by the Eq. (1) and the switching sequence is shown in Table II.

$$v_{out} = v_1 + v_2 + v_3 \quad (1)$$

Table II. Switching sequence

| Switches closed | Vout |
|---|---|
| S2,S4,S6,S8,S10,S12 | 0 |
| S9,S12 | 0.5Vo |
| S5,S8 | Vo |
| S5,S8,S9,S12 | 1.5Vo |
| Sc1,S1,S4,S6,S7 | 2Vo |
| Sc1,S1,S4,S10,S11 | 2.5Vo |
| Sc1,S1,S4 | 3Vo |
| Sc1,S1,S4,S9,S12 | 3.5Vo |
| Sc1,S1,S4,S5,S8 | 4Vo |
| Sc1,S1,S4,S5,S8,S9,S12 | 4.5Vo |
| Sa1,S1,S4,S6,S7 | 5Vo |
| Sa1,S1,S4,S10,S11 | 5.5Vo |
| Sa1,S1,S4 | 6Vo |
| Sa1,S1,S4,S9,S12 | 6.5Vo |
| Sa1,S1,S4,S5,S8 | 7Vo |
| Sa1,S1,S4,S5,S8,S9,S12 | 7.5Vo |
| S10,S11 | -0.5Vo |
| S6,S7 | -Vo |
| S6,S7,S10,S11 | -1.5Vo |
| Sc1,S2,S3,S5,S8 | -2Vo |
| Sc1,S2,S3,S9,S12 | -2.5Vo |
| Sc1,S2,S3 | -3Vo |
| Sc1,S2,S3,S10,S11 | -3.5Vo |
| Sc1,S2,S3,S6,S7 | -4Vo |
| Sc1,S2,S3,S6,S7,S10,S11 | -4.5Vo |
| Sa1,S2,S3,S5,S8 | -5Vo |
| Sa1,S2,S3,S9,S12 | -5.5Vo |
| Sa1,S2,S3 | -6Vo |
| Sa1,S2,S3,S10,S11 | -6.5Vo |
| Sa1,S2,S3,S6,S7 | -7Vo |
| Sa1,S2,S3,S6,S7,S10,S11 | -7.5Vo |

## III. CHOICE OF DEVICES

The use of different dc voltage sources naturally leads to hybrid multilevel topologies, which employ distinct types of semiconductor switches. Devices in two upper H-bridges are operated at low voltage rating, hence MOSFETs are used, devices in lower H-bridge with series/parallel circuit are operated at high voltage rating, hence IGBTs are used

## IV. MATLAB MODELING & SIMULATION RESULTS

The Matlab/Simulink model of the proposed inverter for 31 level output is shown in Fig. 3. It consists of two upper H-bridges cascaded with lower H-bridge and the series/parallel circuit. Simulation is performed for the proposed circuit with MATLAB/SIMULINK version R2009b.

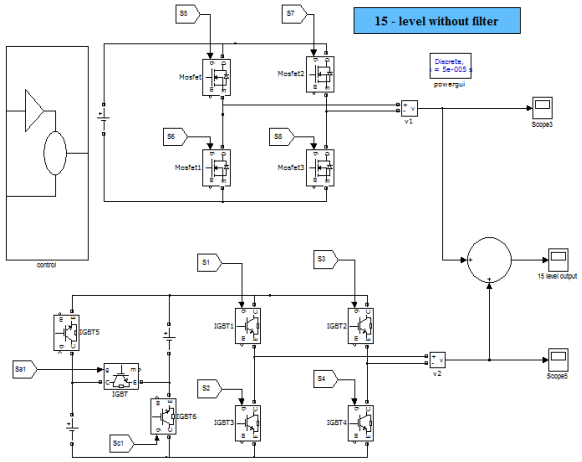


Fig. 4 Matlab/SImulink Model of proposed converter for 15 level output

Fig. 3 shows the Matlab/Simulink model of proposed converter for fifteen level output. Here low voltage H-bridge is modeled with MOSFET and high voltage H-bridge is modeled with IGBT's.

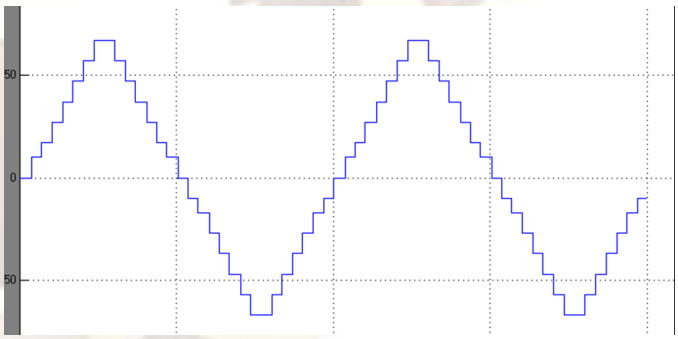


Fig. 5 Fifteen level output

Fig. 5 shows the fifteen level output without PWM. It is clearthat as the number of level increases distortion reduces.

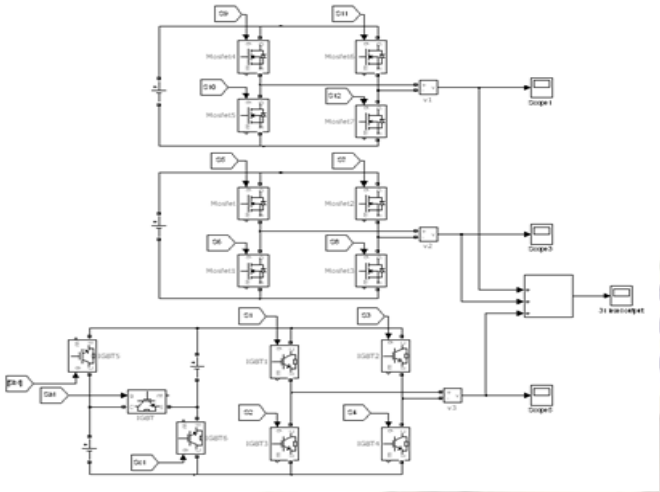

Fig. 6. Matlab/Simulink model.

For 5V, 10V in upper H-bridges, two voltage sources of 30V each in series/parallel circuit then the amplitude of the inverter's output voltage waveform for 31 level is 73.3V.

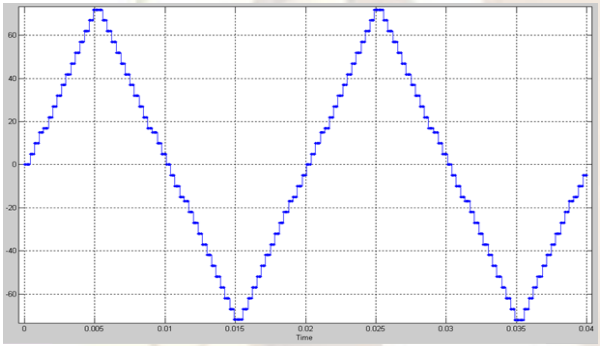

Fig. 7. 31 level output

Fig. 7. Shows the output voltage waveforms of the proposed 31-level. The amplitude of the inverter's output voltage waveform in the simulation is close to the theoretical values

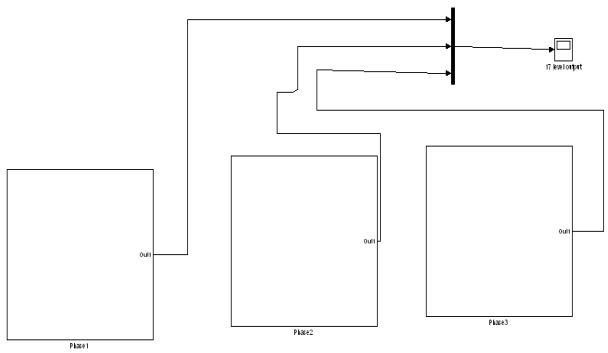

Fig. 8 Matlab/SImulink Model of proposed converter for three phase 31 level output

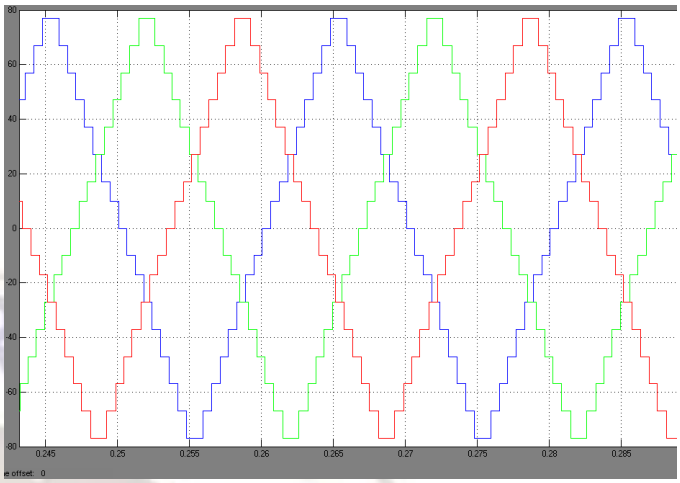

Fig. 9. Three phase 31 level output

Fig. 8 shows the Matlab/SImulink model of three phase 31 level output and Fig. 9 shows the corresponding three phase 31 level output.

## V. CONCLUSION

A new configuration of cascaded multilevel inverter with separate dc sources has been proposed. The suggested topology needs less number of switching devices with minimum standing voltage. THD is also reduced. The simulation results are shown which are accorded with the theoretical results. The proposed inverter is used in high power applications like EV and HEV drives

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