Rajeev Kumar, Kuldeep Singh, Mandeep Singh Saini / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 3, May-Jun 2012, pp. 183- 186

Design of 64 bit Register File for VLIW Processor Architecture

Rajeev Kumar
Assistant Professor IITT College, Deptt of ECE, Pojewal, Punjab

Kuldeep Singh
Assistant Professor, Deptt of Electronic Science, Kurukshetra University, Kurukshetra

Mandeep Singh Saini
Assistant Professor, Deptt of ECE, IITT College,Pojewal,Punjab

Introduction

VLIW stands for Very Long Instruction Word.This Processor Architecture is based on parallel processing in which more than one instructions are executed in parallel. This architecture is used to increase the instruction throughput. So this is the base of the modern Superscalar Processors. Basically VLIW is a RISC Processor. The difference is it contains long instruction as compared to RISC.

During the execution of the program the operands are stored in the General Purpose Register File. Register file is the combination of registers. Depending upon the processor architecture the number of registers inside the register file can be varies. Here the design of 64 bit register file has been presented which contains 32 registers. Now in which register the operand is transfer is decided by the five bit address.

Experimental Work

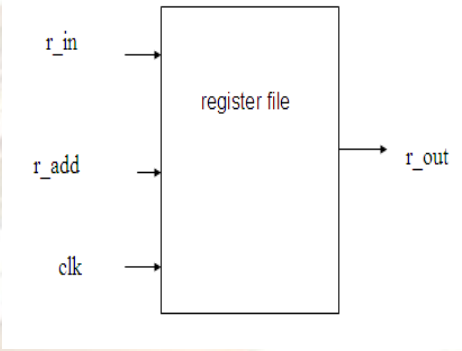
To design 32 registers inside register file the 5 bit address is required. So the encoding of each register is done first. The register starts from r0-r31.

Now the RTL coding is done in Verilog HDL.

Register Name	Register Address
r0	00000
r1	00001
r2	00010
r3	00011
r4	00100
r5	00101
r6	00110
r7	00111
r8	01000
r9	01001
r10	01010
r11	01011
r12	01100
r13	01101
r14	01110
r15	01111
r16	10000
r17	10001
r18	10010
r19	10011
r20	10100
r21	10101
r22	10110

r23	10111
r24	11000
r25	11001
r26	11010
r27	11011
r28	11100
r29	11101
r30	11110
r31	11111

The block diagram of the register file is shown in the following figure. Here r_in is the 64 bit input of the register, r_add is the 5 bit address of each register, and clk is the clock input. For fast triggering negative edge clock is used during the design.r_out is the 64 bit output.



Architecture Design of Register File

When clk signal becomes negative edge triggered then after applying the five bit address the data is stored in the designated register.
So by changing the address we can select the register for the storage of operand.

Experimental Results

Simulation

To check the functionality of the register file simulation is done on Modelsim 6.4a.Now according to the waveform 64 bit data is stored in r_in1 which contains the output r_out1. After the simulation it is found that the clock latency is 24.

Synthesis

Now to generate the gate level netlist Synthesis is done on Xilinx ISE 10.1 by taking Virtex 4 FPGA with **4vsx35ff668** package with speed grade **-12**.After the synthesis the total gate count is 20,756 and additional JTAG gate count for IOBs is 98,688.The number of bonded IOBs are 2,056.

Device Utilization Report

```
Device utilization summary:
---------------------------

Selected Device : 4vsx35ff668-12

 Number of Slices:                1201  out of  15360     7%
 Number of 4 input LUTs:          2090  out of  30720     6%
 Number of IOs:                   2056
 Number of bonded IOBs:           2056  out of    448   458% (*)
    IOB Flip Flops:               1024
 Number of GCLKs:                    1  out of     32     3%
```

Delay Report

```
Timing Summary:
---------------
Speed Grade: -12

   Minimum period: No path found
   Minimum input arrival time before clock: 1.852ns
   Maximum output required time after clock: 3.793ns
   Maximum combinational path delay: No path found

Timing Detail:
--------------
All values displayed in nanoseconds (ns)
```

Final Results and discussion

Parameter	Value
Net Delay	1.163ns
Gate Delay	1.852ns
Gate Count	20,756
Additional JTAG Gate Count	98,688
Bonded IOB	2,056
Speed Grade	-12
Setup Time	1.852ns
Hold Time	3.793ns

Future Work:

In the present design register file contains 32 registers in which each register stores 64 bit data.In future, the registe file can be designed for 64 registers in which each register stores 128 bit data.The another modification is that one can design register file for low power consumption.

References

[1] R.Balasubramonian et al.Reducing the complexity of the register file in Dynamic superscalars.Proc.Ann IEEE/ACM Symp on Microarchitecture,Dec 2001.
[2] A.K Jones, R Hoare, D.Kusic, J Fazekas and J.Foster, "An FPGA based VLIW Processor with custom hardware execution," in Proc. ACM FPGA Symp, Monterey, CA 2005.
[3] A VLIW Processor with Hardware Functions: Increasing Performance while Reducing Power, Alex K Jones, Raymond Hoare, "IEEE Transactions on Circuits and Systems", vol 53, November 2006
[4] Liao, and Roberts, "A High-Performance and Low-Power 32-bit multiply- Accumulate Unit with Single-Instruction-Multiple-Data (SIMD) Feature", IEEE Journal of Solid- State Circuits, Vol. 37, No. 7, July 2002.
[5] ARM System –on –Chip Architecture (2nd-Edition) by Steve Furber published by Addison Wesley ISBN 0-201-67519-6.
[6] J.Zalamea et.al Two- level hierarchichal register file organization for VLIW Processors.Proc.Ann.IEEE/ACM Symp. on Microarchitecture, Dec 2000.
[7] I.Park et al.Reducing register ports for higher speed and lower energy Proc. Ann. IEEE/ACM Symposium on Microarchitecture, Nov 2002.