A DISTINGUISH BETWEEN REVERSIBLE AND CONVENTIONAL LOGIC GATES

B.Raghu kanth*, B.Murali Krishna **, M. Sridhar ***, V.G. Santhi Swaroop*,

*(P.G. Students, Department of Electronics and Communication Engineering, K.L. University, Vijayawada, India)
** (Assistant Professor, Department of Electronics and Communication Engineering, K.L.University, Vijayawada, India)
*** (Associate Professor, Department of Electronics and Communication Engineering, K.L.University, Vijayawada, India)

ABSTRACT
In the last years reversible logic functions has emerged as an important research area. Other fields such as low-power design, optical computing and quantum computing benefit directly from achieved improvements. It is interesting to compare both reversible and conventional gates. Implementing the reversible logic has the advantages of reducing gate counts, garbage outputs as well as constant inputs. Addition, subtraction operations are realized using reversible DKG gate and compared with conventional gates. Reversible logic are also the fundamental requirement for the emerging field of the Quantum computing having with applications in the domains like Nano-technology, Digital signal processing, Cryptography, Communications.

Keywords - Constant inputs, Garbage outputs, Quantum computing, Reversible logic.

I. INTRODUCTION

First of all, we'll restrict our discussion of logic functions to two-valued functions describing switching logic. Energy loss is an important consideration in digital circuit design, also known as circuit synthesis. Higher levels of integration and the use of new fabrication processes have dramatically reduced the heat loss over the last decades. The other part of the problem arises from Landauer's principle for which there is no solution. Landauer's principle states that logic computations that are not reversible necessarily generate kT * log 2 Joules of heat energy for every bit of information that is lost, where k is Boltzmann's constant and T the absolute temperature at which computation is performed. For room temperature T the amount of dissipating heat is small at (i.e. 2.9 *10^{-21} Joules), but not negligible. This amount may not seem to be significant, but it will become relevant in the future.. A reversible logic circuit should have the following features:

· Use minimum number of reversible gates.

· Use minimum number of garbage outputs.

· Use minimum constant inputs.

Consider heat dissipation due to the information loss in modern computers. [1]First of all, current processors dissipate 500 times this amount of heat every time a bit of information is lost. Second, assuming that every transistor out of more than 4 * 107 for Pentium-4 technology dissipates heat at a rate of the processor frequency, for

instance 2 GHz, the figure becomes 4 *1019 * kT ln 2 J/sec. The processor's working temperature is greater than 400 degrees Kelvin, which brings us to 24 * $1021 kT$ ln 2.

II. Reversible Logic Gates

The main object in reversible logic theory is the reversible function, which is defined as follows.

Definition1. The multiple output Boolean function $F(x1; x2; :::; xn)$ of n Boolean variables is called reversible if:
1. The number of outputs is equal to the number of inputs;
2. Any output pattern has a unique preimage.
In other words, reversible functions are those that perform permutations of the set of input vectors.

Definition2. Garbage is the number of outputs added to make an n-input k-output function (($n; k$) function) reversible.
We use the words "constant inputs" to denote the present value inputs that were added to an ($n; k$) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs
    Input + constant input = output + garbage.
The Quantum Cost of 1*1 Reversible gates is zero, and Quantum Cost of 2*2 Reversible gates is one. Any Reversible gate is realized by using 1*1 NOT gates and 2*2 Reversible gates, such as V, V^+ and FG gate which is also known as CNOT gate. The V and V^+ Quantum gates have the property given in the Equations 1, 2 and 3.
V * V = NOT ……………… (1)
V * V^+ = V^+ * V = I ……….. (2)
V^+ * V^+ = NOT ……………. (3)
The Quantum Cost of a Reversible gate is calculated by counting the number of V, V+ and CNOT gates [2],[3].

2.1 NOT Gate
The simplest Reversible gate is NOT gate and is a 1*1 gate. The Reversible 1*1 gate is NOT Gate with zero Quantum Cost is as shown in the Figure 1.

Figure1. NOT gate

2.2 Feynman / CNOT Gate
Controlled NOT (CNOT) gate is an example for a 2*2 gate. The Reversible 2*2 gate with Quantum Cost of one having mapping input (A, B) to output (P = A, Q = A B) is as shown in the Figure 2.

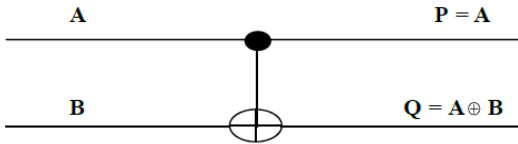Figure2. Feynman/CNOT gate

There are many 3*3 Reversible gates such as F, TG, PG and TR gate.

2.3 Toffoli Gate

The 3*3 Reversible gate with three inputs and three outputs. The inputs (A, B, C) mapped to the outputs (P=A, Q=B, R=A.B C) is as shown in the Figure 3.
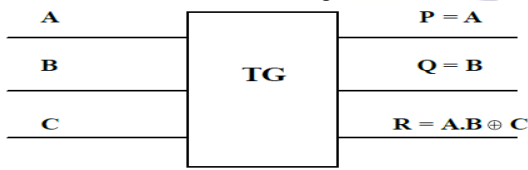

Figure3 Toffoli gate.

Toffoli gate [4] is one of the most popular Reversible gates and has Quantum Cost of 5.

2.4 Peres Gate

The three inputs and three outputs i.e., 3*3 reversible gate having inputs (A, B, C) mapping to outputs (P = A, Q = A B, R = (A.B) C). Since it requires 2 V+, 1 V and 1 CNOT gate, it has the Quantum cost of 4.
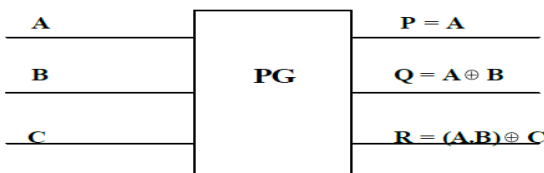

Figure4. Peres gate

2.5 Fredkin Gate

Reversible 3*3 gate maps inputs (A, B, C) to outputs (P=A, Q=A'B+AC, R=AB+A'C) having Quantum cost of 5 and it requires two dotted rectangles, is equivalent to a 2*2 Feynman gate with Quantum cost of each dotted rectangle is 1, 1 V and 2 CNOT gates. Fredkin gate and are shown in Figure 7 respectively[4].
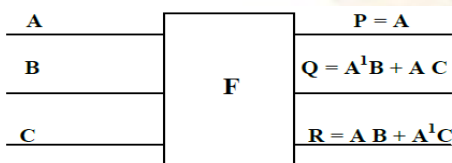

Figure5. Fredkin gate

II. Reversible Logic DKG Gate

A 4* 4 reversible DKG gate [6] that can work singly as a reversible Full adder and a reversible Full subtractor is shown in Fig 6a. It can be verified that input pattern corresponding to a particular output pattern can be uniquely determined. If input A=0, the proposed gate works as a reversible Full adder, and if input A=1, then it works as a reversible Full subtractor. It has been proved that a reversible full-adder circuit requires at least two garbage outputs to make the output combinations unique [5], [6].
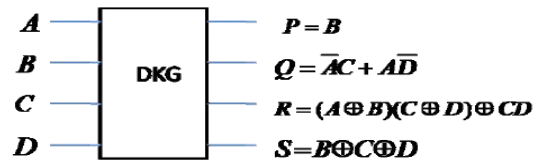

Fig 6a: Reversible DKG gate [6]

The binary Full adder/subtractor is capable of handling one bit of each input along with a carry in/borrow in generated as a carry out/ borrow from addition of previous lower order bit position. If two binary numbers each consisting of n bits are to be added or subtracted, then n binary full adders/subtractors are to be cascaded.
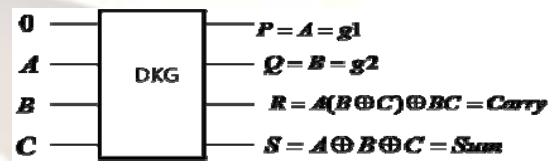

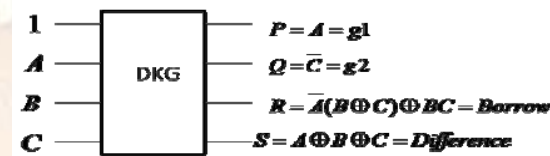Fig 6b: DKG gate implemented as Full adder [6]

Fig6c: DKG gate implemented as Full subtractor [6]

A Parallel adder/subtractor is an interconnection of full adders/subtractors and inputs are simultaneously applied. The carry/borrow generated at a stage is propagated to the next stage. When the control input A=0, the circuit acts as a parallel adder, produces a 4 bit sum and a carry out, as shown in Fig 7a. If the control input A=1, the circuit acts as a parallel subtractor, produces a 4 bit difference and a borrow out, as shown in Fig 7b.
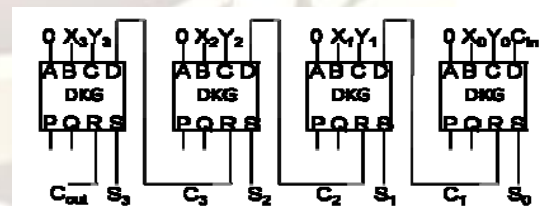

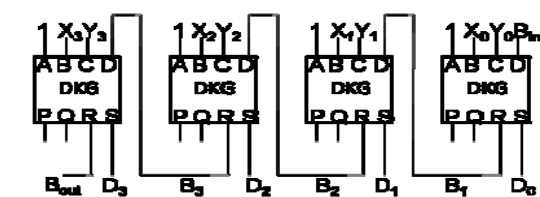Fig 7a: Reversible Parallel adder when A/S=0

Fig 7b: Reversible Parallel subtractor when A/S=1

A 4 bit reversible parallel adder/subtractor is implemented using the reversible DKG gate and shown in Fig 7a and 7b.

IV. Conventional Logic Gates

In this section we discussed mainly about the 'ripple carry adder'. As in section III the reversible logic is also developed on this ripple carry mode we are also compared with the same model in conventional gates. The ripple carry adder is constructed by cascading full adders (FA) blocks in series. One full adder is responsible for the addition of two binary digits at any stage of the ripple carry. The carryout of one stage is fed directly to the carry-in of the next stage. A number of full adders may be added to the ripple carry adder or ripple carry adders of different sizes may be cascaded in order to accommodate binary vector strings of larger sizes. For an n-bit parallel adder, it requires n computational elements (FA). Figure 4 shows an example of 4-bit ripple carry adder. It is composed of four full adders. The augends' bits of x are added to the addend bits of y respectfully of their binary position. The carry out is then transmitted to the carry in of the next higher-order bit. The final result creates a sum of four bits plus a carry out (c4)[7].
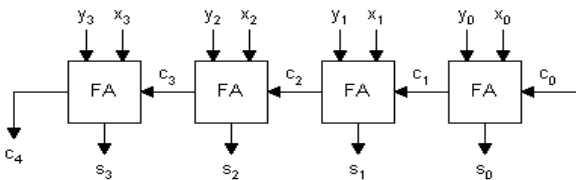

Fig8. 4-bit ripple carry adder.

Even though this is a simple adder and can be used to add unrestricted bit length numbers, it is however not very efficient when large bit numbers are used. In similar fashion the 4-bit subtractor is also done. The difference and borrow are obtained in place of sum and carry of ripple carry adder model represented in the above figure8 respectively.

V. Comparison and Results

The total comparison work is carried out in between the reversible and conventional logic gates by using XILINX 9.1and program is written in VHDL language. In reversible logic we use DKG gate for both adder/subtractor as it has low power consumption and less garbage output as already discussed in the section III. The comparison is carried out for the four operand four bit adder/subtractor in reversible and conventional gates.
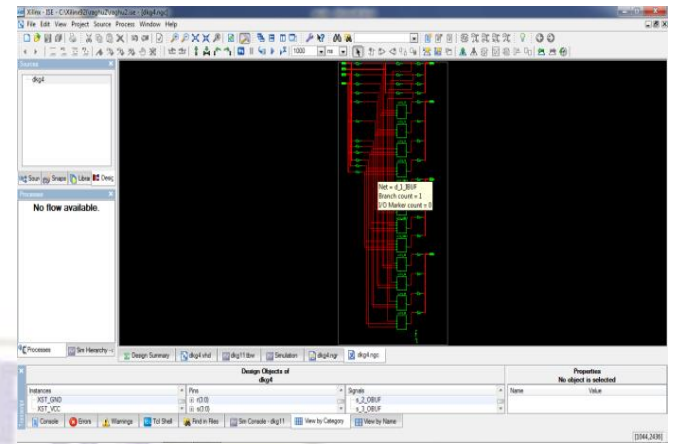

Fig9. Four bit DKG Adder.

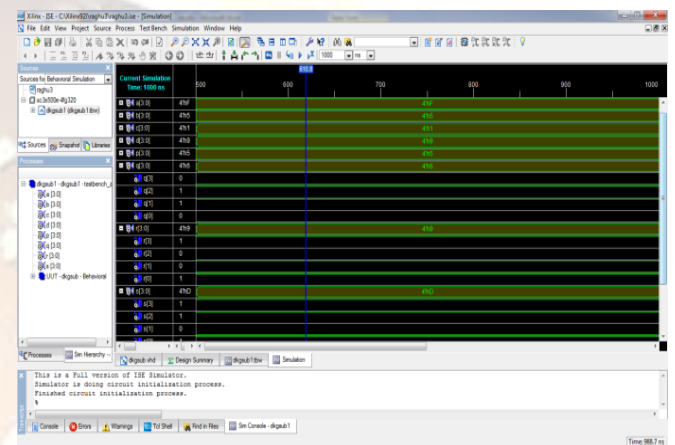Fig10. Technological view of four bit DKG gate adder.

Fig11. Four bit DKG subtractor.

Fig12. Technological view of four bit DKG subtractor.

Table 1 discuss about the delay and power consumption of the four bit reversible and conventional gates simulated in XILINX. Table 1 is stated below. The results which are furnished in the table are obtained by simulating the code in XILINX which is written in VHDL in Ripple Carry Adder Model.

PARA-METER	BASIC 4-BIT ADDER	BASIC 4- BIT SUBTRACTOR	REVERSIBLE DKG ADDER 4- BIT	REVERSIBLE DKG SUBTRACTOR 4- BIT
POWER (W)	0.081073	0.08173	0.08143	0.08143
DELAY (NS)	9.882	9.882	7.850	7.850

TABLE 1 Comparison of power and delay for 4-bit reversible and conventional adder and subtractor in XILINX

In this paper the authors also developed the code for 1-Bit adder for the same reversible and conventional logic gates in VERILOG HDL and simulated in CADENCE TOOL and XILINX 9.1 version. Table 2 discuss about the comparison of the some important parameters of adder simulated in CADENCE and   XILINX as mentioned earlier.
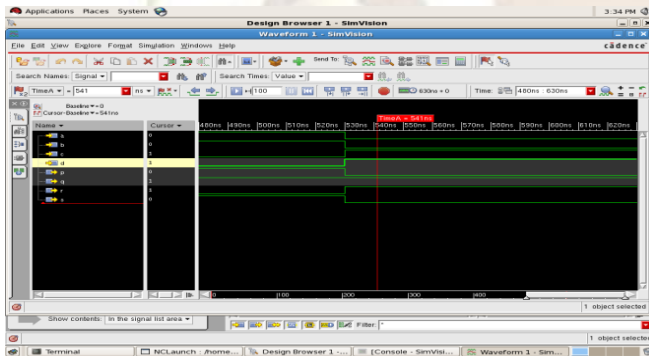

Fig13. 1- Bit DKG gate full adder in CADENCE

Table2. Comparison of 1-bit adder in Xilinx and cadence for reversible and conventional gates.

PARA-METER	CONVENTIONAL 1-BIT ADDER IN XILINX.	REVERSIBLE1-BITDKG ADDER IN XILINX	REVERSIBLE 1-BIT DKG ADDER IN CADENCE
POWER(mw	81	0.08143(W)	675.275(nw)
DELAY(ns)	6.236	7.850	0.571
AREA	16%	18%	23%
LUT`S	2	12	DON`T KNOW

VI. Conclusion

In this paper, we compared 4-bit reversible adder/subtractor circuit using DKG gate. Table1 demonstrates the basic comparison of the power and delay for conventional gates and reversible gates Furthermore, the restrictions of reversible circuits were highly avoided. Table2 demonstrates that the comparison is carried out for reversible adder circuit is better than the existing designs in terms of having low power consumption and lesser delay, number of gates, garbage outputs and constant inputs. Our proposed reversible adder/subtractor circuit can be applied to the design of complex systems in nanotechnology. All the proposed circuits are technology independent since quantum logic and Optical logic implementations are not available.

References

1. Reversible logic synthesis by Dmitri Maslow in MCS University of New Brunswick, 2002.
2. Low power reversible parallel binary adder/subtractor by Rangaraju H.G, Venugopal U, Muralidhara K.N, Raja K.B.
3. "An improved design of a multiplier using reversible logic gates" in IJEST by Bhagya Lakshmi and Venkatesa.
4. "Design of low power arithmetic unit based on reversible logic" in International Journal of VLSI and signal processing applications, ISSN 2231-3133.
5. "Optimal design of a reversible full adder" in International Journal of unconventional computing by Yvan Van Rentergen and Alexis De Vos.
6. "A novel design of reversible serial and parallel adder/subtractor" in International journal of engineering science and technology by Krishnaveni.D and Geetha priya.M.
7. Parallel adders from Google website.
8. www. Wikipidea. Org.