Ultra high speed wideband rate conversion architectures based on Cascaded Integrator comb (CIC) filters

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ABSTRACT

Software defined radio (SDR) is a radio in which the properties of carrier frequency, signal bandwidth, modulation, and several other characteristics are defined by software. Today's SDR is turning the hardware problems into software problems, some or all of the physical layer functions are software defined. Digital down conversion (DDC) is one of the core technologies in SDR, as well as an important component of digital intermediate frequency receiver system.

When a wide band signal is to be rate converted to a different clock frequency then special filter architectures running at high clock rates are required. Normal FIR architectures and its variants fail to work at such high frequencies. Cascaded Integrator comb (CIC) decimation filter is useful to reduce the data sampling rate such high bandwidth applications.

In this project a full fledged digital down conversion system will be developed in VHDL for FPGA based software defined radio applications. The CIC based architecture will be implemented in VHDL and will be tested on Xilinx FPGAs. The major blocks in design would include digital I and Q carrier generators, digital mixers, decimating/interpolating CIC filters and clock distribution circuits. The blocks such as, adder, multipliers, registers and clock & control circuitry will be used in implementing these blocks.

Modelsim Xilinx Edition (MXE) will be used for simulation and functional verification. Xilinx ISE will be used for synthesis and bit file generation. The Xilinx Chipscope will be used to test the results on Spartan 3E 500K FPGA board.

Keywords-SOPC; IP Core; FPGA; cascaded integrator comb decimation filter

I. Introduction:

Software defined radio (SDR) is a radio in which the properties of carrier frequency, signal bandwidth,

modulation, and network access are defined by software. Today's SDR is turning the hardware problems into software problems, some or all of the physical layer functions are software defined.

Digital down conversion (DDC) is one of the core Technologies in SDR, as well as an important component of digital intermediate frequency receiver system. CIC decimation filter is widely applicable to reduce the data sampling rate in DDC. This design makes use of SOPC technology which uses the tool of SOPC Builder component editor to design a new modify parameters component. The project developers can add the component to system directly, and use the component in other project or share the component with other designers. It not only avoids the duplication of work ,but also adds numbers of other IP core resources to build a SOPC system. In this paper, we use a OUI which SOPC Builder provides to design the hardware of CIC decimation filter component. We design the software driver files for the hardware of CIC component, generate a component and establish an SOPC system in SOPC Builder. Finally, the designed system is downloaded to the device and verified in FPGA.

II. Why DDC?

In digital signal processing, a digital down-converter (DDC) converts a digitized real signal centered at an intermediate frequency (IF) to a base banded complex signal centered at zero frequency. In addition to down conversion, DDC's typically decimate to a lower sampling rate, allowing follow-on signal processing by lower speed processors.

A DDC consists of three subcomponents: a direct digital synthesizer (DDS), a low-pass filter (LPF),

and a down sampler (which may be integrated into the low-pass filter).

Digital Down-Converter (DDC) is a key component of digital radios. The DDC performs the frequency translation necessary to convert the high input sample rates found in a digital radio, down to lower sample rates for further and easier processing.

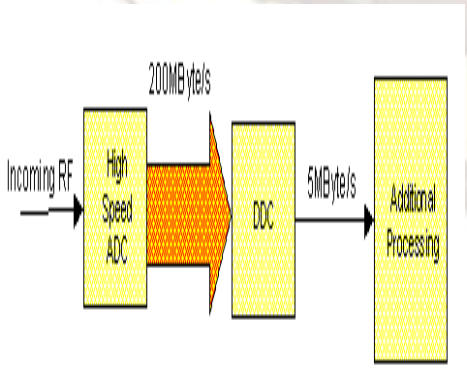
The DDC consists of a Numeric Controlled Oscillator (NCO) and a mixer to down convert the input signal to baseband. The baseband signal is then low pass filtered by a Cascaded Integrator-Comb (CIC) filter followed by two FIR decimating filters to achieve a low sample-rate.

The DDS generates a complex sinusoidal signal at the intermediate to down converting by creating a difference signal at the IF minus the DDS frequency, they also up convert, generating an unwanted signal at the sum of the two frequencies.

A fundamental part of many communications systems is Digital down Conversion (DDC). Digital radio receivers often have fast ADC converters delivering vast amounts of data; but in many cases, the signal of interest represents a small proportion of that bandwidth. A DDC allows the rest of that data to be discarded, allowing more intensive processing to be performed on the signal of interest.

As an example, consider a radio signal lying in the range 39-40MHz. The signal bandwidth is 1MHz. However, it is often digitized with a sampling rate over 100MHZ, representing in the region of 200Mbyte/second.

The DDC allows us to select the 39-40MHz band, and to shift its frequency down to baseband. Once this is complete, the sampling rate can be reduced – with a 1MHz bandwidth, a sampling rate of 2.5MHz would be fine - giving a data rate of only 5Mbyte/second. This is shown in Figure.



An Overview of DDC Function..

Any suitable low-pass filter can be used including FIR, IIR and CIC filters. The most common choice is a FIR filter for low amounts of decimation (less than ten) or a CIC filter followed by a FIR filter for larger down sampling ratios.

DDC's are most commonly implemented in logic in field-programmable gate arrays or application-specific integrated circuits. While software implementations are also possible, operations in the DDS, multipliers and input stages of the low pass filters all run at the sampling rate of the input data. This data is commonly taken directly from analog to digital converters (ADC's) sampling at tens or hundreds of MHz, which is beyond the real time computational capabilities of software processors.

The front end part of many communications systems is Digital Down Conversion (DDC). This allows a signal to be shifted from its carrier (or IF) frequency down to baseband. The technique greatly simplifies the amount of effort required for subsequent processing such as correlation, demodulation etc.

The conventional analog radio uses analog down conversion which does not have scope for reconfigurability. From last two decades the digital down conversion is performed in processor kind of environment which overcomes the disadvantages of analog technique to some extent. In the current technology either ASICs or FPGAs are used for this purpose. The DDC ASICs are of two types; ASICs implemented for standard protocols like GSM, CDMA, WCDMA etc. Second category is the ASICs implemented for wide range of applications. Texas instruments GC4016 can be considered as an example for second category of ASICs.

III. Cascaded Integrator comb (CIC) decimation filter ARCHITECTURE:

The CIC filter architecture is based on the FIR Pre filtering techniques, it first proposed by Hogenauer There are two forms of CIC filter: One is decimation filter, the other is interpolation filter. The CIC decimation filter is the concatenation of integrators and comb filters, it consists of an integrator section operating at the high sampling rate, a decimator section and a comb filters section operating at the low sampling rate . The integrators section and comb Filters section are separated b y decimator section.

The impulse response of the CIC decimation filter can be

Expressed as:

$$h(n)=\begin{cases}1 & 0\le n\le RM-1\\ 0 & other\end{cases} \quad (1)$$

From (1), R is decimation rate, M is differential delay factor.

Z-domain transfer function:

$$H(z)=\sum_{n=0}^{RM-1}h(n)\times z^{-n}=\frac{1-z^{-RM}}{1-z^{-1}}=H_1(z)\times H_2(z) \quad (2)$$

Integrator transfer function:

$$H_1(z)=\frac{1}{1-z^{-1}} \quad (3)$$

Comb filters transfer function:

$$H_2(z)=1-z^{-RM} \quad (4)$$

Fig. 1 shows the basic implementation diagram of the multi-stage CIC decimation filter.

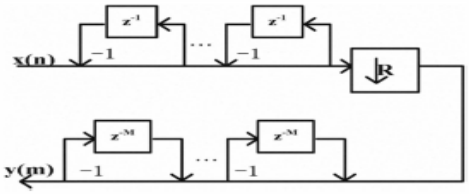


Figure 1. multi-stage CIC decimation filter implementation diagram

Determinate factors of the performance of N-stage CIC decimation filter. The parameter N is used to control the stop band attenuation, stop band attenuation will be greater with the increase of N, but the pass band aliasing droop becomes worse. So N can not choose too large, N is usually not more than 5. The differential delay factor M is used to control the zero position, the increase of M can effectively reduce the pass band aliasing, but the main lobe of the pass band attenuation will be too large, so M is usually set to 1 or 2. Decimation factor R is used to determine the sampling frequency of the signal after decimate. R determines the main lobe and side lobe width with the delay factor M together. In this design, we select N= 5, M= 2, decimation factor R can be adjustable.

IV. IMPLEMENT OF CIC DECIMATION FILTER IP COREL:

Usually, the user defined IP core consists of two main sections: hardware design and software design. Hardware design includes three sections: task logic, register and Avalon bus interface. Software design includes five main files: driver header file, register header file, driver source code file, configuration file and test file.

A. Hardware Design:

VHDL (VHSIC description language) is used to describe the hardware design section. The component editor in SOPC Builder provides a GUI to create the Hardware design of CIC decimation filter IP Core.

In the hardware design section, the VHDL document is altrea avalon cic.vhd. In this document, the definition of the entity conclude system clock signal (CLK), input signal (DIN), output signal (DOUT, CLK2), Avalon bus interface signals, two generic variables n and m: n sets the median of output signal, n can be set to the maximum output of 8 bits; m is the decimation factor, m can be set to the maximum extraction of 24 times.First, in the VHDL document, we define the task logic of the CIC decimation filter IP core, the input signals send in the input signal register (din Jeg), the data of din Jeg access to a fifth-order integral section, then through a decimator.
section with decimation factor R, export the output signal clk2 which is the clock of comb filters section. The data of integral register access to comb filters section, finally get the output signal DOUT. Second, we define two registers which achieve the signal of task logic to exchange the information of the outside world. The registers section include three register: control register (ctlJeg) and the input signal register. Table 1 shows the list of internal registers. Meanwhile set three registers' separate offset that mapped the Avalon port address space. Avalon user interface use the base address + offset to read and write each register.

TABLE I. INTERNAL REGISTERS

Register	Offset	Access	Description
din_reg	01	R/W	input signal
ctl_reg	10	R/W	output enable

The programs which define the internal registers' address are as follows:

```
process(address)
begin
  int_reg_selected<='0';
  din_reg_selected<='0';
  ctl_reg_selected<='0';
  case address is
```

```
when"O 1" =>dinJ eg_ selected<='l' ;
when"l O"=>ctlJeg_selected<='l' ;
when others=>null;
end case;
end process;
```

Third, we use Avalon Slave interface to design the CIC component Avalon bus interface, Avalon Slave uses less Avalon signal to read and write internal registers. In this design, the CIC component is an Avalon Slave peripheral interface component. Table 2 shows the list of Avalon Interface Signal.

TABLE II AVALON INTERFACE SIGNAL

Signal Name in HDL	Interface	Avalon Signal Type	Bit Width	Direction
clk	clk	clk	1	input
reset_n	clk	reset_n	1	input
clk2	clk2	export	1	output
dout	dout	export	n-1	output
chipselect	avalon_slave	chipselect	1	input
address	avalon_slave	address	2	input
write	avalon_slave	write	1	input
writedata	avalon_slave	writedata	32	input
read	avalon_slave	read	1	input
byteenable	avalon_slave	byteenable	4	input
readdata	avalon_slave	readdata	32	output

B.Soft ware Design:

The Nios II IDE development flow is an integrated environment in which you can create, modify, build, run, and debug Nios II programs with the Nios II IDE GUI. The Nios II IDE flow does not use the Nios II Software Build Tools.
The makefiles it creates cannot be user-managed. This flow provides limited control over the build process and the project settings, with no support for customized scripting. We provide software drivers files for the CIC component hardware, and create a software driver to integrate into the Nios II hardware abstraction layer (HAL) [6]. CIC software section is the design of the CIC drivers and applications, the drivers include register macro, CIC statement function prototypes and CIC functions. The functions of applications can read and write the data of these registers, control the output of CIC component, and illuminate the LED display Module on SOPC comprehensive experimental testbed. The first step of software design is creating a device registers header file which uses to describe the registers of equipment. In this design, the device registers header file is altera avalon cic Jegs.h. It not only to uses the macro symbols to describe the use of three registers, but also gives the method to write or read registers. Take the input signal register as an example:
I)
lORD ALTERA AVALON CIC DIN REG(base)
- - - - - IORD(base,
IOWR AL TERA A V ALON_ CIC DIN REG(base,data
IOWR(base, I,
data)
ALTERA AVALON CIC DIN REG MSK
- - - - - (OxFFFFFFF
)
AL TERA AVALON CIC DIN_REG OFST
(0)
The altera avalon cic routines' file is the driver header file, this file declares-the-function prototypes which access CIC decimation filter IP core.The altera avalon cic routines.c is the driver source code file which defines and writes the CIC decimation filter component functions.To facilitate the project management and compilation,the software design provides three documents: Mak efile,altera avalon cic sw.tcl, altera avalon cic hw.tcl.The altera avalon cic sw.tcl document is the softwaredriver configuration document, it specifies the path of .H and. C document that associate with the CIC components.The altera avalon cic hw.tcl is a component file which used to define the output of the IP core hardware design section, it generates automatically when use the component editor to create component in SOPC Builder system, the component editor saves it in the directory where the source VHDL file is located.

C. Equipment Verification:

In Quartus II 7.2, we establish a new project, we use SOPC Builder component editor to mak e the hardware design and software design to package into a CIC decimation filter component, and mak e the CIC component appear in SOPC Builder's list of available components, we can use the component in other project and share the component with other designers. We add CPU, RAM, JTAG IP core resources, generate a simple SOPC system. The Fig. 2 is the CIC component top level block diagram. Compile this system in Quartus II 7.2, and the designed system is downloaded to SOPC comprehensive experiment testbed which conclude the EPICI2Q240C8N device, LED display module, JTAG interface, LCD display module, etc. In order to verify the performance of the CIC component, a new project is established in NIOS II, we write the test document, compile and run the test program.

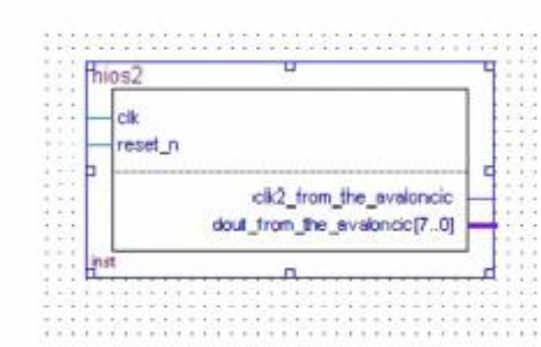


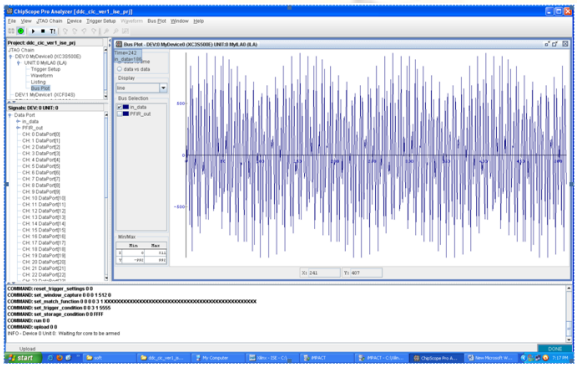
Figure 2. Top level block diagram

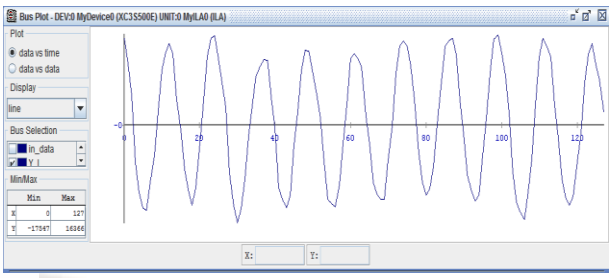
In this design, the generic variables n is set to 8, so the output signal is 8 bits. We observe the running phenomenon of LED display module on SOPC comprehensive experiment testbed, extract briefly the running results of LED display module in different parameters and input signals. The results is verified the correctness of the system. Table 3 shows the running results of LED display module. In the LED display Column, there are eight little lights in LED display module display the results of output signal, we use" I" to indicate the little light is on, use "0" to indicate the little light is off.

TABLE III. LED DISPLAY

Stage N	Differential delay factor M	Decimation factor R	Input Din	LED display
5	2	20	1	10100000
5	2	20	3	11100000
5	2	20	4	10000000
5	2	24	1	00100000
5	2	24	3	01100000
5	2	24	4	10000000

CIC based DDC - Chipscope results:





V. Conclusion & Future Work:

This paper researches on the theory of CIC decimation filter structure. In SOPC Builder, we use the component editor to design a new modify parameters CIC decimation filter component which selecting N= 5, M= 2, R can be adjustable. Then we add other relevant components to build a SOPC system. Aiming at validating on FPGA, we establish a test file to run the SOPC system in NIOS II. At last we download the system to the EPICI2Q240C8N device on the SOPC comprehensive experiment testbed, observe results of LED display module in different parameters and input signals. Experimental results show that the designed CIC decimation filter component can be implemented successfully based on FPGA, and proves that the functions of CIC decimation filter component are programmable, reliable, and portable.

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