Ila Gupta, Neha Arora, Prof. B. P. Singh / International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 2, Mar-Apr 2012, pp.1492-1496

New Design of High Performance 2:1 Multiplexer

Ila Gupta
Deptt. Of ECE
FET-MITS (Deemed University)
Lakshmangarh

Neha Arora
Deptt. Of ECE
FET-MITS (Deemed University)
Lakshmangarh

Prof. B. P. Singh
Deptt. Of ECE
FET-MITS (Deemed University)
Lakshmangarh

ABSTRACT
Recently low power circuits have become a top priority in modern VLSI design. This paper presents post layout simulations of a new improved 2:1 multiplexer design. The proposed design demonstrates its superiority against existing 2:1 multiplexer design in terms of power–delay product (PDP), temperature sustainability, noise immunity and frequency. All the post-layout simulations have been performed at 45nm technology on Tanner EDA tool version 13.0

Keywords **- CMOS Logic, 2:1 multiplexer, low power, power consumption, speed and VLSI.**

I. INTRODUCTION
The increasing prominence of portable systems and need to limit power consumption has led to rapid and innovative developments in low power VLSI design during recent years. The driving forces behind these developments are portable device applications requiring low power consumption and high throughput due to their small chip size with large density of components, increased complexity and high frequencies. A 2:1 multiplexer is a basic building block of the "switch logic". The multiplexer circuit is typically used to combine two or more digital signals onto a single line, by placing them there at different times. Technically, this is known as time-division multiplexing. Multiplexers can also be used as programmable logic devices. By specifying the logic arrangement in the input signals, a custom logic circuit can be created. The selector inputs then act as the logic inputs. This is especially useful in situations when cost is a factor and for modularity. Therefore study on multiplexer is inevitable [1].

IC Layout or mask design is the representation of an integrated circuit in terms of planar geometric shapes which correspond to the patterns of metal, oxide, or semiconductor layers that make up the components of the integrated circuit. In other words, layout is the process by which a circuit specification is converted to a physical implementation with enough information to deduce all the relevant physical parameters of the circuit. The paper is organized as follows: Section II describes an existing 2:1 multiplexer design as reported in the literature. Section III introduces the proposed 2:1 multiplexer design. Simulation results and their comparisons are included in Section IV and finally Section V concluded the paper.

II. PRIOR WORK
In this paper, we explore the Differential Cascode Voltage-Switch Logic (DCVSL) circuit design methodology. The key benefits of DCVSL are consumes no static power (like standard CMOS), uses latch to compute output quickly, requires true/complement inputs, produces true/complement outputs [2]-[4]. Allows "Complex" gates, never needs inverters in the logic path and low power consumption. A logic function and its inverse are automatically implemented in this logic style [4], [5].

TABLE I. Truth table of 2:1 multiplexer

S	A	B	Z
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

The schematic diagram and layout design of existing DCVSL 2:1 multiplexer is shown in Fig1 and Fig2. The pull-down network implemented by the NMOS

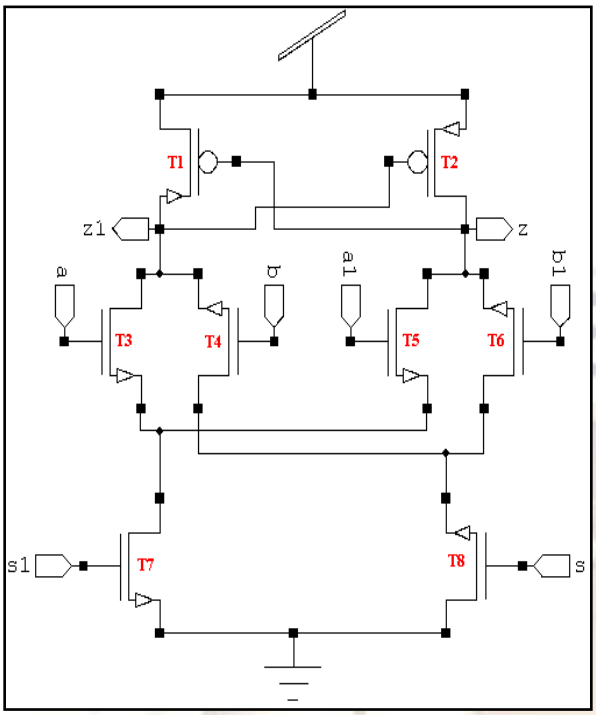

Fig 1: Schematic of existing 2:1 multiplexer

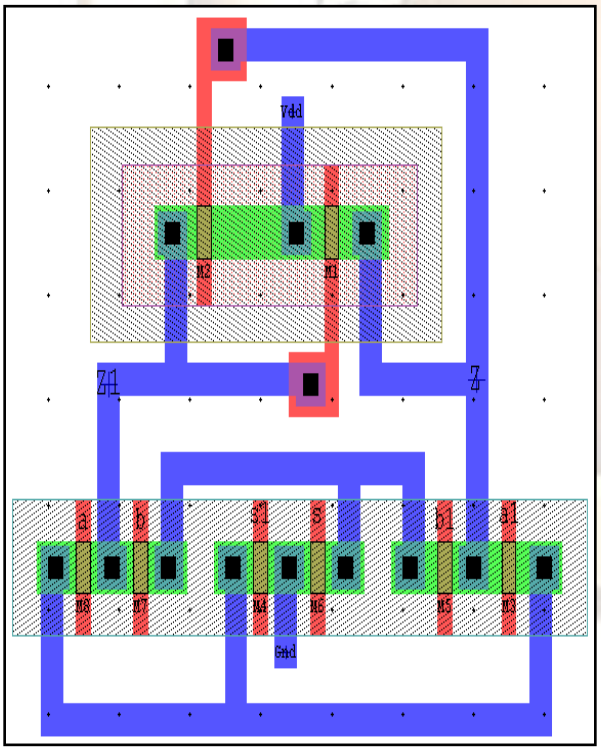

Fig 2: Layout design of existing 2:1 multiplexer

logic tree generates complementary output. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function. It can be divided it to two basic parts: a differential latching circuit and a cascoded complementary logic array [6]-[10].

III. PROPOSED 2:1 MULTIPLEXER DESIGN

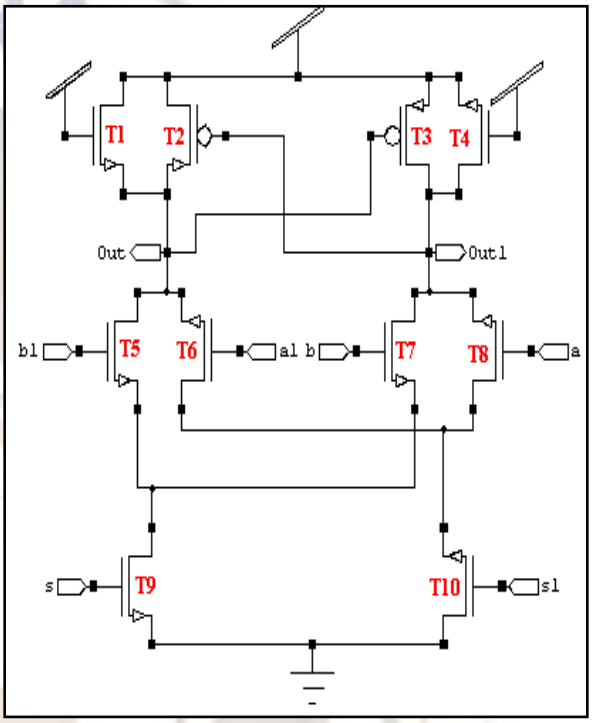

Fig 3: Schematic of proposed 2:1 multiplexer

Adding two NMOS transistors T1 and T4 in the pull up part of existing 2:1 multiplexer the circuit shows a remarkable improvement over the existing design. In the proposed circuit due to the excess added transistors there is a reduction in threshold loss for the circuit, which further causes the reduction in overall power consumption of the circuit. Due to the transmission gate topology in the proposed design the circuit shows better output waveforms in terms of threshold loss. The two logic trees are capable of processing complex functions within a single circuit delay. The schematic of proposed design and layout design of 2:1 multiplexer is shown in Fig3 and Fig4.

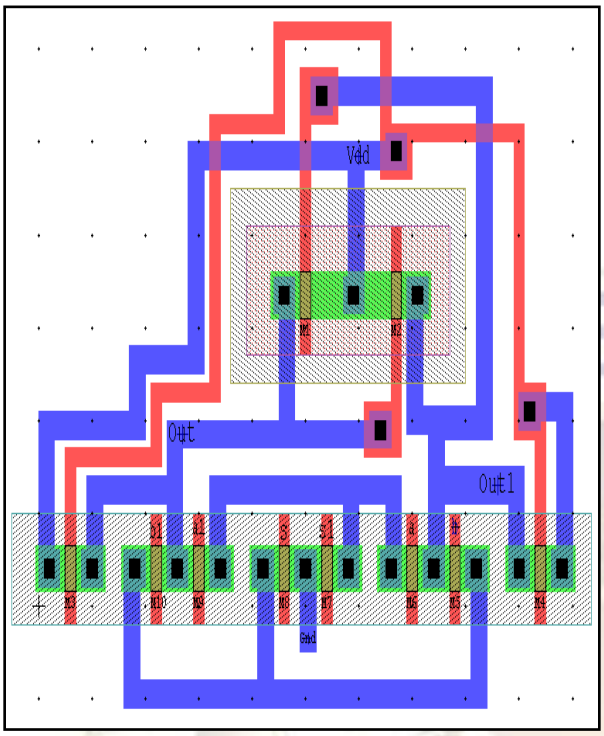

Fig 4: Layout design of proposed 2:1 multiplexer

IV. SIMULATION AND COMPARISON

All post layout simulations are performed on Tanner EDA tool version 13.0 using 45nm technology with input voltage ranges from 0.6 to 1.4 V in steps of 0.2 V. In order to prove that proposed design is consuming low power and have better performance, simulations are carried out for power consumption and delay and hence PDP at varying input voltages, frequency and temperature. For observing the noise immunity of the circuit the simulations are given for output noise voltage over a range of frequency. To establish an impartial testing environment both circuit have been tested on the same input patterns which covers all combinations of the input stream.

After the physical layout designing post-layout simulations are carried out with extraction of parasitic capacitances. Power consumption is a function of load capacitance therefore any reduction in capacitance will lead to reduced power consumption [1, 2]. Table II shows significant improvement in total as well as output parasitic capacitances. The proposed design of 2:1 has less parasitic capacitance than existing design and hence, as power consumption is directly proportional to capacitance, therefore proposed design will also have remarkable reduction in power consumption. Also, both the 2:1 multiplexer has been implemented with same logic of cascoding nMOS transistors therefore both have equal number of power consuming transitions at all the nodes. The results for the same are shown in Fig. 5- Fig. 7. Fig. 5 depicts the superiority of proposed 2:1 multiplexer in terms of power consumption with varying input voltage and supply voltage.

TABLE II. Parasitic Capacitance of existing and proposed 2:1 Multiplexer

2:1 Multiplexer Circuit	Parasitic Capacitance (F)	
	Total	Output
Existing	3.44E-14	6.06E-15
Proposed	2.91E-14	5.80E-15

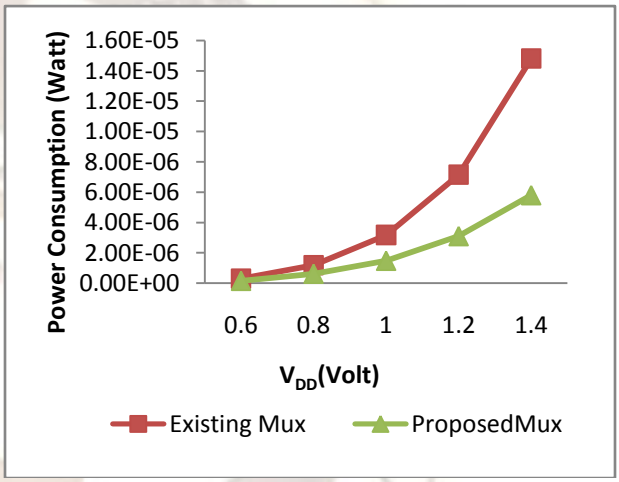

Fig 5: Power consumption vs input voltage

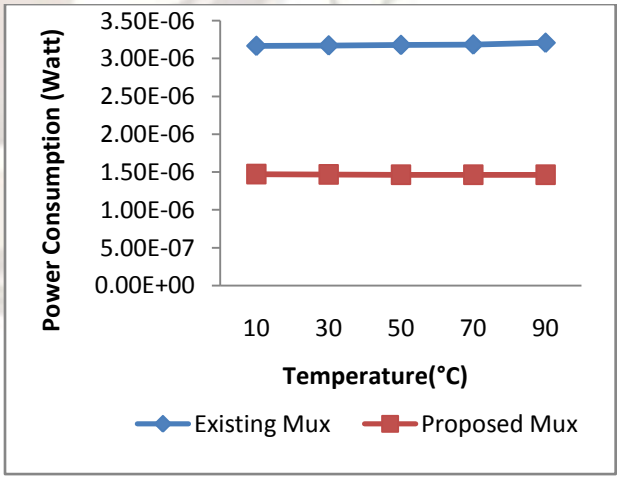

Fig 6: Power consumption vs varying temperature at 1V input voltage

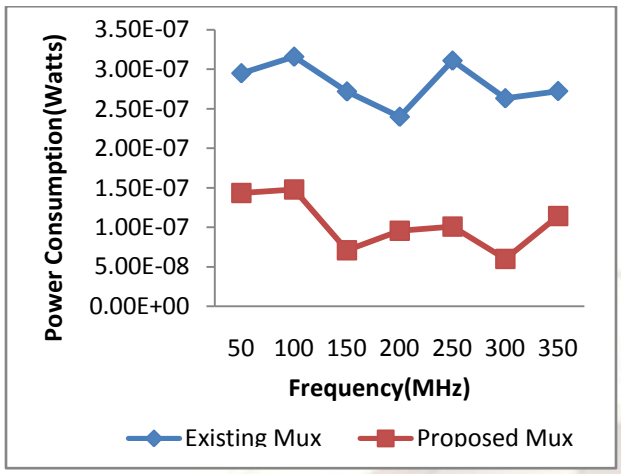

Fig 7: Power consumption vs varying frequency at 0.6V input voltage

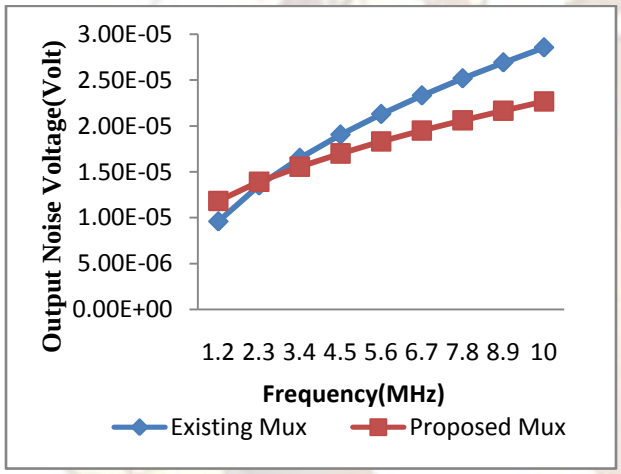

Fig 8: Output noise voltage with operating frequency

Table III. Power Delay Product comparison of existing and proposed 2:1 multiplexer

V_{DD} (volts)	Power Delay Product(Watt-sec) (45nm)	
	Existing Mux	Proposed Mux
.6	6.01585E-15	2.92549E-15
.8	2.38968E-14	1.25053E-14
1	6.37606E-14	2.98792E-14
1.2	1.43934E-13	6.33948E-14
1.4	2.97643E-13	1.18432E-13

Similar results for power consumption vs. temperature and power consumption vs. frequency are shown in Fig 6 and Fig 7 respectively. Also, the noise immunity of proposed cell is remarkably better than existing one as shown in Fig.8. Table III show the power delay product over a range of power supply voltages and as it is shown in the table that proposed 2:1 multiplexer circuit show minimum power delay product.

V. CONCLUSION

We presented a new 2:1 multiplexer design which consume less power than the existing 2:1 multiplexer. The post layout simulation have been done for the proposed circuit in order to show the improvement in power consumption over supply voltages, operating frequency and temperature. The proposed 2:1 multiplexer has been designed using 45nm technology and proved it to be a better option for low power complex system design. The net effect is that proposed 2:1 multiplexer shows a much better performance compared to existing 2:1 multiplexer.

REFERENCES

[1] A. Bellaouar, Mohamed I. Elmasry, *"Low-power digital VLSI design: circuits and systems*", 2nd Edition.

[2] Kang, Sung-Mo, Leblebici and Yusuf (1999), "*CMOS Digital Integrated Circuits Analysis and Design"*, McGraw-Hill International Editions, Boston, 2nd Edition.

[3] D. Z. Turker,, S. P.Khatri , "A DCVSL Delay Cell for Fast Low Power Frequency Synthesis Applications", *IEEE transactions on circuits and systems* june 2011, vol. 58, no. 6, pp. 1125-1138.

[4] F-s Lai and W Hwang, "Design and Implementation of Differential Cascode Voltage Switch with Pass-Gate (DCVSPG) Logic for High-Performance Digital Systems" *IEEE journal of solid-state circuits*, vol. 32, no. 4, april 1997,pp 563-573.

[5] P. K. Lala and A. Walker, "*A Fine Grain Configurable Logic Block for Self-checking FPGAs",*VLSI Design 2001, Vol. 12, No. 4, pp. 527-536.

[6] Jan M. Rabaey, *Digital Integrated Circuits; a design prospective*, Upper Saddle River: Prentice-Hall, 1996.

[7] Heller, L. G. et al., "Cascode Voltage Switch Logic: A differential CMOS Logic Family", proceedings of 1984 *IEEE International Solid-state Circuits Conference*, pp. 16-17.

[8] Ila Gupta, Neha Arora, Prof.B.P.Singh, "Simulation and Analysis of 2:1 Multiplexer Circuits at 90nm Technology" in *International*

Journal of Modern Engineering Research, Vol.1, Issue.2, pp-642-647, ISSN: 2249-6645**,** 2011.

[9] Ila Gupta, Neha Arora, Prof.B.P.Singh, "Analysis of Several 2:1 Multiplexer Circuits at 90nm and 45nm Technologies" *International Journal of Scientific and Research Publications*, Vol.2, Issue.2, February 2012, ISSN: 2250-3153.

[10] Ila Gupta, Neha Arora, Prof.B.P.Singh, "Design and Analysis of 2:1 Multiplexer for High Performance Digital Systems" *International Journal on Electronics & Communication Technology (IJECT)* Vol.3, Issue1, Jan- March 2012, pp-183-186, ISSN : 2230-7109 (Online)|ISSN : 2230-9543 (Print).

Ila Gupta was born in 1986. She did B.Sc. and M.Sc. (Physics) from Dr RML Avadh University, Faizabad, (U.P), INDIA in 2005 and 2008. She is pursuing her M.Tech in VLSI design from Faculty of Engineering & Technology, Mody Institute of Technology and Science, Lakshmangarh, Rajasthan, INDIA. She has a number of publications in some journal of well repute. Her research interest is low power VLSI device design.

Neha Arora was born in 1986. She received the B.E. degree in Electronics and Communication engineering from the reputed college of Rajasthan University, India, in 2007, and completed the academics of M.Tech in VLSI Design from Faculty of Engineering & Technology, Mody Institute of Technology and Science in 2010. She started to work as a lecturer in 2007. After gaining the experience of two years, she was promoted to Assistant Professor in 2009 with the Department of Electronics and Communication Engineering, at Mody Institute of Technology and Science Lakshmangarh, Rajasthan, INDIA (Deemed University).Her current research interests include low-voltage, low power and high-performance integrated circuit design and simulation of very large scale integrated circuits. She has more than 32 publications in international journals and conferences in the areas of high performance integrated circuits and emerging semiconductor technologies.

Dr. B. P. Singh was born in a village ORRO, NAWADAH, BIHAR (INDIA) in 1947. He did B.Sc. (Engg.) and M.Sc. (Engg.) from Bihar Institute of Technology, Sindri, Dhanbad and B.I.T. Mesra Ranchi in 1980. He served B.I.T. Mesra, Ranchi from 1970 to 1981, Indinan School of Mines Dhanbad from1981 to 1987 and Madan Mohan Malaviya Engg. College from 1987 to 2009. From 2009 till date he is the HOD of ECE and EEE, Mody Instiute of Technology Lakshmangarh, Sikar, Rajasthan (INDIA). He has over 50 papers to his credits in International and national Journals and over 50 presentations in International and National Seminars /Symposia/ Conferences. His area of research is device modeling, low-power and high performance integrated circuit design and emerging CMOS technologies semiconductor Technologies.