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Harmonic Signal Generator Based On Direct Digital Synthesizer And SOPC

Lavanya Thunuguntla*, Bindu Madhavi K ** , Neeharika R ***

* (Associate Professor, Department of ECE, HITAM, Hyderabad, India
** (Associate Professor, Department of ECE, HITAM, Hyderabad, India)
*** (Assistant Professor, Department of ECE, HITAM, Hyderabad, India)

Abstract

In modern industrial detection and communication, a signal generator has gained increasing applications.Currently available signal generators are mainly based on the DDS technology.It is a kind of frequency synthesis technology which directly synthesizes waveform on the basis of phase. As the appearance of Field Programmable Gate Array (FPGA) chips, FPGA are used to realize DDS logic to meet different demand of the user. A harmonic signal generator with adjustable frequency, phase and harmonic proportion is designed in this paper. The design of this harmonic signal generator is based on direct digital frequency synthesis (DDS) technology and the idea of System on a Programmable Chip (SOPC). The classic structure of DDS is introduced and a kind of compression ROM is designed. Then, the DDS core with compression ROM is compiled using Quartus II by VHDL language. As a kind of processor which is supplied by Atera Inc., the soft core, Nois II is embedded on FPGA chip. Using Nois II and other modules, a system is designed on one single FPGA chip. The performances such as integration, expansibility are very much improved. The principle of DDS is discussed particularly; the optimized structure of DDS core and the design SOPC on single FPGA are presented in this paper.

Key Words: FPGA, frequency Synthesizer, wave generators

I Introduction

Verilog and computer vision methods become increasingly important not only in the industrial applications but also in our daily life. Video processing generally exploits tasks with very high computational demands. Such tasks can be handled by the standard processors and computers or by computers connected to the computational networks. However, such approach is not always suitable that's why specialized hardware solutions based on digital signal processors (DSP) or a field programmable gate arrays (FPGA) are usually used in embedded systems.

From the given constant clock frequency, the frequency of the output sine wave can be controlled with the control of parameter step M. Besides, the initial phase could also be changed with the change of the output position of the sampled sine wave serial.

The frequency accuracy relative to the clock frequency is limited only by the precision of the arithmetic used to compute the phase. NCOs are phase and frequency agile, and can be trivially modified to produce phase-modulated or frequency modulated by summation at the appropriate node, or provide quadrature outputs.Whilst in theory a DAC gives a series of impulses, in practice, the output of a DAC is more typically a series of stair-steps – thus the step response of the filter (the integral of the impulse response) is of more interest. The low pass reconstruction filter smooths the stair step (removes the harmonics above the Nyquist limit) to reconstruct the analogue signal corresponding to the digital time sequence.The DCM is built for maximum flexibility, but there are certain requirements on clock frequency and clock stability, both frequency variation and clock jitter.The designs will be implemented using Verilog Hardware Description Language (HDL) at the Register Transfer Level (RTL) abstraction level.

Direct Digital Synthesizer (DDS) is a type of frequency synthesizer [1] used for creating arbitrary waveforms from a single, fixed-frequency reference clock. Applications of DDS include: signal generation, local oscillators in communication systems, function generators, mixers, modulators, sound synthesizers and as part of a digital phase-locked loop. Basically Direct Digital Synthesizer consists of a frequency reference (often a crystal or SAW oscillator), a numerically-controlled oscillator [2,3] and a digital-to-analog converter (DAC).

The reference provides a stable time base for the system and determines the frequency accuracy of the DDS. It provides the clock to the NCO which produces at its output a discrete-time, quantized version of the desired output waveform (often a sinusoid) whose period is controlled by the digital word contained in the Frequency Control Register. The sampled, digital waveform is converted to an analog waveform by the DAC. The output reconstruction filter rejects the spectral replicas produced by the zero-order hold inherent in the analog conversion process.

II Direct Digital Synthesizer (DDS)& SOPC (System On Programmable Chip)

A frequency synthesizer is the means by which many discrete frequencies are generated from one or more fixed reference frequencies. The reference frequencies are stable and spectrally pure frequency typically generated from a piezoelectric crystal. Modern frequency synthesizers must provide many discrete output frequencies so that it is impractical to generate the frequencies by having a reference frequency for each desired output frequency. The control input determines the value of the frequency synthesizer output frequency, f_o.

2.1 DDS Memory Utilization

Function generators utilize DDS to generate periodic signals at precise frequencies by choosing samples from memory rather than generating all samples of a waveform. By contrast, arbitrary waveform generators (AWGs) generate each sample of a waveform that is stored into memory. While AWGs allow a user to precisely define the waveform that is being generated, they are limited in the frequency precision they can achieve, particularly at high frequencies. By contrast, we illustrate how a function generator is able to generate a 21 MHz sinusoid, even though its frequency is not a direct multiple of the sample rate. This is illustrated in the graph below:

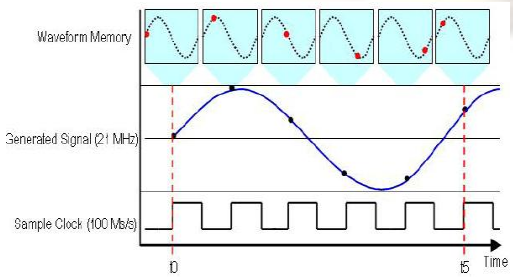

Fig 2.1: Sine wave Generation using DDS

From the graph above, we notice that the frequency of the sinusoid is not a divisor of the sampling rate. As a result, generating a 21 MHz sinusoid would be difficult with an AWG sampling at 100 MS/s. Function generators, on the other hand, use DDS to store a 16,384 sample waveform in memory. With each clock cycle, the appropriate sample is chosen from a lookup table and then generated. As a result, we are able to generate signals at precise frequencies while supplying the digital-to-analog converter (DAC) with a constant 100 MHz clock.

2.2 Principle of DDS

The principle of DDS is easy to understand. Firstly, a single frequency sine signal should be sampled for one period with the satisfaction of Shannon Sampling Theorem. It is assumed that we sample 2*N* points in one period of sine signal, and then put the points into a ROM which has 2N addresses. We convert the order of the above course. The data stored in the ROM are outputted firstly. If the sampling frequency is the output frequency of the sampled data in the ROM the output data could form sine wave and the frequency of the output sine signal is

$$f_0 = \frac{M}{2^N} f_c \quad \text{---------- (1)}$$

Where

f_0 - the frequency of output sine wave

f_c - the sampled frequency (the base clock)

M − the step of the address of output data

N −the number of ROM's address lines

From the given constant clock frequency, the frequency of the output sine wave can be controlled with the control of parameter step M. Besides, the initial phase could also be changed with the change of the output position of the sampled sine wave serial. The position of the sampled data serial [6] is transformed the address of the ROM. When the address of the ROM is over 111…11 (N bits), it means the phase of the output sine wave is over one period. The address will start from begin again. So with the address of the ROM accumulated with the step M, the continuous sampled data of sine wave is outputted. And the frequency of the output sine signal is related with the step M. Through the digital to analog converter (DAC) and the low pass filter, a sine wave whose frequency and phase can be controlled is outputted.

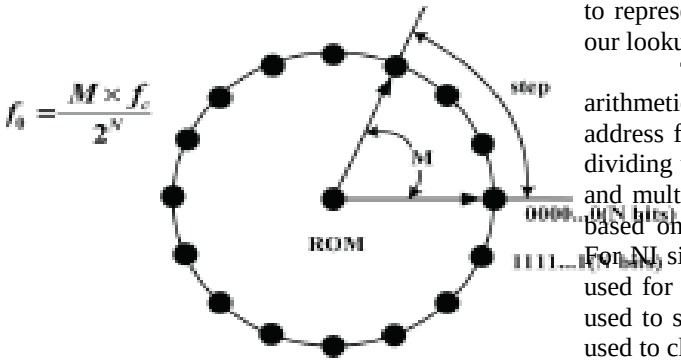

Fig 2.2: Principle of the DDS

2.3 Block Diagram DDS

The classic constructer of the DDS is composed of Numerically Controlled Oscillator (NCO) [4], Digital to Analog Converter and Filter.The actual implementation of DDS requires a look-up table to determine the phase output signal at any point in time. The following figure shows the building blocks for direct digital synthesis-based waveform generation.

As the figure above illustrates, a phase accumulator compares the sample clock and desired frequency to increment a phase register. Again, the fundamental idea is that we can generate signals with precise frequencies by generating an appropriate sample based on the phase of that frequency at any point in time.

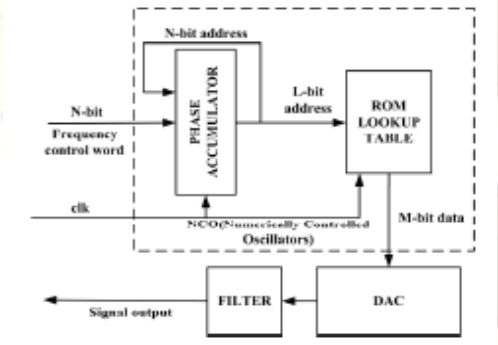

Fig 2.3 Block diagram of classic DDS.

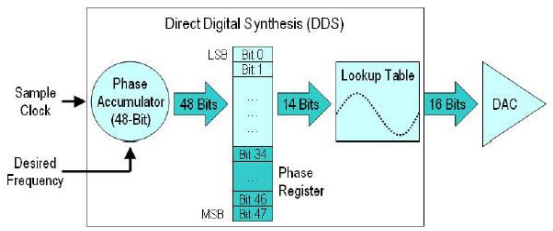

Fig 2.4 Implemented block diagram of DDS

In addition, by representing our waveform with 214 (16,384) points, we are able to represent exactly 16,384 phase increments with our lookup table.

The phase accumulator uses simple arithmetic operations to calculate the lookup table address for each generated sample. It does this by dividing the desired frequency by the sample clock and multiplying the result by 248. This number is based on the bit resolution of the phase register. For NI signal generators, a 48-bit phase register is used for maximum precision. Of these, 34 bits are used to store the remainder phase, and 14 bits are used to choose a sample from the lookup table.

The NCO contains the phase accumulator and ROM lookup table. It is the core of DDS. In each clock period, the output of phase accumulator is accumulated with frequency control word M (N-bit) and high L-bit results of the output are used as address input to the ROM lookup table. In the ROM lookup table, these addresses are converted to the M-bit sampled data of expected signal. Suppose that the clock frequency is constant, we can absolutely get the formula (1). According to the Shannon Sampling Theorem, upper limit the output frequency is c 0.5 f . However, the biggest output frequency in practice is about c 0.25 f , and the resolution of output frequency is $\frac{1}{2^N} f_c$.

2.4 Design of DDS Core

The DDS core has two important parts, the frequency and phase control module and the ROM lookup table. The frequency and phase control module is composed of an

Accumulator and an added. The frequency of the signal is controlled by accumulator and the initial phase of the signal is controlled by the adder [5]. The initial value of the accumulator is 0. In every clock period, the frequency control word is added at the previous result of the sum in accumulator, and then the result of the accumulator is added with the phase control word in the adder. Finally, the result input to the ROM lookup table.

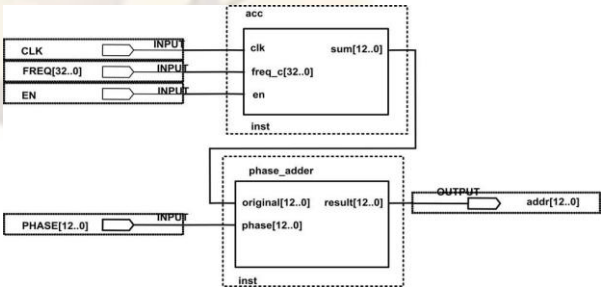

Fig 2.5 Frequency and initial phase control module

The initial phase and frequency of the signal can be changed by this module flexibly. The same time, the control precision can be increased by increasing the bit number of the frequency control word and initial phase control word.The module which is created in Quartus II. DDS provides remarkable frequency resolution and allows direct implementation of frequency, phase and amplitude modulation. These features which were 'tacked-on' to function generators now are handled in a clean, fundamental way by DDS.

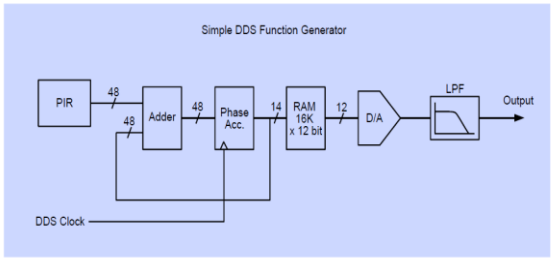

Fig 2.6 DDS function generation

SOPC, When a system has been configured then generated, the SOPC builder generates an RTL description of the CPU and peripherals and a Software Development Kit (SDK) configured for this core. The SDK includes header files defining the memory map and all peripherals, a library of example drivers for the peripherals included and a series of example source files and a make files which may be used for debugging.

III Project design and implementation flow

3.1 Digital Design Flow

The lowest level of digital hardware modeling is the gate level and transistor level modeling. These two level modeling provides the most accurate of hardware modeling including the timing information and is able to model as close to real silicon as possible. However, the simulation speed for design in gate and transistor level is extremely slow. On top of that, normally design in gate or transistor level is performed by the help of CAD synthesis tools by synthesizing the RTL level design to gate level and from gate level to transistor level.

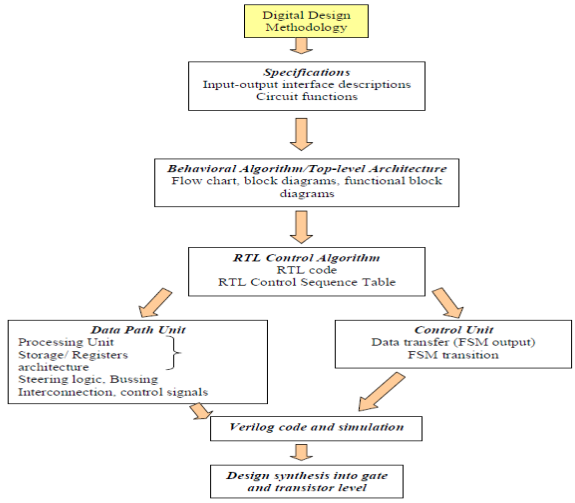

Figure 3.1 Digital design flow

With the advancement in CAD tools, it is rarely that digital hardware design is modeled at gate level or transistor level by the designer. In most if not all, the design is modeled at RTL level and synthesize to gate and transistor level by the CAD tools. During the design process, the design is partitioned into a smaller function block. Each functional block is design and verify separately. The design is modeled using Verilog HDL at RTL level. Simulation and validation is then performed using the Xilinx ISE 12.1 tools.

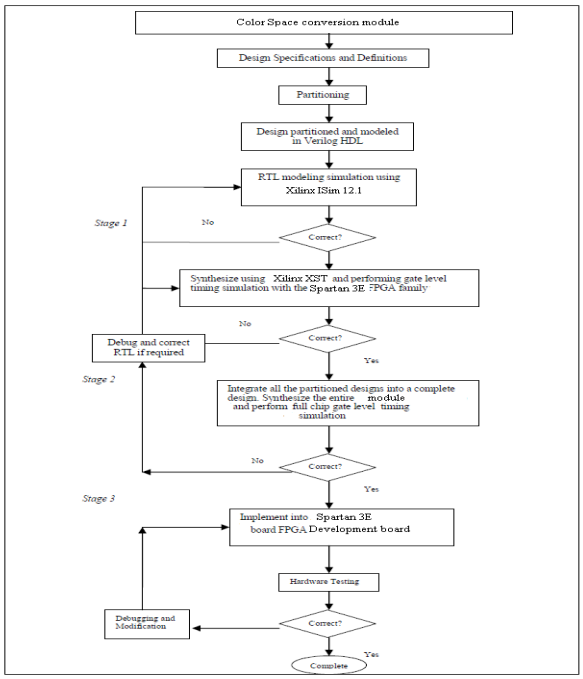

Figure 3.2: Project design and implementation flow

After the partitioned design has been verified, all the functional blocks are integrated together to become the complete design. Full chip RTL simulation and validation is then performed. Once the validation at RTL level is complete, the entire IOP is being synthesized and gate level timing simulation is performed using Xilinx XST synthesis tool.Finally, the design is implemented in the hardware by programming the design into the Spartan 3E FPGA development board.

3.2 Hardware Design Using System Generator

System Generator is a system-level modeling tool that facilitates FPGA hardware design. It extends Simulink in many ways to provide a modeling environment that is well suited to hardware design. The tool provides high-level abstractions that are automatically compiled into an FPGA at the push of a button. The tool also provides access to underlying FPGA resources through low-level abstractions, allowing the construction of highly efficient FPGA designs.

IV. Global Clock Resources

This describes how to take advantage of the Spartan®-3 generation global clock resources, including the dedicated clock inputs, buffers, and routing. The clocking infrastructure provides a series of low-capacitance, low-skew interconnect lines well suited to carrying high-frequency signals throughout the FPGA, minimizing clock skew and improving performance, and should be used for all clock signals. Third-party synthesis tools, and Xilinx synthesis and implementation tools, automatically use these resources for high-fanout clock signals.

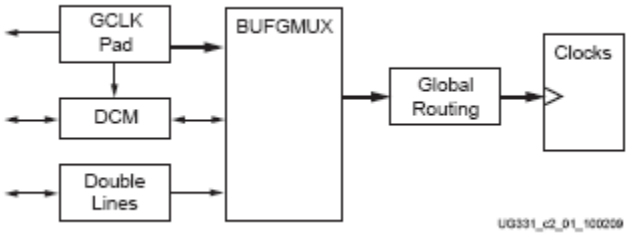

Fig 4.1 Overview of clock connection

The BUFGMUX drives the global clock routing, which in turn connects to clock inputs on device resources. The BUFGMUX can also connect to a DCM, typically used for internal feedback to the DCM CLKFB input.

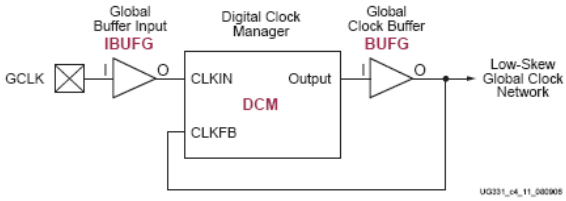

Fig4.2 Using a DCM to estimate clock skew

5.1 Spartan-3 Global Clock Buffers

The Spartan-3 family has only eight global clock buffers. Four BUFGMUX elements are placed at the center of the die's bottom edge, just above the GCLK0 - GCLK3 inputs. The remaining four BUFGMUX elements are placed at the center of the die's top edge, just below the GCLK4 - GCLK7 inputs. Each pair of BUFGMUX elements shares two sources; each source feeds the I0 input of one BUFGMUX and the I1 input of the adjacent BUFGMUX. Thus two completely independent pairs of clock inputs to be multiplexed could be on the same side of the die but not on the adjacent BUFGMUX elements.

v cONCLUSION & fUTURE sCOPE

The output frequency of a DDS is determined by the value stored in the frequency control register (FCR) which in turn controls the NCO's [5] phase accumulator step size. Because the NCO operates in the discrete-time domain, it changes frequency instantaneously at the clock edge coincident with a change in the value stored in the FCR.

The DDS output frequency settling time is determined mainly by the phase response of the reconstruction filter. An ideal reconstruction filter with a linear phase response (meaning the output is simply a delayed version of the input signal) would allow instantaneous frequency response at its output because a linear system can not create frequencies not present at its input.

The clocking infrastructure provides a series of low-capacitance, low-skew interconnect lines well suited to carrying high-frequency signals throughout the FPGA, minimizing clock skew and improving performance, and should be used for all clock signals. Third-party synthesis tools, and Xilinx synthesis and implementation tools, automatically use these resources for high-fanout clock signals. This is focuses on the global clock resources found in all Spartan-3 generation platforms, and the quadrant clock resources found in the Spartan-3E and Extended Spartan-3A families.

The clock routing can be used in conjunction with the DCMs, which are discussed in more detail in "Using Digital Clock Managers (DCMs)." For information on the special clock inputs used for configuration (CCLK) and Boundary-Scan.Global clock inputs, buffers, and routing are automatically used for a design's highest fanout clock signals. Implementation reports should be checked to verify the usage of clock buffers where desired. The user can specify the details of global clock usage in order to take advantage of special features such as multiplexing and clock enables, or to maximize the number of clocks using global resources in a design.

Digital Clock Managers (DCMs) provide advanced clocking capabilities to Spartan®-3 generation FPGA applications (Spartan-3, Spartan-3E, and Extended Spartan-3A families).

Primarily, DCMs eliminate clock skew, thereby improving system performance. Similarly, a DCM optionally phase shifts the clock output to delay the incoming clock by a fraction of the clock period. DCMs optionally multiply or divide the incoming clock frequency to synthesize a new clock frequency. The DCMs integrate directly with the FPGA's global low-skew clock distribution network.

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Authors

Ms Lavanya Thunuguntla has 6 years of Teaching experience and presently working as an Associate Professor in the Department of ECE in Hyderabad Institute of Technology and Management (HITAM), Hyderabad, AP(India).She received her B.Sc degree in Computer Science from Acharya

Nagarjuna University in 2002, M.Sc degree in Physics from University of Hyderabad, Hyderabad in 2004 and M.Tech from Indian Institute of Technology (IIT) Kharagpur in 2007. She has Professional Membership in IEEE. She has various journal publications in International journals in the field of Nano Technology etc. She has guided several M.Tech and B.Tech projects. She has strong motivation towards research in the fields of Nano Technology, Microwave and Optical & Analog Communications ,VLSI system design etc.

Mrs Bindu Madhavi K has 7 years of Teaching experience and presently working as an Assistant Professor in the Department of ECE in Hyderabad Institute of Technology and Management (HITAM) Hyderabad, AP(India). She received her B.Tech degree in ECE from MITS, JNTU in 2003, M.Tech in VLSI System Design from JNTU ,Hyderabad. She has guided several M.Tech and B.Tech projects. Her areas of interests are VLSI System Design and Communication Systems, Signal Processing.

Ms R Neeharika has 3 years of Teaching experience and presently working as an Assistant Professor in the Department of ECE in Hyderabad Institute of Technology and Management (HITAM), Hyderabad, AP(India).She received her B.Tech degree from JNTU.