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To Reduce SRAM Sub-Threshold Leakage Using Stack and Zig-Zag techniques

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Abstract-- The growing market of portable electronics devices demands lesser power dissipation for longer battery life and compact system. Considerable attention has been given to the design of low-power and high-performance SRAMs since they are critical components in both high-performance processors and hand-held portable devices. The reduction of the threshold voltage due to voltage scaling leads to increase in sub threshold leakage current and hence static power dissipation. The leakage current consists of reverse-bias diode currents and sub threshold currents. Scaling down of threshold voltage results in exponential increase of the sub threshold leakage current. This paper presents a method based on controlling the leakage currents by using effective stacking of transistors using stack technique and another method based on zig-zag approach.

The proposed stack technique forces a stack effect by breaking down an existing transistor into two half size transistors. When the two transistors are turned off together, induces reverse bias between the two transistors results in sub-threshold leakage current reduction. The Zig-Zag technique reduces wake-up overhead caused by sleep transistors by placement of alternating sleep transistors, assuming a particular pre-selected input vector. The simulation results have been carried out using microwind tool on 90 nm technology.

Key terms : SRAM, Stack Technique, Zig-Zag Technique. Low Power.

1. INTRODUCTION

Aggressive scaling of CMOS devices in the last four decades has enabled the semiconductor industry to meet its ever-increasing demand for higher performance and higher integration densities. However, this trend is encountering several major challenges in the nanometer era, due to the high integration levels as well as the physical limitations of semiconductor devices. High power consumption is one of the major challenges of integrated circuit design in nano-scale technologies [1]. For high-performance applications, large power dissipations within a small die area are resulting in alarming temperatures, posing serious reliability concerns. For battery operated devices, on the other hand, increased power consumption is drastically limiting the battery lifetime.

High power consumption leads to reduction in the battery life in the case of battery-powered applications and affects reliability, packaging, and cooling costs. The main sources for power dissipation are: 1) capacitive power dissipation due to the charging and discharging of the load capacitance; 2) short-circuit currents due to the existence of a conducting path between the voltage supply and ground for the brief period during which a logic gate makes a transition; and 3) leakage current. The leakage current consists of reverse-bias diode currents and sub-threshold currents. Scaling down of threshold voltage results in exponential increase of the sub-threshold leakage current.

2. CONVENTIONAL 6T-SRAM CELL

Random access means that locations in the memory can be written to or read from in any order, regardless of the memory location that was last accessed. The schematic diagram of 6T SRAM cell is shown in fig 1. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. Access to the cell is enabled by the word line (WL in figure 1) which controls the two access transistors, in turn, control whether the cell should be connected to the bit lines: BL and BL’. They are used to transfer data for both read and write operations. While it's not strictly necessary to have two bit lines, both the signal and its inverse are typically provided since it improves noise margins.

3. RELATED WORK

Random access means that locations in the memory can be written to or read from in any order, regardless of the memory location that was last accessed. The schematic diagram of 6T SRAM cell is shown in fig 1. Each bit in an SRAM is stored on four transistors that form two cross-coupled inverters. This storage cell has two stable states which are used to denote 0 and 1. Two additional access transistors serve to control the access to a storage cell during read and write operations. Access to the cell is enabled by the word line (WL in figure 1) which controls the two access transistors, in turn, control whether the cell should be connected to the bit lines: BL and BL'. They are used to transfer data for both read and write operations. While it's not strictly necessary to have two bit lines, both the signal and its inverse are typically provided since it improves noise margins.

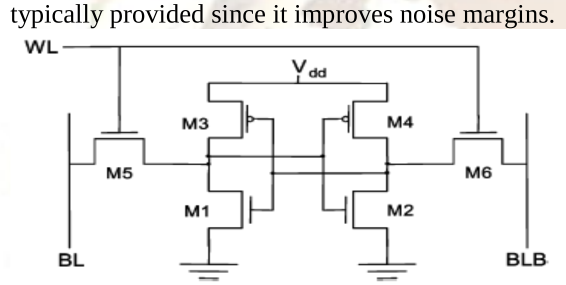


Fig 1. Conventional 6T SRAM cell

The leakage current of deep submicron CMOS transistor consists of two major components: sub threshold current, and gate tunneling current. Sub threshold leakage is the drain-source current of a transistor when the gate-source voltage is less than the threshold voltage. More precisely, sub threshold leakage happens when the transistor is operating in the weak inversion region. The sub threshold current depends exponentially on threshold voltage, which results in large sub threshold current in short channel devices. Sub-threshold leakages in the SRAM cell are shown in the fig 2.

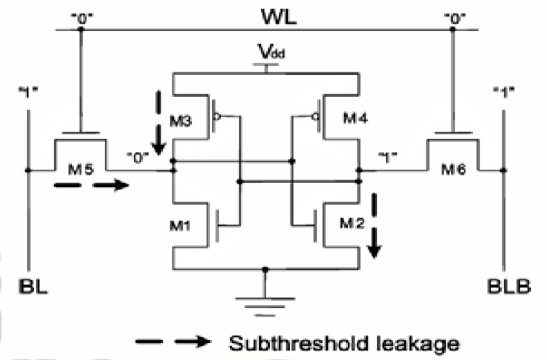


Fig 2. Sub-Threshold leakage current in SRAM cell

4. PROPOSED TECHNIQUES

The first technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [5]. Figure 3 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in sub-threshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach.

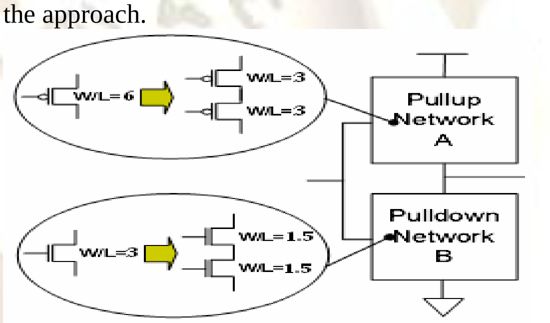


Fig 3. Stack approach

A variation of the sleep approach, the zigzag approach, reduces wake-up overhead caused by sleep transistors by placement of alternating sleep transistors assuming a particular pre-selected input vector [4]. In Figure 4, we assume that, in sleep mode, the input of the logic is '0' and each logic stage reverses its input signal, i.e., the output is '1' if the input is '0,' and the output is '0' is the input is '1.' If the output is '1,' then a sleep transistor is added to the pull down network; if the output is '0', then a sleep transistor is added to the pull-up network. Thus, the zigzag approach uses fewer sleep transistors than the original sleep approach. Furthermore, this approach still results in destruction of state (i.e., state is set to the particular pre-selected input vector), although the problem of floating output voltage is eliminated.

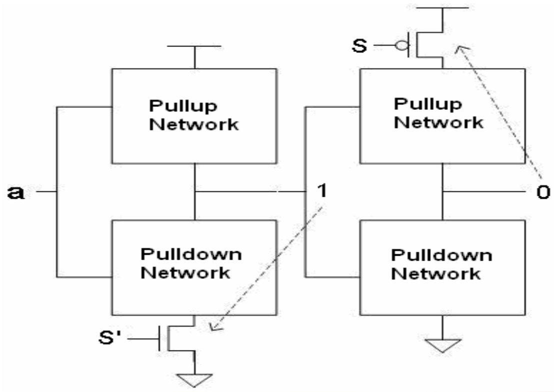


Fig 4. Zig-Zag approach

5. DESIGN IMPLEMENTATION

5.1. CONVENTIONAL 6T SRAM CELL:

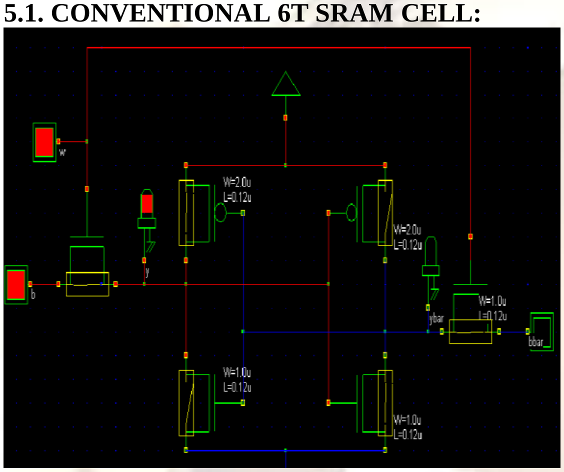


Fig 5. Schematic of Conventional 6T SRAM Cell

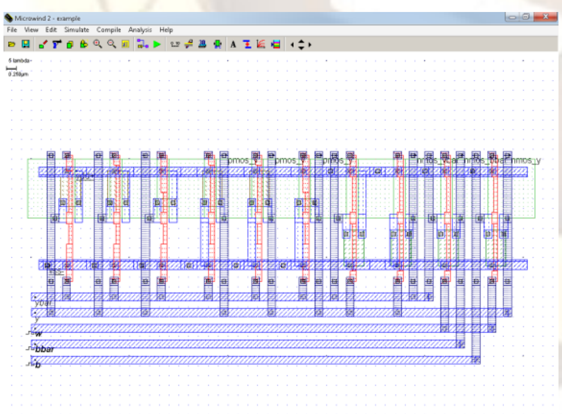


Fig 6. Layout of Conventional 6T SRAM Cell

5.2. SRAM CELL USING STACK TECHNIQUE:

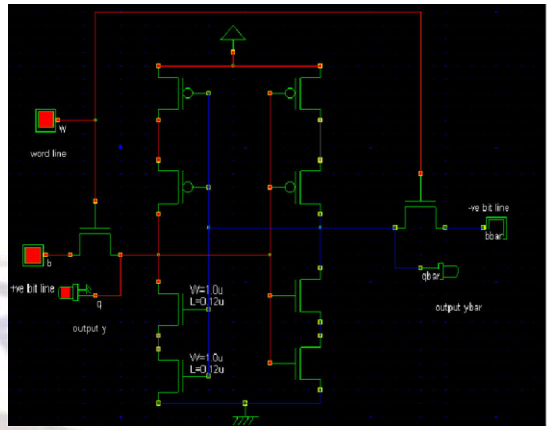


Fig 7. Schematic of SRAM Cell Using Stack

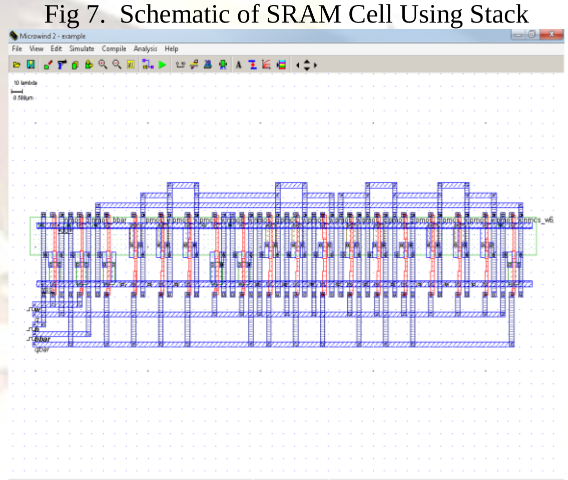


Fig 8. Layout of Stack SRAM Cell

5.3. SRAM CELL USING ZIG-ZAG TECHNIQUE:

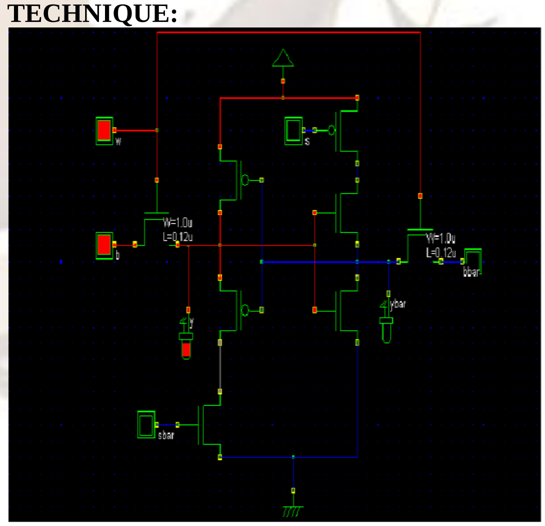


Fig 9. Schematic of Zig-Zag SRAM Cell

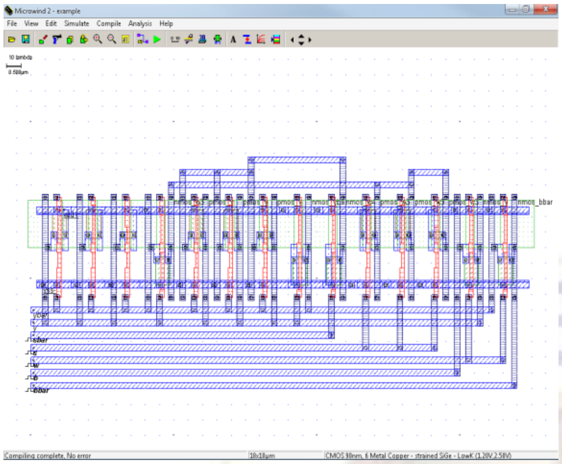
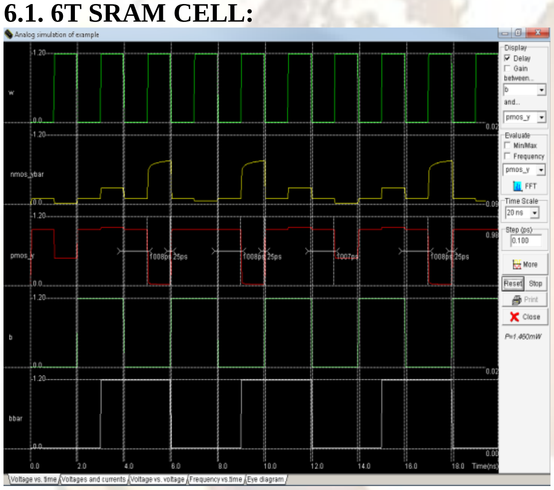


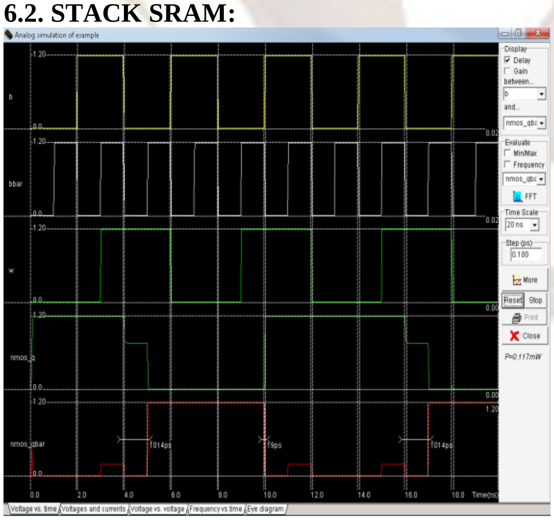
Fig 10. Layout of Zig-Zag SRAM Cell

6. SIMULATED RESULTS:

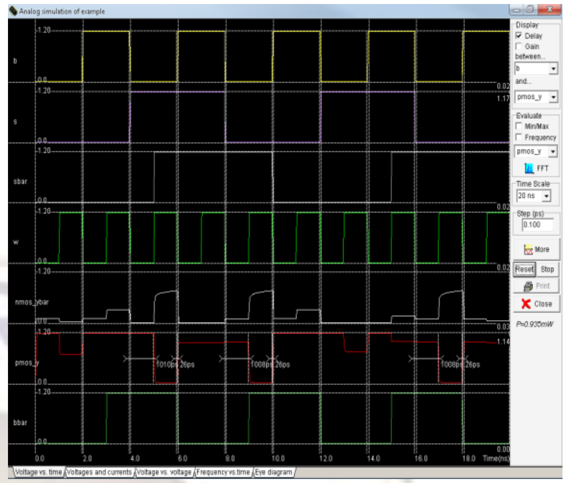
6.1. 6T SRAM CELL:



6.2. STACK SRAM:



6.3. ZIG-ZAG SRAM:



7. POWER CONSUMPTION

Conventional 6T SRAM	Zig-Zag SRAM	Stack SRAM
1.460mw	0.935mw	0.117mw

8. CONCLUSION

Scaling down of the CMOS technology feature size and threshold voltage for achieving high performance has resulted in increase of leakage power dissipation. We have presented an efficient methodology for reducing leakage power in VLSI design. SRAM cell is designed using stack and zig-zag approaches so that the power dissipation is less when compared with conventional SRAM cell.

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