Lavanya Thunuguntla, Bindu Madhavi K, Pullaiah T/ International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 2,Mar-Apr 2012, pp.183-191

Designing of Efficient Online Testable Reversible Multiplexers and DeMultiplexers with New Reversible Gate

Lavanya Thunuguntla * , Bindu Madhavi K **, Pullaiah T ***

* (Associate Professor, Department of ECE, HITAM, Hyderabad, India)
** (Assistant Professor, Department of ECE, HITAM, Hyderabad, India)
***(Professor & HOD, Department of ECE, HITAM ,Hyderabad ,India)

Abstract

Reversible logic is emerging and a promising computing paradigm having its applications in low power VLSI design, quantum computing, nano technology and optical computing. In this paper, a new 4*4 reversible gate termed 'OTG' (Online Testable Gate)and CTSG are proposed suitable for online testability in reversible logic circuits. OTG can also work singly as a reversible full adder with a bare minimum of two garbage outputs. OTG is shown better than the recently proposed R1 gate (introduced for providing online testability in reversible logic circuits), in terms of computation complexity. The proposed reversible gate is combined with the existing 4*4 Feynman gate to design online testable reversible adders such as ripple carry adder, carry skip adder and BCD adder and 4*1 Multiplexers and De Multiplexers. The efficient reversible design of two pair rail checker is also shown in this paper. The testable reversible circuits proposed in this work are shown to be better than the recently proposed testable designs in terms of number of reversible gates, garbage outputs and unit delay.

Keywords **- Garbage outputs, , Online Testable Gate, Power consumption, Reversible logic circuits**

I. Introduction

Energy loss on the other hand, is an important consideration in a binary arithmetic circuit. Part of the problem of energy dissipation is related to non-ideal of transistors and materials. Higher level of integration and the use of new fabrication processes have reduced the heat loss over the last decades. Another problem arises from Landauer's principles [1] state that, logic computations that are not reversible, necessarily generate heat KTln2 for every bits of information that is lost, where K is the Boltzmann's constant and T is the temperature. Reversible are circuits (gates) in which there is a one-to-one mapping between vectors of inputs and outputs. The reversible designs do not lose any information.. Bennett showed that kTln2 energy dissipation would not occur, if a computation is carried out in a reversible way [2]**,** since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Reversible circuits are those circuits that do not lose information. Reversible computation in a system can be performed only when the system comprises of reversible gates. These circuits can generate unique output vector from each input vector, and vice versa, that is, there is a one-to-one mapping between input and output vectors.

The reversible logic operations do not erase (lose) information and dissipate very

less heat. Thus, reversible logic is likely to be in demand in high speed power aware circuits. Reversible circuits are of high interest in low power VLSI design, optical computing, quantum computing and nanotechnology. The most prominent application of reversible logic lies in quantum computers as they must be built from reversible logic components. In reversible logic, testing can be one of the major problems, as the levels of logic are significantly higher than the standard logic [3,4]. Moreover, the major goal in reversible logic design is to minimize the number of reversible gates used and garbage outputs produced (Garbage output refers to the output that is not used as a primary output or as an input to other gate). In this project, the focus is on the proposal of a new 4*4 reversible gate termed 'OTG' (Online Testable Gate), and its use in designing efficient online testable reversible adder circuits. The OTG can work singly as a reversible full adder .The used OTG gate is combined with 4*4 FEYNMAN gate [5,6] to provide the online testability feature. The testable 1-bit reversible full adder designed using the used reversible OTG gate, is shown to be better than the recently used testable full adder used in terms of number of reversible gates, garbage outputs and unit delay. The efficient reversible design of two pair two rail checker is also presented, better than the existing one in literature. The used OTG gate is used to design online testable reversible adders such as ripple carry adder, carry skip adder and BCD adder. The testable reversible BCD adder is presented first time in literature. Noted that the used work concentrates on design of online testable reversible circuits rather than the fault tolerant one [7,8]. The used online testable reversible adder designs are proved to be better (efficient) than the recently used testable designs, in terms of number of reversible gates, garbage outputs and unit delay. The online testable reversible circuits used and designed in this work will form the basis for a testable primitive reversible/quantum ALU. In this project, we propose a novel 4*4 reversible gate termed 'OTG' (Online Testable gate) suitable for providing online testability in reversible logic circuits. OTG can work singly as a reversible full adder with bare minimum of two garbage outputs.

Figure 1.1 shows the used OTG gate. OTG can also implement all Boolean functions. Figure 1.3 shows the implementation of OTG gate for realizing NAND function. Since, NAND is a universal gate any Boolean function can be realized with OTG gate. The used OTG gate is more efficient in computation complexity, compared to recently used 4*4 'R1' gate [9,10] (R1 gate is shown in Fig.12. and was used for introducing online testability in reversible logic circuits). Figure 2.b shows the working of OTG as a reversible full adder with bare minimum of two garbage outputs (at least two garbage outputs will be required to realize a reversible full adder).

1.1 Used New Gate

In this project, we propose a novel 4*4 reversible gate termed 'OTG' (Online Testable gate) and CTSG which are suitable for providing online testability in reversible logic circuits.

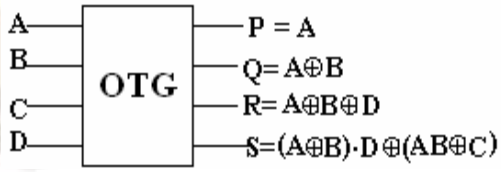


FIGURE 1.1 OTG GATE

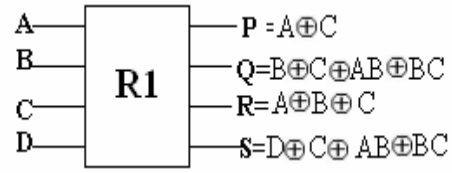
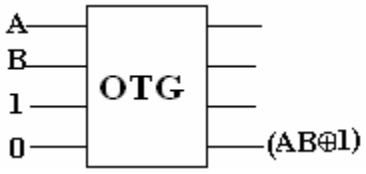


FIGURE 1.2 A R1 GATE



1.3 OTG GATE AS A NAND FUNCTION

OTG can work singly as a reversible full adder with bare minimum of two garbage outputs. A reversible gate has an equal number of inputs and outputs. Generally, with *n* inputs, there exist (2*n*)! reversible gates. The well-known 2×2 Feynman gate operates as a controlled NOT (CNOT). If the control input of CNOT is set to '0', the gate acts as a BUFFER gate; else, it acts as a NOT gate. The Feynman gate can be used as fanout gate to copy a signal. If the *B* input in Fig. 3a is set to '0' then two outputs of the Feynman gate are *A*. Toffoli and Fredkin gates are 3×3 reversible gates. Each of these gates is universal, i.e. any logical reversible circuit can be implemented using these gates.

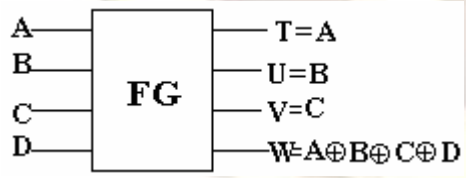


FIGURE 1.4 4*4 FEYNMAN GATE

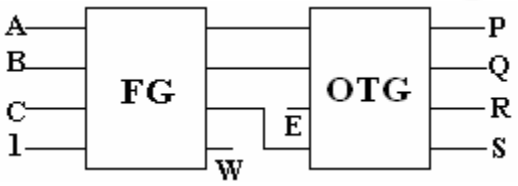


FIGURE 1.5 COMBINATION OF FEYNMAN AND OTG FOR ONLINE TESTABILITY

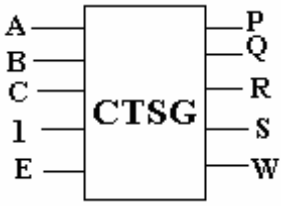


FIGURE 1.6 A COMBINATION OF FEYNMAN AND OTG TERMED 'CTSG'

Figure 1.6 shows the realization of the used CTSG block as an online testable reversible full adder with the complementary R & W outputs (input E=0 in this case).

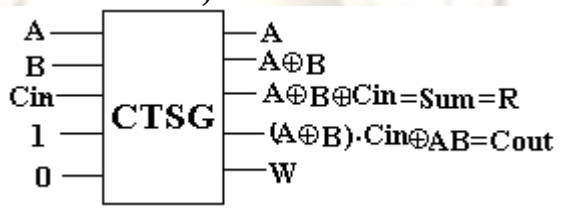


FIGURE 1.7 CTSG AS A REVERSIBLE FULL ADDER WITH ONLINE TESTABILITY

1.2 Design of Online Testable Reversible Adders

The used CTSG block (OTG and FEYNMAN gate) is used to design efficient online testable reversible arithmetic adders. The online testable reversible adders designed in this work are ripple carry adder, carry skip, and BCD adder and Multiplexer and De Multiplexers.

1.2.1 Reversible Design of Ripple Carry Adder using CTSG

The full adder is the basic building block in a ripple carry adder. The reversible online testable ripple carry adder can be designed by cascading the one bit testable reversible full adder

designed from CTSG block as shown in 1.7. Thus, we are able to achieve the improvement ratio of 8, 1.5 and 8 in terms of number of reversible gates, garbage outputs and unit delay, respectively.

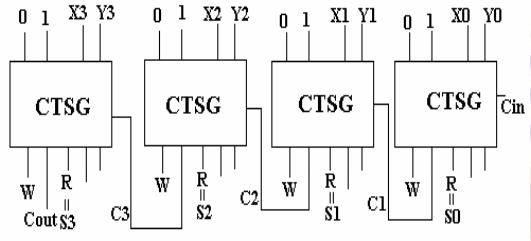


FIGURE 1.7 ONLINE TESTABLE REVERSIBLE RIPPLE CARRY ADDER

II. The VHDL Approach to Design

A number of concepts that were presented during the explanation of the design trajectory in the previous section, are clearly recognizable in VHDL. The most important of these are behavior versus structure and Hierarchy and abstraction. A behavioral description of a hardware building block, regardless of whether the block covers the overall design or only a part, strictly documents the relation between the input and output signals. It does not say anything about the division of the block into subblocks. If such a division exists, then we have a structural description. You should note that a structural description not only specifies the subblocks that make up the block, but also the exact interface between the various blocks. In other words, when there is a division into subblocks, a description is needed of the various input and output signals of each block, as well as of how the signal interaction between the different blocks is effected.

Hierarchy and abstraction,the subblocks making up a block that has a structural description, can on their turn have their own structural description. This could go on recursively until we finally come to the elementary or atomic building blocks of the design. In this lab course, for example, these blocks are the elements from the cell library. Under different circumstances the individual transistors might be the elementary building blocks. The recursive division of the building blocks results in a hierarchical description of the design. A concept that is related to hierarchy is abstraction. At a given level in the hierarchy, not all details of the underlying levels are important. By eliminating those details, abstraction enables us to refer to the calculations at a specific level in a meaningful way. It might be useful, for example, to express a calculation at a certain abstraction level in integers, while at a lower level the same calculation might be described in terms of the bits in the binary representation of those numbers.

Top-down design is a design methodology starts with a behavioral description of the overall system to be designed. The system is then subdivided into a number of subblocks. This is called decomposition.

The advantage of using VHDL or another hardware description language in a top- down design methodology is that each decomposition step can be verified immediately. This is done by simulating the description before and after decomposition using the same input signals. This approach is used as much as possible during this lab course.

It should be noted that, while simulation is a common and useful tool to verify designs, it does not provide any guarantee of correctness. That is because the number of possible combinations of input patterns for circuits is hardly manageable (except for small and trivial

circuits). An alternative for verification through simulation is formal verification. This proves mathematically that decomposition step preserves the behavior of the circuit. Formal verification is not covered further in the course as this is not applied much in practice (only a few CAD tools). Until now it was assumed that a decomposition step would be performed directly by the designer. It can also be done, however, using CAD tools.

III. Design of Online Testable Multiplexer and De Multiplexer

3.1 Design of a 4 in To 1 Multiplexer

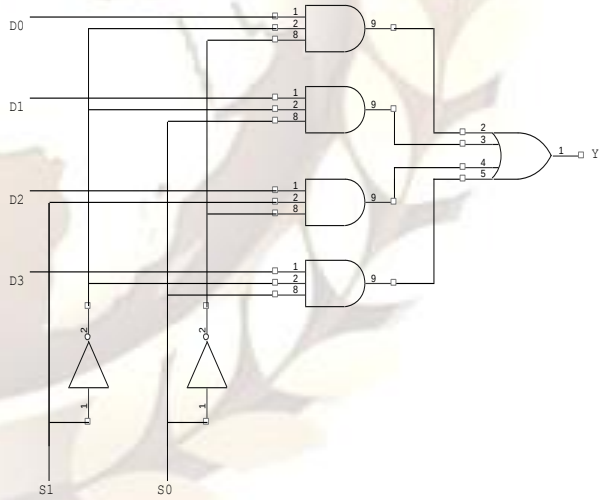
A Multiplexer is a combinational circuit that is given a certain number (usually a power of two) data inputs, let us say 2^n, and n address inputs used as a binary number to select one of the data inputs. The Multiplexer has a single output, which has the same value as the selected data input. In other words, the Multiplexer works like the input selector of a home music system. Only one input is selected at a time, and the selected input is transmitted to the single output. While on the music system, the selection of the input is made manually, the Multiplexer chooses its input based on a binary number, the address input. The truth table for a Multiplexer and the corresponding logic diagram were shown below.

INPUTS	SELECT LINES		OUTPUT
A	S0	S1	Z
	0	0	A
B	0	1	B
	1	0	C
C	1	1	D
D			

TABLE.1 TRUTH TABLE FOR A 4 IN TO 1 MULTIPLEXER

The truth table for a Multiplexer is huge for all but the smallest values of n. We therefore use an abbreviated version of the truth table in which some inputs are replaced by `-' to indicate that the input value does not matter.

A 4*1 Multiplexer has basically 4 input lines one output line and 2 select lines. Basing on the select line inputs



one of the input is passed to the output.

Fig 3.1 Rtl Schematic For 4*1 Multiplexer Design Using Ctsg Gate

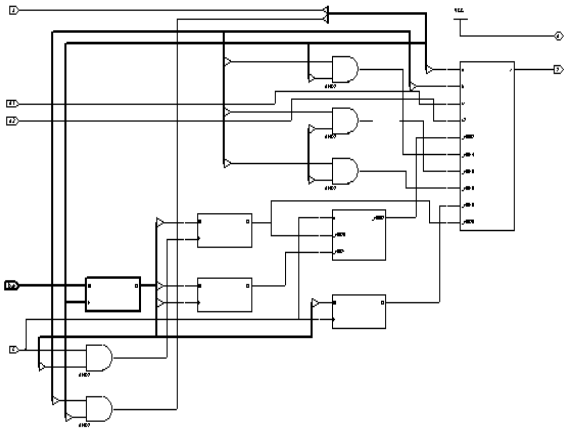


Figure 3.2 LOGIC DIAGRAM FOR A 4 IN TO 1 MULTIPLEXER

The design of a 4 in to 1 Multiplexer can be well defined also using the suggested online testable gate. Using the truth table of the CTSG gate and also the inputs and outputs of the CTSG gate, we can design a 4 * 1 mux very easily in a simple behavioral vhdl model. As we are going to use CTSG gate in the implementation of the mux , the online testable feature of the CTSG gate also imparts to the mux design. So finally a online testable Multiplexer is also designed.

INPUTS	SELECT LINES		OUTPUT
	S1	S2	Z
A	0	0	A
B	0	1	B
C	1	0	C
E	1	1	E

TABLE.3 Truth Table For 4*1 Multiplexer

3.2 Design of an Online Testable 1 To 4 Demultiplexer

The Demultiplexer is the inverse of the Multiplexer, in that it takes a single data input and n address inputs. It has 2^n outputs.

	Address		Outputs			
Data	S_1	S_0	Y_0	Y_1	Y_2	Y_3
D	0	0	D	0	0	0
D	0	1	0	D	0	0
D	1	0	0	0	D	0
D	1	1	0	0	0	D

TABLE.4 TRUTH TABLE FOR A DEMULTIPLEXER

The address input determine which data output is going to have the same value as the data input. The other data outputs will have the value 0.

A Demultiplexer (DMUX) is a device which essentially performs the opposite operation to the MUX. That is, it functions as an electronic switch (/data distributor) to route an incoming data signal to one of several outputs. Figure shows the logic symbol for the 1-line-to-4-line Demultiplexer circuit and Table list the associated Truth table. The implementation is then shown in Figure. The conventional Demultiplexer 1:4 logic diagram and its truth table were shown below. Here data is the input to the Demultiplexer, s1 and s0 are the select lines, y0, y1, y2, y3 are the output lines.

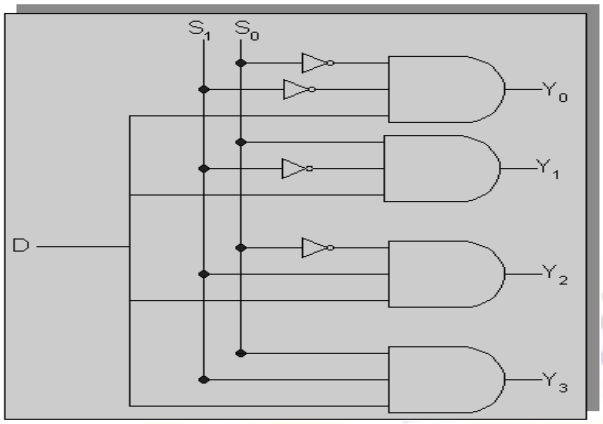


FIGURE 3.3 LOGIC DIAGRAM FOR A 1 TO 4 DEMULTIPLEXER

The design of a 1*4 Demultiplexer can be well defined also using the suggested online testable gate. Using the truth table of the CTSG gate and also the inputs and outputs of the CTSG gate, we can design a 1 * 4 demux very easily in a simple behavioral vhdl model.

As we are going to use CTSG gate in the implementation of the demux , the online testable feature of the CTSG gate also imparts to the demux design. So finally a online testable Demultiplexer is also designed using the CTSG gate.

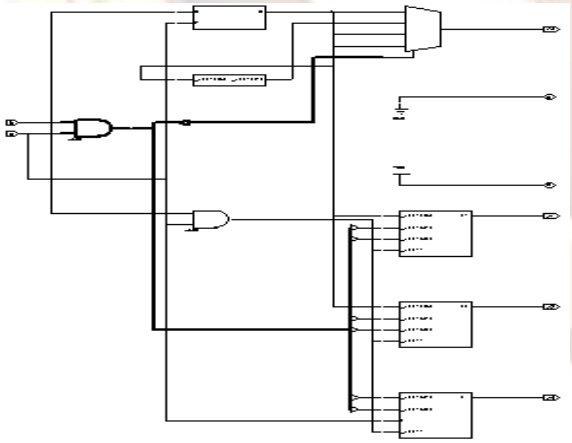


FIGURE 3.4 Rtl Schematic For 1*4 Demultiplexer design Using Ctsg Gate

IV. Conclusion

PARAMETER	RCA	CSA	BCD	MUX	DEMUX
POWER CONSUMPTION(mw)	50	50	50	92	92
MEMORY OCCUPIED(KB)	100652	100652	100652	99628	99628
COMBINATIONAL TIME DELAY (ns)	12.38	12.40	13.764	8.137	7.85

TABLE 5 Discussion of Paremeters

Here RCA refers to Ripple Carry Adder.
CSA refers to Carry Skip Adder.
BCD refers to BCD Adder.
MUX refers to 4*1 multiplexer.
DEMUX refers to 1*4 de multiplexer.
The focus of this paper is towards the efficient design of online testable multiplexers and demultiplexers using a novel online testable reversible gate CTSG. The proposed gate is shown better than the existing testable reversible gate in terms of computation complexity. The proposed online testable reversible adders are demonstrated efficient in terms of number of reversible gates, garbage outputs and unit delay, compared to recently proposed work. Design of online testable reversible BCD adder is addressed first time in literature. The online testable reversible OTG gate and adders proposed in this paper will form the basic building block of testable quantum/reversible system. At present the work done using OTG gate was limited upto the design of fast adders, Multiplexer and de Multiplexer. In future, the work can be extended upto the design of an ALU which is also online testable. The power dissipation, power utilization, unit time delay and others can be optimized to a level so that this can replace the conventional ALU used in present days.

REFERENCES

[1] Landauer, R., 1961. Irreversibility and heat generation in the computingprocess. IBM J. Res. Develop., 5: 183-191.

[2] C.H. Bennett , "Logical Reversibility of Computation", *IBM J.Research and Development*, 17, 525 (1973).

[3] D.P. Vasudevan , P.K. Lala and J.P. Parkerson, "Online Testable Reversible Logic Circuit Design using NAND Blocks" , *Proc,Symposium on Defect and Fault Tolerance*, October 2004, pp-324-331.

[4] D. P. Vasudevan, P. K. Lala, J. P Parkerson, "Reversible-Logic Design With Online Testability", *IEEE Transactions onInstrumentation and Measurement*, VOL. 55, NO. 2, pp. 406-414, APRIL 2006.

[5] E. Fredkin, T Toffoli, "Conservative Logic", *International Journal of Theor. Physics*, vol. 21, nos. 3-4, pp. 219-253, 1982.

[6] T. Toffoli., "Reversible Computing", *Tech memo MIT/LCS/TM-151*,MIT Lab for Computer Science (1980).

[7] K. N. Patel, J. P. Hayes, and I. L. Markov, ``Fault Testing for Reversible Circuits" , *IEEE Trans. on CAD, 23(8)*, pp. 1220-1230,August 2004.

[8] P.O. Boykin and V.P. Roychowdhury, "Reversible fault-tolerant logic" *Proceedings International Conference on Dependable Systems and Networks, 2005 (DSN 2005)*, 28 June-1 July 2005, pp.444-453.

[9] D.P. Vasudevan , P.K. Lala and J.P. Parkerson, "Online Testable Reversible Logic Circuit Design using NAND Blocks" , *Proc,Symposium on Defect and Fault Tolerance*, October 2004, pp-324-331.

[10] D. P. Vasudevan, P. K. Lala, J. P Parkerson, "Reversible-Logic Design With Online Testability", *IEEE Transactions on Instrumentation and Measurement*, VOL. 55, NO. 2, pp. 406-414, APRIL 2006.

Authors

Ms Lavanya Thunuguntla has 6 years of Teaching experience and presently working as an Associate Professor in the Department of ECE in Hyderabad Institute of Technology and Management (HITAM), Hyderabad, AP(India).She received her B.Sc degree in Computer Science from Acharya Nagarjuna University in 2002, M.Sc degree in Physics from University of Hyderabad, Hyderabad in 2004 and M.Tech from Indian Institute of Technology (IIT) Kharagpur in 2007. She has Professional Membership in IEEE. She has various journal publications in International journals in the field of Nano Technology etc. She has guided several M.Tech and B.Tech projects. She has strong motivation towards research in the fields of Nano Technology, Microwave and Optical & Analog Communications ,VLSI system design etc.

Mrs Bindu Madhavi K has 7 years of Teaching experience and presently working as an Assistant Professor in the Department of ECE in Hyderabad Institute of Technology and Management (HITAM), Hyderabad, AP(India).She received her B.Tech degree in ECE from JNTU in 2003, M.Tech in VLSI System Design from JNTU ,Hyderabad. She has guided several M.Tech and B.Tech projects.Her area of interest is VLSI System Design and Communication Systems.

Sri. T. Pullaiah Working as a Professor & HOD in Hyderabad Institute of Technology & Management has 13 years of teaching experience. His area of interest is VLSI & analog circuits.