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A Low-Cost First-Order Sigma-Delta Converter Design and Analysis in 0.18µm Technology

Jayendra Sikarwar[1], R. C. Gurjar[2]

Electronics & Instrumentation Engg. Department,
Shri G.S.Institute of Technology and Science, Indore, India

Abstract-This paper presents the design technique for a low-cost first order narrow band sigma-delta modulator in a standard 0.18*µm CMOS* technology for biomedical sensor applications.This circuitry performs the function of an analog-to-digital converter. A first-order 1-bit sigma-delta (Σ-Δ)analog-to-digital converter is designed and simulated using Cadence 0.18 µm CMOS process technology with power supply of 1.8 V through Cadence. The analysis of sigma-delta modulator structures and the design flow were given. The modulator is proved to be robustness, the high performance in stability .The simulation are compared with those from a traditional analog-to-digital converter to prove that sigma-delta is performing better in the case of weak signals acquisition.

Index Terms-First order modulator,Op-Amp Comparator, DAC, Differentiator , 1 bit Output.

I.INTRODUCTION

The rapid growth of mobile electronic systems increases the demand for developing low-cost and low-power circuit technique with high performance. An essential building block of such systems is the analog-to-digital converter (*ADC*). Sigma delta (ΣΔ) modulators are one of the preferred architectures for high resolution converters. For the design of analog circuits, low voltage and relatively high threshold have brought enormous challenges: some of the traditional circuit are no longer applicable or even don't work at low voltage, such as restricting the stack structure of output swing is no longer applicable to improve the low voltage DC gain of op-amp ; the lower supply voltage means the reduction of signal swing, but the noise of the circuit does not decrease with the reduction of supply voltage, thus it becomes very difficult that achieving higher signal to noise ratio in lower voltage. The main job of this paper to introduce modulator which is suitable for the application of low-voltage and low-power consumption, reducing the requirement of Op-Amp DC gain, circuit complexity, area and power consumption from the system level; Secondly, selection comparator, DAC proposed by the literature[2], which makes greatly reduced power consumption compared with the operational amplifier of two levels[1]. It is very important for reducing the power consumption of the entiresystem; Finally, a First order modulator of low-voltage is achieved.

II.OPTIMUM TOPOLOGY DELTA SIGMA ARCHITECTURE

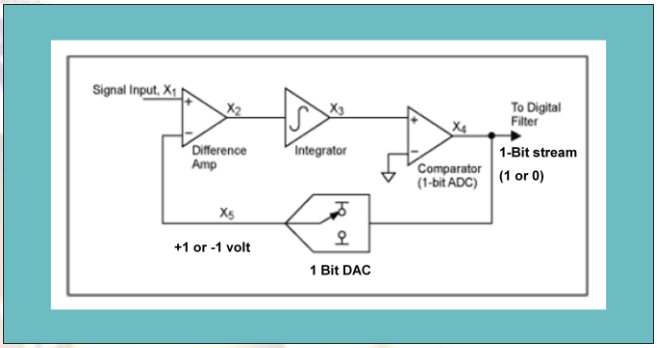


Fig:-First-order Σ-Δ modulator.

The term of Σ-Δ A/D converter has become almost synonymous with noise shaping A/D converter. Oversampling reduces the quantization noise power in the signal bandwidth by spreading the quantization noise power over a larger frequency range [4]. Noise shaping attenuates this noise in the signal bandwidth and amplifies it outside of this bandwidth. Low-pass filter attenuates the out-of-band quantization noise. A down sampling circuit is following to obtain the Nyquist rate output. This is the work principle of Σ-Δ A/D converter. The following is the mathematics analysis of first-order Σ-Δ modulator. Referring to Fig. in discrete-time domain,

$$y[n] = x[n-1] + e[n] + e[n-1] \quad (1)$$

Where, y[n] is the digital output;
x[n] is the input signal after sampling;
e[n] is the quantization of internal 1-bit A/D converter. The output noise due to the quantization error in the Σ-Δ modulator is,

$$q[n] = e[n] - e[n-1] \quad (2)$$

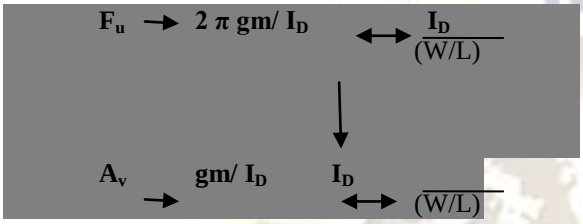
Cadence 0.18µm CMOS technology to implement the first-order Σ-Δ modulator in a circuit design is shown in Fig.1. In this circuit, the input analog signal is a sinusoidal 1 kHz waveform with 250 mV peak-to-peak voltage. Oversampling signals are generated by a non-overlapping clock circuit with a frequency of 250 kHz. The integrator is formed using switch capacitor as shown in Fig III The internal 1-bit A/D converter is made of a comparator.

III.TWO STAGE OP-AMP DESIGN METHODOLOGY

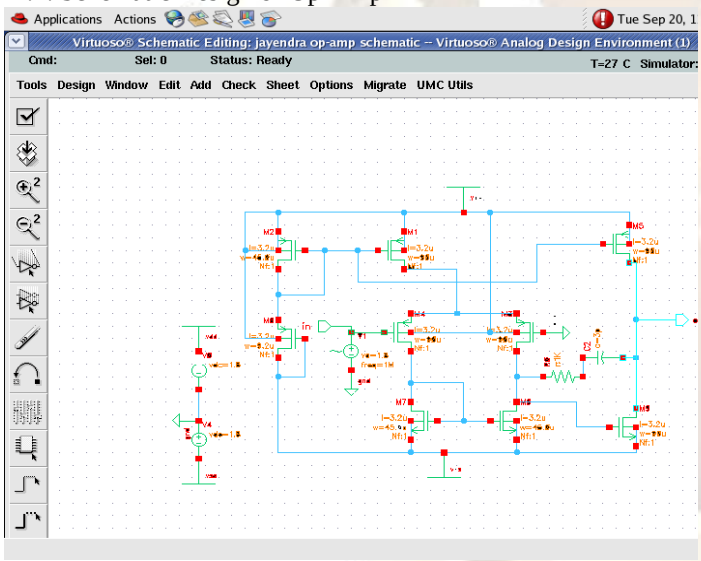
III.1. Sizing Algorithm

MOS transistors are either in strong inversion or in weak inversion. The design methodology based G_m/I_D characteristic, proposed by allows a unified synthesis methodology in all regions of operation the MOS transistor. We consider the relationship between the ratio of the transconductance G_m over the DC drain current I_D, and the normalized drain current I_D / (W/L) as a fundamental design relation[7]. G_m/ I_D are based on its relevance for the following reasons:

- It is strongly related to the performance of analog circuits;
- It gives an indication of the device operation Region;
- It provides a simple way to determine the transistors dimensions.



III.2. Schematic Design of Op-Amp

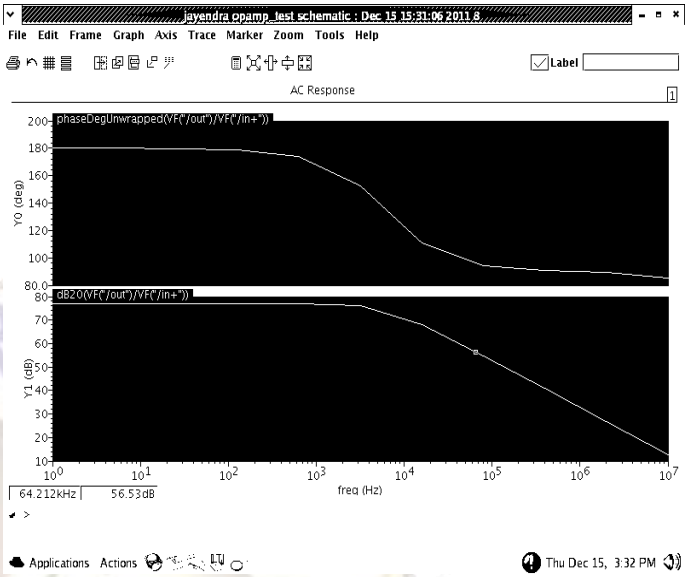


After applying the design strategy, we obtained the parameters computed and summarized in Table 1.

Transistor	W(µm)
M_1	90
M_2	45
M_3	90
M_4	90
M_5	90
M_6	45
M_7	45
M_8	9
M_9	45
R,C	2 ohm,2pf

Table 1:- Width of different Transistors

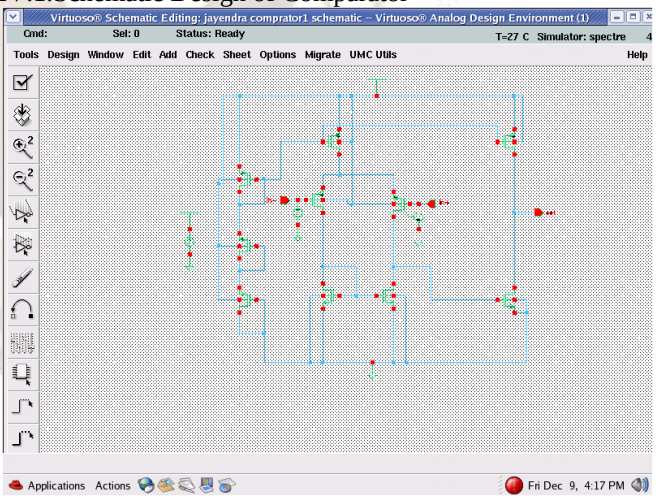
III.3. Gain And Phase Plot Of Op-Amp



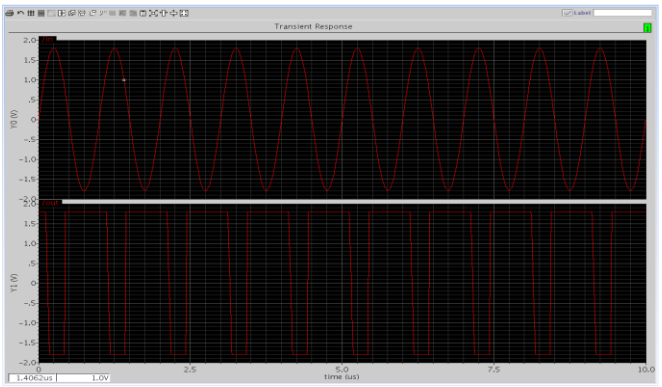
IV.Designing of Comparator

The one-bit quantizer as reported in [4] is used in this work .It is realized withCMOS Transister. The whole comparator is a pure dynamic circuit, which is very power efficient [1]. The offset voltage is mainly defined by matching of the input transistors. The only key design issue that is related to comparator design is propagation delay. The comparator circuit does not consume any static power, only dynamic power.

IV.1.Schematic Design of Comparator



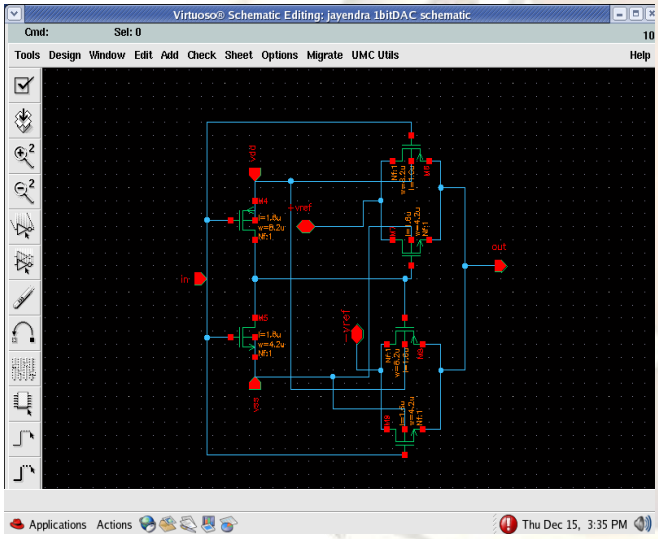
IV.2.Simulated waveform of Comparator



V. 1-bit D/A Converter Design

The structure of this converter made-up of transmission gate and inverter. Here the vref is set to 250mV, and the -vref is -230mV, in order to satisfy the output voltages. From the simulation results, it shows, if the input is 1V, then the output will equal -250mV; otherwise if the input is 0V, the output will be 250mV.

V. 1.Schematic of D/A Converter Design



VI. Designing and Simulation of First Order Σ-Δ Modulator

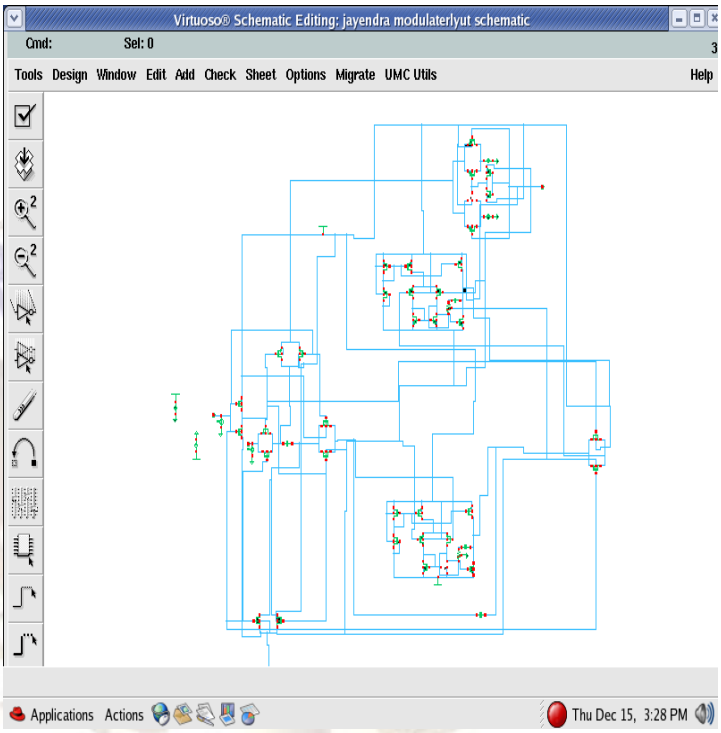
A sinusoidal input to a 1-bit Σ-Δ converter and its corresponding digital outputs as a result of using oversampling frequencies are as shown in VI.1. In the design of Σ-Δ converter, several factors are quite important, which are showing in the following formulas.Of course, with greater oversampling frequency, the output resolution is better, and hence 250 kHz oversampling frequency is chosen. Oversampling ratio

(OSR), OSR = fs/2fB ..... (3)

Where, fB is the frequency of input signal;
fs is the frequency of sampling signal.
Signal to noise ratio (SNR),

SNR = 30log10(OSR)-3.14 …. (4)
Overall resolution (N),
N = (SNR-1.76)/6.02 ….. (5)

VI.1 Schematic of first OrderΣΔModulator



VI.2 Simulated Waveform of first Order ΣΔModulator

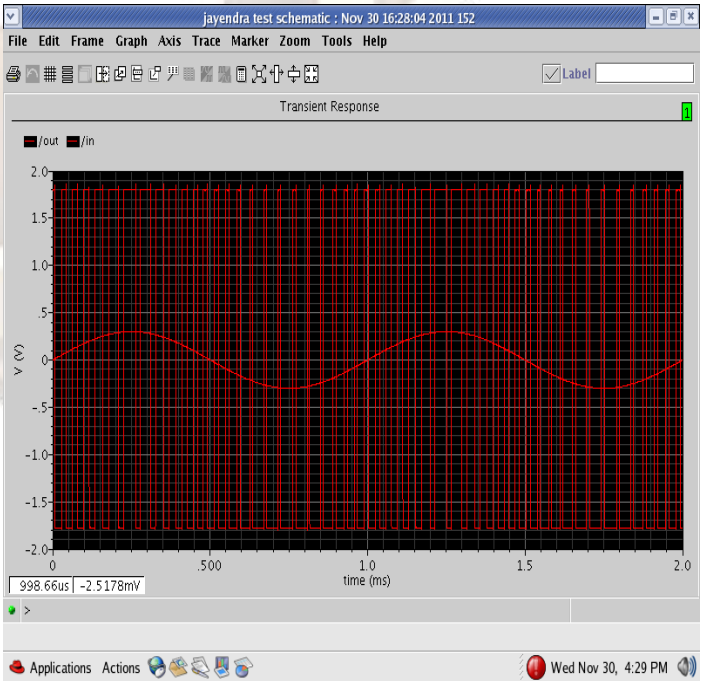


Figure :- AC Response Of Modulator

Results summary

Parameters	Results
Technology	0.18 µm
OP-Amp BW	10 kHz
SNR	68.79 dB
Clock Frequency	250 KHz
Unity Gain BW	64 MHz
Gain	77 dB
Phase Margin	54^{o}
OSR	250

Table 2. Results

VII CONCLUSIONS

This paper presents a Σ-Δ interface circuit design, its analysis for biomedical sensor applications, and simulation results. The results demonstrate that the usage of an Σ-Δ modulator allows very weak analog signals to be converted to an extremely high resolution digital output. Choosing cadence .18µm CMOS process for designing the circuit, allows. This Σ-Δ modulator has an input signalfrequency of 1KHz, oversampling frequency of 250 kHz, oversampling ratio (OSR) of 250; and signal-to-noise ratio of 68.79dB.

VIII ACKNOWLEDGMENT

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Author's Profile

Jayendra Sikarwar received the B.E. degree in Electronics and communication Engineering from I.T.M. Gwalior, India in 2008 and Pursuing MTech. Degree in Microelectronics And VLSI Design in Department of Electronics & Instru. Engineering , S.G.S.I.T.S.Indore India.

R.C.Gurjar received the B.E. degree in Electronics Engineering from R.G.P.V.University , India . and M.E. Degree in Digital Techniques & Instrumentation Engineering from SGSITS
INDORE, under the Rajiv Ghandhi Technical University Bhopal, India. He has been teaching and in research profession since 2007. He is now working as Asst. Professor in Department of, Electronics & Instrumentation Engineering S.G.S.I.T.S,Indore,India. His interest of research is in Designing of Microcontroller and Microprocessor .