Raghuwar Sharan Gautam,P. K. Jain,D. S. Ajnar/ International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com
Vol. 2, Issue 1,Jan-Feb 2012, pp.566-570

# Design of Low Voltage Folded Cascode Operational Transconductance Amplifier with Optimum Range of Gain and GBW in 0.18µm Technology

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**Abstract- An optimum OTA topology is done in order to optimize MOS transistor sizing. Also, the design of Folded Cascode OTA, which works for frequencies that lead to a baseband circuit design for RF application, is based on transistor sizing methodology. Simulation results are performed using CADENCE software and virtuoso spectre model for CMOS 0.18µm process technology, BSIM3V3 model simulator show that the designed folded cascode OTA has a 80.5dB DC gain and provides a gain bandwidth product 452MHz.**

Keywords- CMOS IC design, optimization, folded cascade OTA, gm/ID methodology, Wilson current mirror, Optimization.

## I.INTRODUCTION

The evolution of the microelectronics industry is distinguished by the raising level of integration and complexity. It aims to decrease exponentially the minimum feature sizes used to design integrated circuits. The cost of design is a great problem to the continuation of this evolution. Senior designer's knowledge and skills are required to ensure a good analogue integrated circuit design. To fulfil the given requirements, the designer must choose the suitable circuit architecture, although different tools partially automating the topology synthesis appeared in the past [1]-[4].The optimization becomes an important method; a heuristic process was developed in [5]. Designing high-performance baseband analog circuits is still a hard task toward reduced supply voltages and increased frequency. Current tendency focus on some radio-software receivers which suppose a RF signal conversion just after the antenna. Thus, a very higher sampling frequency and resolution analog-to-digital converter design is required. The Operational Transconductance Amplifier (OTA) is a basic element in this type of circuit whether switched capacitors technique is kept for ADC design. Our target was to design a folded cascode OTA circuit insight of Sigma Delta analog-to-digital converter design using for wide band radio applications.

This paper is organized as follows. An optimum Architecture of the folded cascode OTA was introduced in section II and its function was analyzed to extract the circuit performances. Section III describes an approach for designing this OTA, clarifies specific design issues, and results. While section IV provides concluding remarks.

## II.OPTIMUM TOPOLOGY OTA ARCHITECTURE

Several fundamental issues exist when selecting an optimal architecture for the operational transconductance amplifier. This choice aimed both at large gain and large bandwidth performances. In order to achieve high gain, the differential telescopic topologies can be used. This topology 566cascade566 both the differential pair transistors and current mirror to increase load resistance (Fig.1)[6].

The telescopic architecture is a better candidate for a low power consumption and low noise OTA. [7] The performance of simple OTA is limited by its input and output voltage swing. To overcome these limits of simple OTA and have an improved performance a Folded Cascode OTA is used. Although, telescopic OTA has a limited

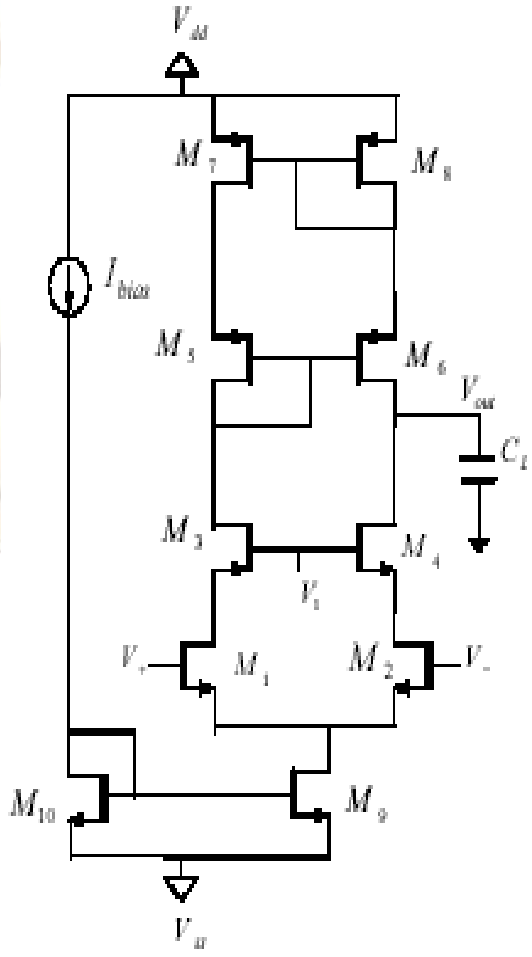


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Figure 1. Telescopic OTA

input and output swing. In order to alleviate some of the drawbacks of telescopic operational amplifier, a folded cascode OTA based on Wilson mirror can be used.

II.I. Basic configuration CMOS Folded Cascode OTA

The operational transconductance amplifier (OTA) is used as basic building block in many switched capacitor filters OTA is basically an op-amp without an output buffer and can only drive capacitive loads [7], [8].

An OTA is an amplifier where all nodes are low impedance except the input and output nodes. A useful feature of OTA is that its transconductance can be adjusted by the bias current. Filters made using the OTA can be tuned by changing the bias current Ibias[9]. Two practical concerns when designing an OTA for filter applications are the input signal amplitude and the parasitic input/output capacitances.

Large signals cause the OTA gain to become non-linear. The external capacitance should be large compared to the input or output parasitic of the OTA. This limits the maximum frequency of a filter built with an OTA and causes amplitude or phase errors. These errors can usually be reduced with proper selection of Ibias. The performance of simple OTA is limited by its input and output voltage swing. To overcome these limits of simple OTA and have an improved performance a Folded Cascode OTA is used.

The folded cascode OTA is shown in Fig. 2 The name "folded cascode" comes from folding down n-channel cascode active loads of a diff-pair and changing the MOSFETs to p-channels. Folded cascode OTA has a differential stage consisting of PMOS transistors M9 and M10 intend to charge Wilson mirror. MOSFETs M11 and M12 provide the DC bias voltages to M5-M6-M7-M8 transistors. [10] Apply AC input Voltage between V+ and V-, cause the diff-amplifier drain current to become gmVin. This AC differential drain current is mirrored in the cascaded MOSFETs M1 to M6.

**The output Voltage of the OTA is given by:**

$$V_{out} = G_m V_{in} R_o \quad (1)$$

**The "Unity gain frequency" of the OTA is:**

$$F_u = 2\pi gm_9 / C_L \quad (2)$$

**$G_m$ is computed as:**

$$G_m = 2\pi GBW C_L \quad (3)$$

**The open-loop voltage gain is given by:**

$$A_V = \frac{\{gm_9\, gm_4\, gm_6\}}{I_D^2 (gm_4\lambda_N^2 + gm_6\lambda_P^2)} \quad (4)$$

Where $gm_9$, $gm_4$ and $gm_6$ are respectively the transconductances of transistors $M_9$, $M_4$ and $M_6$. $I_D$ is the bias current flowing in MOSFETs $M_4$, $M_6$, and $M_9$. Like, $C_L$ is the capacitance at the output node. $\Lambda_N$ and $\lambda_P$ are the parameters related to channel length modulation respectively for NMOS and PMOS devices. Taking the complementarities between the Transistors $M_4$ and M6 into account:

$$gm_4 = gm_6 \quad (5)$$

The gain expression becomes:

$$A_V = \frac{\{gm_9\, gm_4\}}{I_D^2 (\lambda_N^2 + \lambda_P^2)} \quad (6)$$

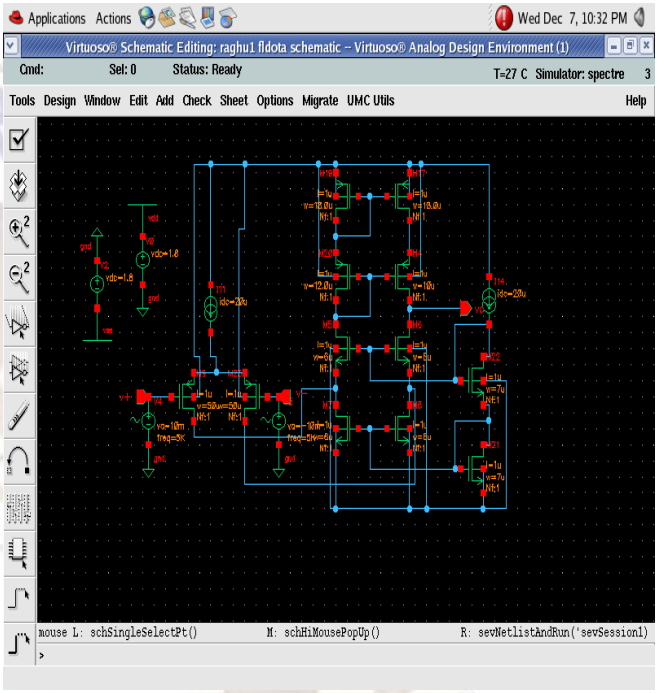


Figure 2. Folded Cascode OTA

## III. FOLDED CASCODE OTA DESIGN METHODOLOGY.

To show folded cascade OTS performances,this paper is interested in OTA design carrying. This design follows synthesis procedure based on the $g_m/I_D$ methodology[11].

III.1. Sizing Algorithm

MOS transistors are either in strong inversion or in weak inversion. The design methodology based $G_m/I_D$ characteristic, proposed by allows a unified synthesis methodology in all regions of operation the MOS transistor. We consider the relationship between the ratio of the transconductance $G_m$ over the DC drain current $I_D$, and the normalized drain current $I_D$ / (W/L) as a fundamental design relation[7]. $G_m/I_D$ are based on its relevance for the following reasons:

- It is strongly related to the performance of analog circuits;
- It gives an indication of the device operation Region;
- It provides a simple way to determine the transistor dimensions.

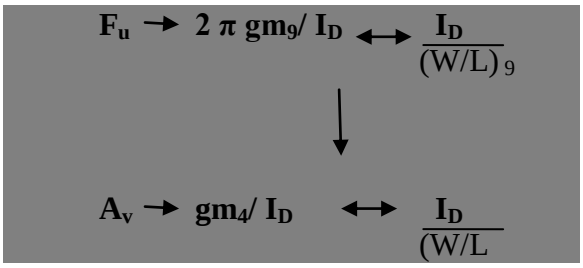


Figure 3. Design Plan

III.2. OTA Design

After applying the design strategy, we obtained the parameters computed and summarized in Table 1.

| Transistor | W(µm) | L (µm) |
|---|---|---|
| $M_1$ | 18 | 1 |
| $M_2$ | 18 | 1 |
| $M_3$ | 12 | 1 |
| $M_4$ | 10 | 1 |
| $M_5$ | 6 | 1 |
| $M_6$ | 6 | 1 |
| $M_7$ | 6 | 1 |
| $M_8$ | 6 | 1 |
| $M_9$ | 50 | 1 |
| $M_{10}$ | 50 | 1 |
| $M_{11}$ | 7 | 1 |
| $M_{12}$ | 7 | 1 |

Table 1. Width and lengths of different transistors

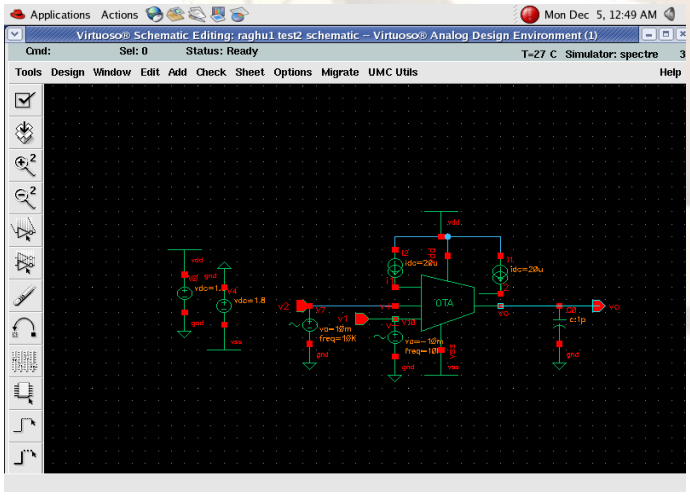


Figure 6. Test Bench of Folded Cascode OTA

III.3. Results

The designed Folded Cascode OTA was biased at 1.8V power supply voltage using CMOS technology of 0.18µm with the BSIM3V3 MOSFET model.

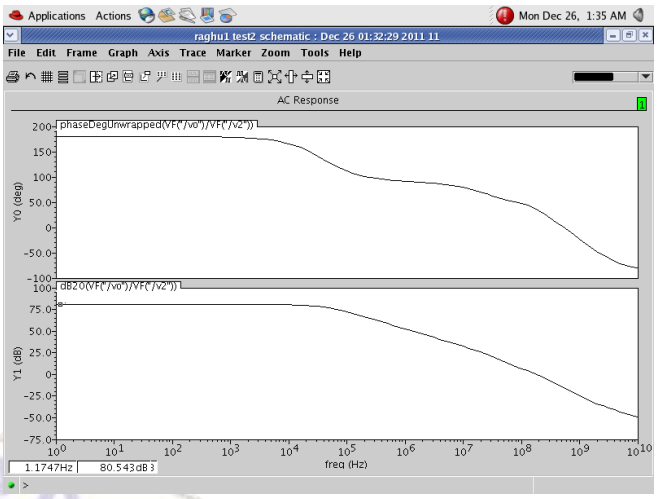


Figure 6. Gain and Phase Curve

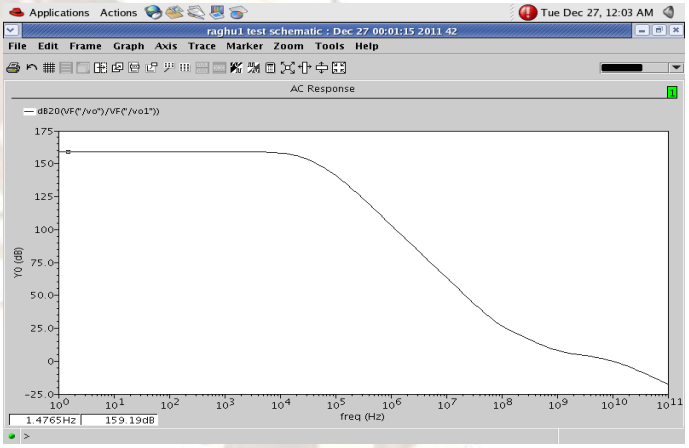


Figure 8.CMRR

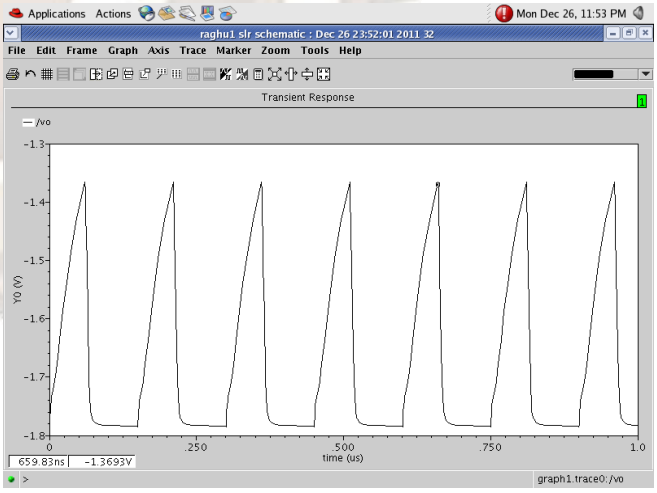


Figure 9. Slew Rate

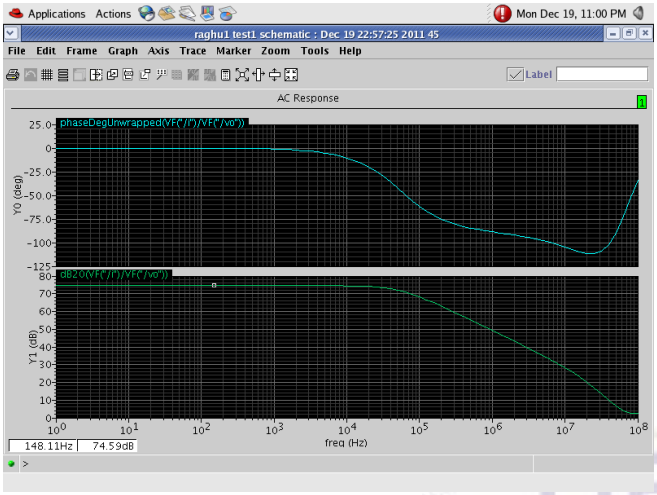


Figure 10. PSRR

**Results summary**

| Specifications | Results |
|---|---|
| Gain | 80.219 dB |
| GBW | 452 MHz |
| 3dB bandwidth | 42.7 KHz |
| $F_T$ | 176 MHz |
| Phase Margin | 40 Degree |
| Gain Margin | 15dB |
| Load | 0.1pf |
| Technology | 0.18µm |
| Supply Voltage | ±1.8V |
| Power Dissipation | 126 uW |
| Slewrate | 5 V/usec |
| CMRR | 159.19 |
| PSRR | 74.59 |

## IV CONCLUSIONS

Since the Folded Cascode OTA based on Wilson mirror has a limited output swing. For the folded Cascode OTA using a Wilson mirror, the maximum output voltage is set lower than: Vdd+VT+2Vdsat, so, we can use cascode mirror to compensate the fall to +2Vdsat. This paper presents an efficient OTA design, so, the goal to reach moderate gain and large bandwidth. Tranconductance cells are relatively simple circuits which allow operating for high frequencies. Future work involves the search of low power consumption and Ultra low-supply voltage structure, an update to nanotechnology process for RF application.

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