COMPARISON OF DIFFERENT REALIZATION TECHNIQUES OF IIR FILTERS USING SYSTEM GENERATOR

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2011-2012

ABSTRACT

This paper explains the design and implementation of different realization techniques of an IIR filter using System Generator. IIR filter can be used in Linear Predictive Coding and in Group Delay Equalizer. The synthesis report concludes the resource utilization of the selected FPGA.

1. INTRODUCTION

A Digital filter uses a digital processor to perform numerical calculations on sampled values of the signal. It can be classified into:
1) Infinite Impulse Response (IIR) filter.
2) Finite Impulse Response (FIR) filter.

IIR filters, when compared to FIR filters, have advantage in terms of computational complexity and require less memory.

There are several ways to realize IIR filters. Direct Form Realization is often the preferred approach in practice due to its simplicity and lower computational requirement. However this realization introduces coefficient quantization errors. IIR filters are very sensitive to filter quantization errors which can affect its stability.

The Lattice Realization has some advantages over Direct Form Realization. A notable feature of the lattice filters are the use of reflection coefficients as the filter parameters [1]. The reflection coefficients allow a straightforward supervision of the stability status, since the condition $|k_i| \leq 1$ can be easily monitored [2].

System Generator is a DSP design tool from Xilinx that enables the use of The Math works model-based design environment Simulink. Over 90 DSP building blocks are provided in the Xilinx DSP blockset for Simulink. There are several advantages of Xilinx which includes wrapping of MSB when the number is too large to be represented by integer bits; rounding of LSB to the nearest precision value.[3]

FPGA stands for Field Programmable Gate Array. It belongs to a group of user programmable digital devices called Programmable Logic Devices (PLD's).FPGAs avoid high initial cost, the lengthy development cycles, and the inherent inflexibility of conventional ASICs. Also, FPGA programmability permits design upgrades in the field with no hardware replacement necessary, an impossibility with ASICs [6].

2. IIR FILTER REALIZATION TECHNIQUES

The IIR filter basically consists of a forward FIR filter, also known as all-zero filter, comprising of the numerator or 'b' coefficients for the zeros, and a feedback FIR for the denominator or 'a' coefficients for the poles. Transfer Function of an IIR filter is of the form:

$$H(z)= \sum_{n=0}^{\infty} h(n)z^{-n} = \frac{\sum_{K=0}^{M} b_k z^{-k}}{1+\sum_{k=1}^{N} a_k z^{-k}} \quad (1)$$

2.1 DIRECT FORM I REALIZATION

For equation (1) the Direct Form I structure is shown in fig. 1, where x(n) is the input, y(n) is the output $a_1, a_2 \ldots a_n$ are the denominator's coefficients and $b_0, b_1 \ldots b_m$ are the numerator's coefficients.

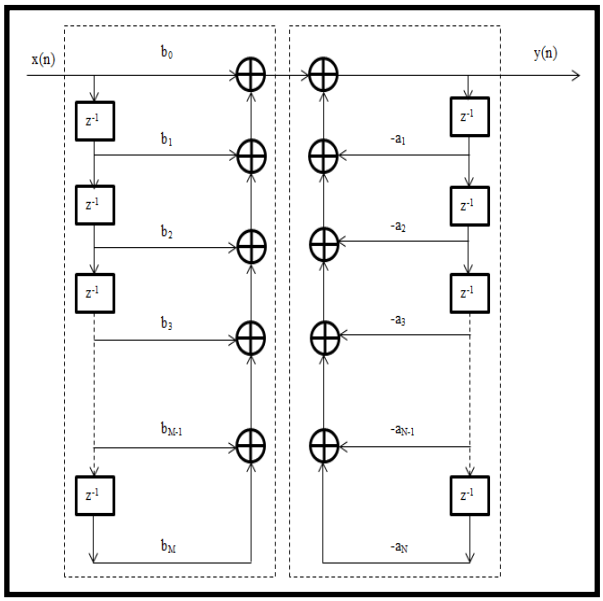

Figure 1. Direct Form I Structure [4].

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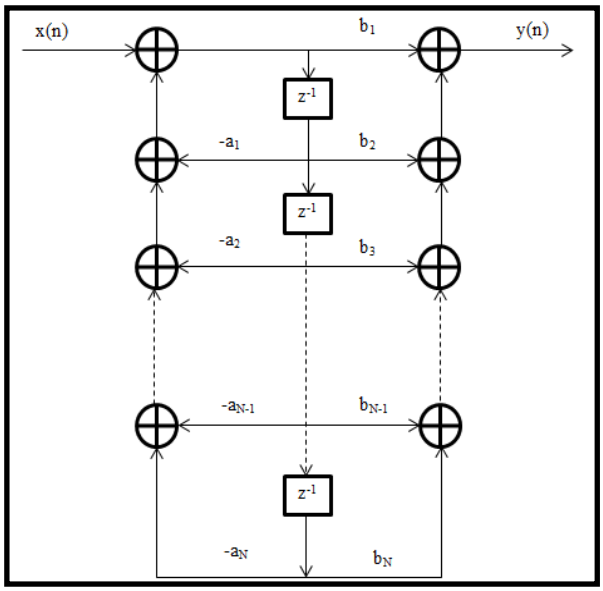

Figure 2. Direct Form II Structure [4].

2.3 LATTICE REALIZATION

For equation (1) the lattice structure is shown in fig. 3, where x(n) is the input, y(n) is the output $k_1, k_2 \ldots k_n$ are the reflection coefficients and $\alpha_0, \alpha_1 \ldots \alpha_n$ are the.

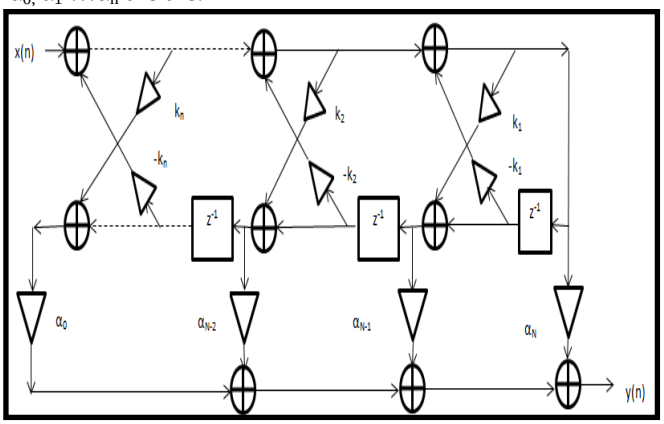

Figure 3.Lattice Structure [5].

3. RESULTS

Consider an IIR filter of order three as shown below

$$H(z) = \frac{0.44z^{-1}+0.362z^{-2}+0.02z^{-3}}{1+0.4z^{-1}+0.18z^{-2}-0.2z^{-3}} \quad (2)$$

For the above transfer function of the filter, k_1, k_2, k_3 and α_1, α_2, α_3, α_4 are 0.3573771,0.270833, -0.2 and 0.02,0.352,0.276533,-0.19016respectively, fs =65kHz, fc = 21.3916kHz.

The SysGen implementation of Direct Form I for equation (2) is shown in Fig. 4.

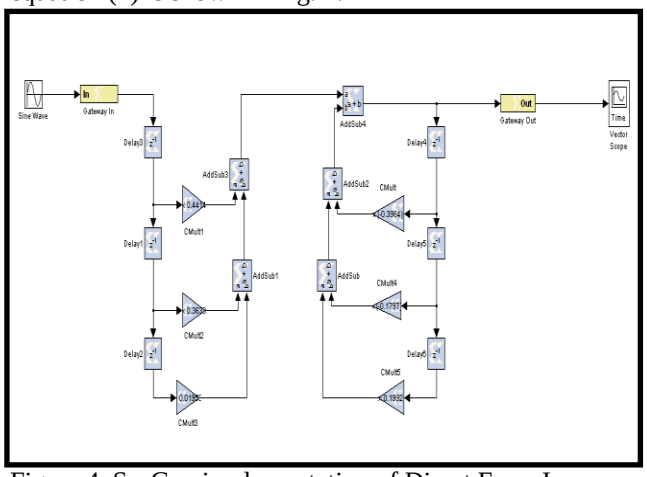

Figure 4. SysGen implementation of Direct Form I

The simulation result of Direct Form I is shown in Fig. 5.

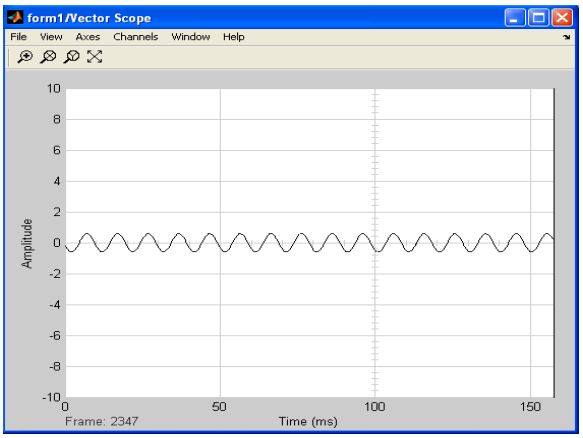

Figure 5.The Output seen on Vector Scope.

The SysGen implementation of Direct Form II for equation (2) is shown in Fig. 6.

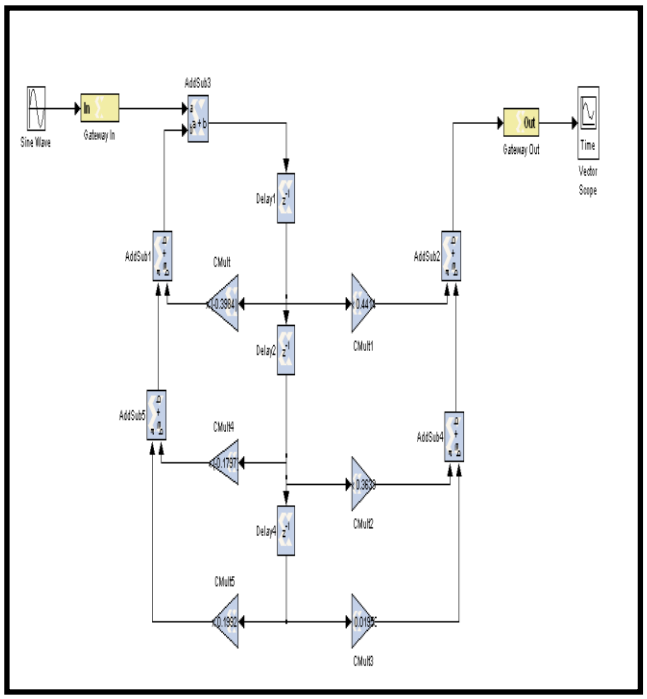

Figure 6.SysGen implementation of Direct Form II.

The simulation result of Direct Form II is shown in Fig. 7.

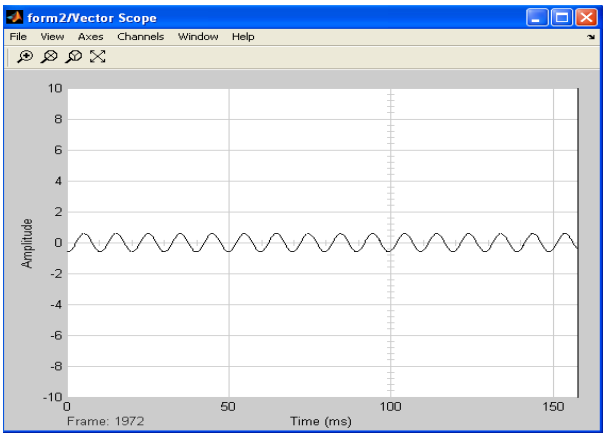

Figure 7.The Output seen on Vector Scope.

The SysGen implementation of Lattice Realization for equation (2) is shown in Fig. 8.

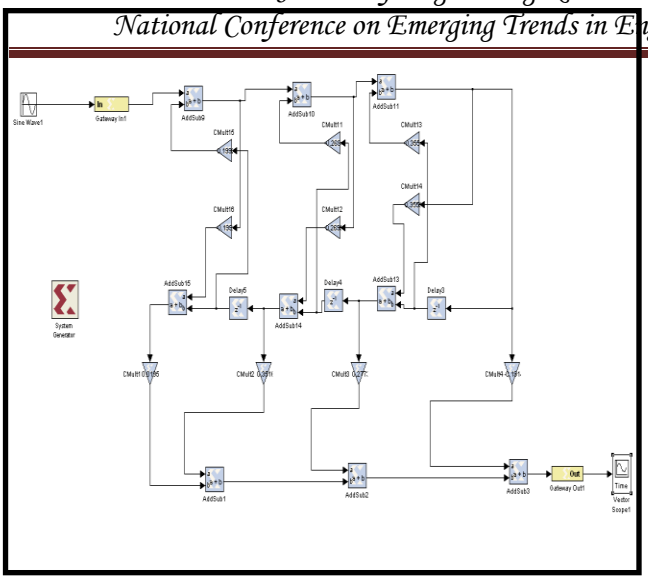

Figure 8. SysGen implementation of Lattice Realization.

The simulation result of Lattice Realization is shown in Fig. 9.

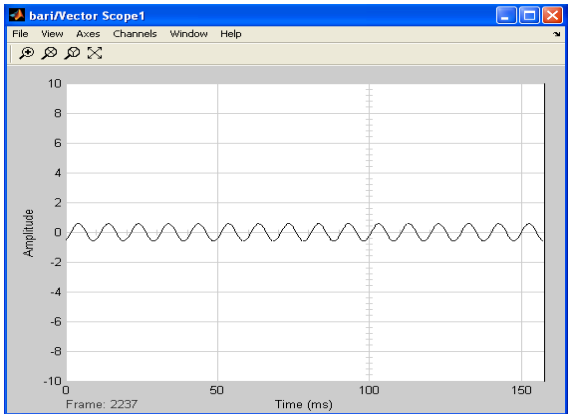

Figure 9.The Output seen on Vector Scope.

The Synthesis using Xilinx ISE tools resulted in the following synthesis report for a Spartan 3E xc3s500e-4fg320 as target FPGA. The results are shown in the following tables.

Table 3.1 Device Utilization Summary of Direct Form I

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	85	9,312	1%	
Number of 4 input LUTs	260	9,312	2%	
Number of occupied Slices	166	4,656	3%	
Number of Slices containing only related logic	166	166	100%	
Number of Slices containing unrelated logic	0	166	0%	
Total Number of 4 input LUTs	264	9,312	2%	
Number used as logic	260			
Number used as a route-thru	4			
Number of bonded IOBs	25	232	10%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.41			

Table 3.2 Device Utilization Summary of Direct Form II

Device Utilization Summary				[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	49	9,312	1%	
Number of 4 input LUTs	260	9,312	2%	
Number of occupied Slices	165	4,656	3%	
Number of Slices containing only related logic	165	165	100%	
Number of Slices containing unrelated logic	0	165	0%	
Total Number of 4 input LUTs	264	9,312	2%	
Number used as logic	260			
Number used as a route-thru	4			
Number of bonded IOBs	25	232	10%	
Number of BUFGMUXs	1	24	4%	
Average Fanout of Non-Clock Nets	2.53			

Table 3.3 Device Utilization Summary of Lattice Realization

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slices	30	4656	0%
Number of Slice Flip Flops	54	9312	0%
Number of 4 input LUTs	12	9312	0%
Number of bonded IOBs	25	232	10%
Number of GCLKs	1	24	4%

4. CONCLUSION

From the Device Utilization Summary Table, it can be concluded that Lattice Realization is faster when compared with Direct Form I and II Realizations, as the LUTs utilization is 0%. Implementing different types of Realization techniques of an IIR Filter using System Generator speeds up the simulation and gives more accurate results.The advantages are high processing speed, reduced power consumption and hardware compability for implementing on FPGA.

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