Hybrid Modulation Techniques for Multilevel Inverters

Ajaybabu Medikonda,
Student member IEEE,
Hindustan university, Chennai**.**

Abstract:

This project presents different sequential switching hybrid modulation strategies and compared for cascaded multilevel inverters.

Hybrid modulation strategies represent combinations of fundamental frequency modulation and multilevel sinusoidal modulation strategies and designed for performance of the well-known alternative phase opposition disposition, phase shifted carrier, carrier based space vector modulation, and single carrier sinusoidal modulations.

The main characteristic of these modulations are the reduction of switching losses with good harmonic performance, balanced power loss dissipation among the devices with in a cell, and among the series connected cells.

The proposed modulations can be easily extended to three phase, and higher level inverters, operates with same physical structure of the power module.
The feasibility of these hybrid modulations are verified through simulation results.

1. Introduction:

Ac loads require constant or adjustable voltages at their input terminals. When such loads are fed by inverters, it's essential that output voltage of the inverters is so controlled as to fulfil the requirements of AC loads. This involves coping with the variation of DC input voltage, for voltage regulation of inverters and for the constant volts/frequency control requirement.

Multilevel Inverters

Multilevel inverters are finding increased attention in industries as a choice of electronic power conversion for medium voltage and high-power applications, because improving the output waveform of the inverter reduces its respective harmonic content and, hence, the size of the filter used and the level of electromagnetic interference (EMI) generated by switching operation. Various multilevel inverter (MLI) structures are reported in the literature, and the cascaded multilevel inverter (CMLI) appears to be superior to other inverter topologies in application at high power rating due to its modular nature of modulation, control and protection requirements of each full bridge inverter (FBI). CMLI synthesizes a medium voltage output based on a series connection of power cells which use standard low-voltage component configurations. This characteristic allows one to achieve high-quality output voltages and input currents and also outstanding availability due to their intrinsic component redundancy. The power circuit for a five level inverter topology is shown in fig.1 used to examine the proposed modulation techniques. Many new modulations have been developed to cater the growing number of MLI topologies. They are aimed at generating a stepped switched waveform that best approximates an arbitrary reference signal with adjustable amplitude, frequency, and phase fundamental component that is usually a sinusoid in steady state. Since the modulation scheme is intended to be used in high-power converters, the main figures of merit pursued are high power quality and minimum switching frequency. These

two requirements compete with each other, and therefore, it is considered one of the major challenges in MLI technology.

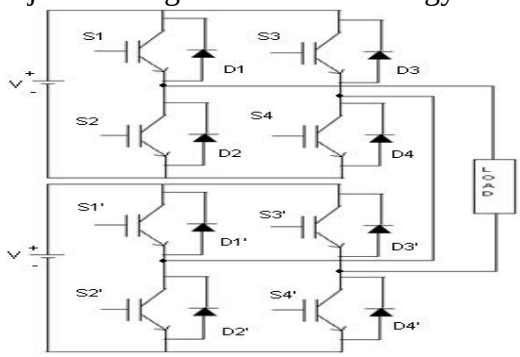

Fig 1: Schematic diagram of the inverter topology

Most of the modulation methods developed for MLI is based on multiple-carrier arrangements with pulse width modulation (PWM). The carriers can be arranged with vertical shifts (phase disposition, phase opposition disposition, and alternative phase opposition disposition PWM), or with horizontal displacements (phase shifted carrier PWM). Space vector modulation (SVM) is also extended for the MLI operation, offers good harmonic performance. These high frequency methods produce high frequency stepped voltage waveforms that are easily filtered by the load and, therefore, present very good reference tracking and low current harmonic distortion. However, this is also the reason for high switching losses, which is undesirable in high power applications. As a result, fundamental frequency modulation methods have been preferred. Selective harmonic elimination (SHE) has the advantage of having very few commutations per cycle and is therefore the one that achieves better efficiency. Nevertheless, offline calculations are necessary, making dynamic operation and closed-loop implementation not straightforward. In addition, SHE becomes unfeasible with the increase of the number of levels, since it is directly related to the number of angles, hence equations that need to be solved. Architecture for CPLD implementation with only logical elements is presented adopting sequential switching hybrid modulation (SSHM) algorithm with PWM circulation.

4. Multilevel Sinusoidal Modulation Schemes

A) Alternative phase opposition Disposition (APOD)

This technique requires m-1 carrier signals, for an m level inverter, to be phase disposed from each other by 180 degree alternatively as shown in Fig. For bipolar mode of operation four carrier signals have been taken. In the upper half two signals are 180 degrees out of phase with each other and the same case will repeat for lower half also.

APOD control technique for bipolar mode and unipolar mode is shown in Fig.4, Fig.5 respectively. In APOD control technique, most significant harmonics appear as sidebands around the carrier frequency f_c. There will not be any harmonics at f_c.

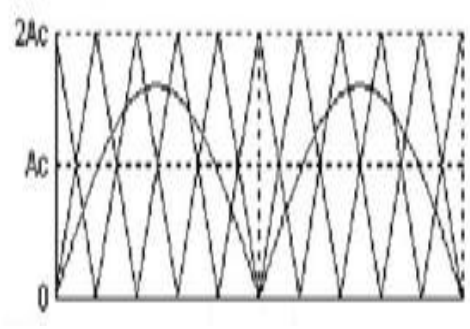

Fig 2: Carrier arrangement for APOD technique

B) Phase-Shifted Carrier PWM Technique (PSC)

Phase-shifted carrier (PSC) pulse width modulation (PWM) in its conventional form is a good solution for single-phase Cascaded inverters as alternative phase opposition disposition (APOD) PWM. The PSC technique consists of N-1 carriers with the frequency $W_C^1=W_C/(N-1)$, where is W_c the switching

frequency of the resulting PWM waveform. The carriers are shifted by 2π/ (N-1) incrementally

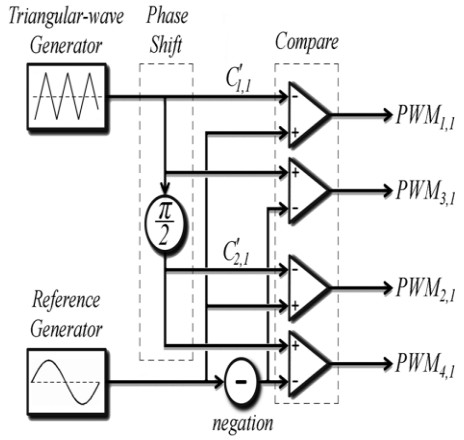

Fig 3: Block diagram for (five-level) PSC

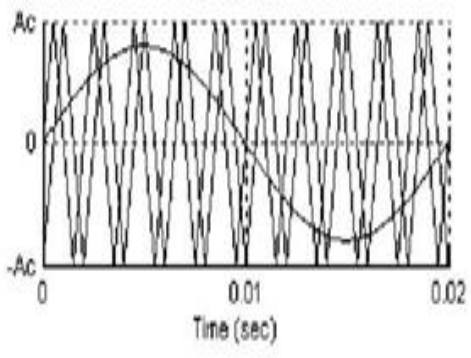

Fig 4: result for (five-level) PSC operation

C) Single-carrier sinusoidal PWM (SC-SPWM) technique

SC-SPWM that is shown in Fig.5 is a result of two sinusoidal reference signals with a frequency of f_0 and amplitude of A_m and one carrier signal. The carrier signal is a train of triangular waveforms with a frequency of f_c and amplitude of A_c. The modulation index is therefore defined as

$$m_i = A_m/MA_c \qquad (1)$$

Where M is the number of converter cells. The definition of the modulation frequency ratio m_f for converter is given as

$$m_f = f_c/ f_0 \quad \text{p.u.} \qquad (2)$$

Let N_1 be the number of the switching transitions that occur between the 0 p.u. level and the 1 p.u. This number is always (i.e. for multilevel output waveform) an odd number since the first switching transition is from 0 p.u. to 1 p.u. level. Let N_2 be the number of the remaining switching transitions occurred between 1 p.u. and 2 p.u. levels. This number can be either even or odd.

An intensive investigation for various values of the modulation index is carried out and it is found that for the selected modulation frequency (20 p.u.), there are eight different regions defining a different distribution ratio of the switching transitions (N_1/N_2). It is known that the harmonics are controlled by the frequency of the carrier waveform.

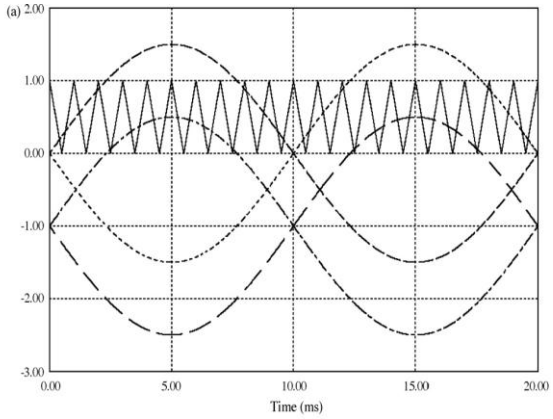

Fig 5: One carrier and two reference signals

D) Carrier-Based Space-Vector Modulation

Space vector modulation (SVM) is intrinsically a digital technique for generating Switching angles, offers relatively good performance at low modulation ratio. But the SVM becomes very difficult to achieve when the levels increases. To simplify the SVM, several

Methods have been proposed in recent years: such as decomposing the multilevel SVM to two level SVMs, implementing the SVM in a 60-degree coordinates.

However, it is complex in some steps yet, such as selection of switching-state. Therefore some researchers
Studied the relationship between SVM and MSPWM and try to use carrier-based PWM to
Achieve SVM's performance. Some techniques using common-mode injection in MSPWM are developed to close to SVM.

Wenxi Yao suggested that these techniques are harmonically equivalent, with the best Spectral performance being achieved when the nearest three space vector states are selected with the middle two vectors centered in each half carrier switching interval. This strategy is known as CBSVM. It is derived from the addition of a common offset voltage to the three-phase references. This will centre the active space-vectors in the switching period, and hence match the carrier modulation to get optimized SVM.

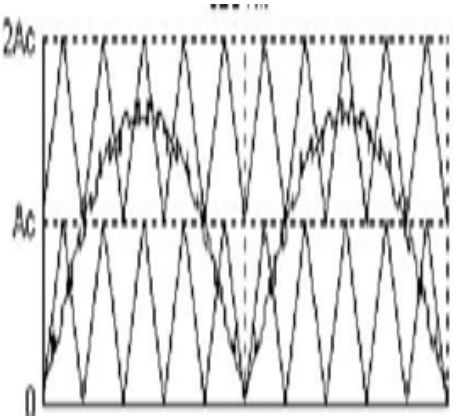

Fig 6: CBSVM signals

5. Proposed Hybrid Modulation

1. Basic principle of this Modulation

Hybrid modulation is the combination of fundamental frequency modulation (FPWM) and MSPWM for each inverter cell operation, so that the output inherits the features of switching loss reduction from FPWM, and good harmonic performance from MSPWM. In this modulation technique, the four switches of each inverter cell are operated at two different frequencies; two being commutated at FPWM, while the other two switches are modulated at MSPWM, therefore the resultant switching patterns are the same as those obtained with MSPWM.

A sequential switching scheme is embedded with this hybrid modulation in order to overcome unequal switching losses and therefore differential heating among the power devices. A simple base PWM circulation scheme is also introduced here to get resultant hybrid PWM circulation makes balanced power dissipation among the power modules. Fig.7 shows the general structure of the proposed SSHM scheme. It consists of modulation base generator, base PWM circulation module, and hybrid modulation controller (HMC) to generate new modulation pulses.

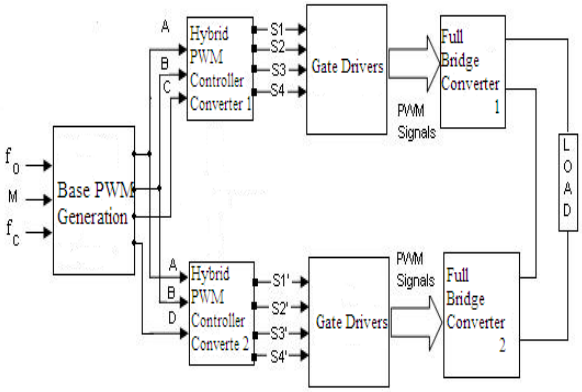

Fig 7: Hybrid Modulation SchemnBase Modulation Design

2. Base Modulation Design

In this modulation strategy, three base modulation pulses are needed for each cell Operation in a CMLI. A sequential switching pulse (*A*) is a square wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM and FPWM sequentially to equalize the power losses among the devices. FPWM (*B*) is a square wave signal synchronized with the modulation waveform; *B=1* during the positive half cycle of the modulation signal, and *B=0* during negative half cycle. A sequential switching pulse (SSP) and FPWM pulses are same for all inverter cells. MSPWMs (*C* or *D*) for each cell, differs depends upon the type of carrier and modulation signals used. The block diagram representation of base modulator design is shown fig.8

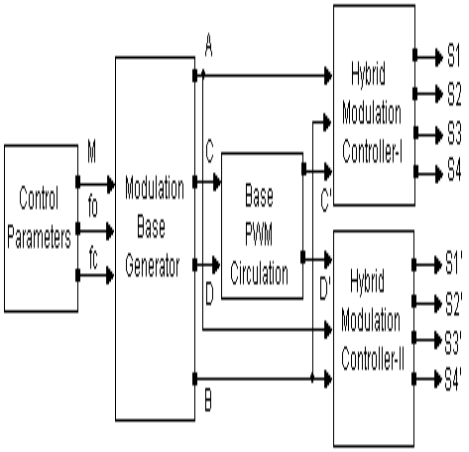

Fig 8: proposed sequential hybrid modulation

A) Hybrid Alternative phase opposition Disposition (HAPOD)

In this modulation strategy, three base modulation pulses are needed for each cell operation in a CMLI. A sequential switching pulse (*A*) is a square wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM, and FPWM sequentially to equalize the power losses among the devices. FPWM (*B*) is a square wave signal synchronized with the modulation waveform; *B=1* during the positive half cycle of the modulation signal, and *B=0* during negative half cycle.

APOD modulation pulses for cell-I (*C*) is obtained from the comparison between unipolar modulation waveform and carrier, while APOD for cell-II (*D*) is generated from the comparison between modulation waveform and carrier with DC bias of *-Vc+ 2Ac* as shown in fig 9.

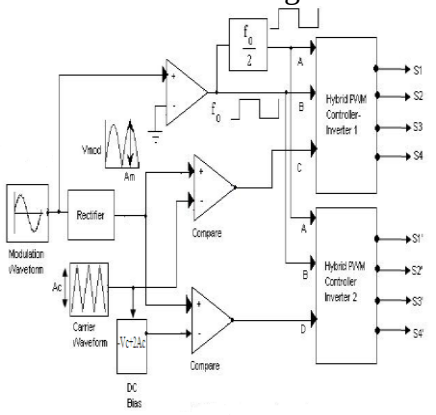

Fig 9: Hybrid Alternative phase opposition Disposition (HAPOD)

B) Hybrid Single-carrier sinusoidal PWM (HSC-SPWM) technique

In this modulation strategy, three base modulation pulses are needed for each cell

Operation in a CMLI. A sequential switching pulse (*A*) is a square wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM, and FPWM sequentially to equalize the power losses among the devices. FPWM (*B*) is a square wave signal synchronized with the modulation waveform; *B=1* during the positive half cycle of the modulation signal, and *B=0* during negative half cycle.

Scspwm modulation pulses for cell-I (*C*) is obtained from the comparison between unipolar modulation waveform and carrier waveform, while scspwm for

cell-II (*D*) is generated from the comparision between modulation signals with bias of –Ac and single carrier.

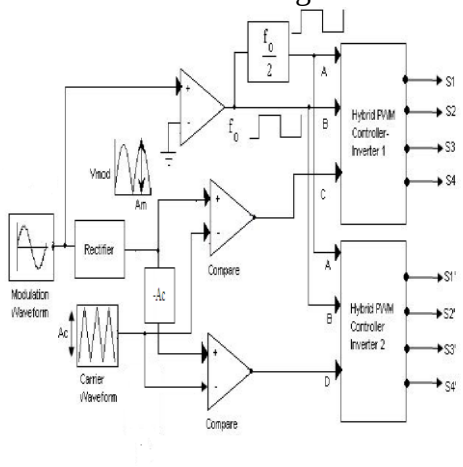

Fig 10: Hybrid Single-carrier sinusoidal PWM (HSC-SPWM) technique

C) Hybrid Carrier-Based Space-Vector Modulation (HCBSVM)

In this modulation strategy, three base modulation pulses are needed for each cell operation in a CMLI. A sequential switching pulse (*A*) is a square wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM, and FPWM sequentially to equalize the power losses among the devices. FPWM (*B*) is a square wave signal synchronized with the modulation waveform; *B=1* during the positive half cycle of the modulation signal, and *B=0* during negative half cycle.

CBSVM is based on a comparison of the modified sinusoidal reference (*Va +Voff +Voff ')* with each carrier to determine the voltage level that the inverter should switch to.

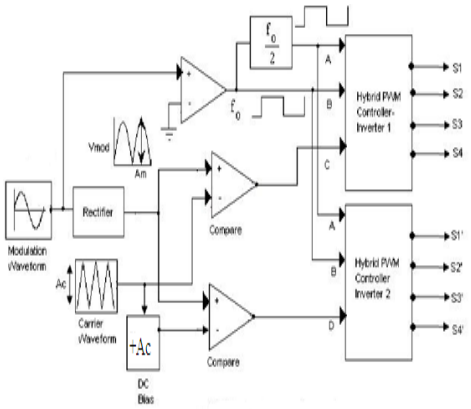

Fig 11: Hybrid Carrier-Based Space-Vector Modulation (HCBSVM)

D) Hybrid Phase-Shifted Carrier PWM Technique (HPSC)

In this modulation strategy, three base modulation pulses are needed for each cell operation in a CMLI. A sequential switching pulse (*A*) is a square wave signal with 50% duty ratio and half the fundamental frequency. This signal makes every power switch operating at MSPWM, and FPWM sequentially to equalize the power losses among the devices. FPWM (*B*) is a square wave signal synchronized with the modulation waveform; *B=1* during the positive half cycle of the modulation signal, and *B=0* during negative half cycle.

A PSC pulses are based on the comparison of modulation waveform with the corresponding PSC waveform for every cell in a CMLI.

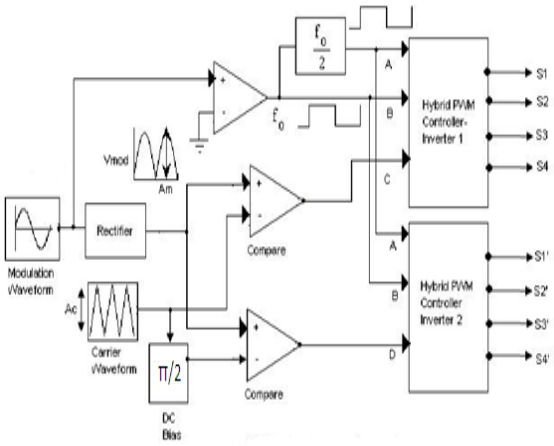

Fig 12: Hybrid Phase-Shifted Carrier PWM Technique (HPSC)

3. Base PWM Circulation

For long operating-time expectancy, it is important to share the power loss among every Module, and furthermore, to every power device in the cell. This is one of the key issues the Modulation should cover. A simple base PWM circulation scheme introduced here to get Resultant HPWM circulation among the power modules. The scheme of five-level base PWM Circulation is shown in fig.13, consists of two 2:1 multiplexer, and selects one among the two PWMs based on the select clock signal. The clock frequency is $f_0/4$, makes the time base for PWM circulation from one module to another.

After two fundamental frequency periods, the order is changed so that the first module HPWM becomes the second module; the second becomes the third and so on while the last module HPWM shifts to the first. *N*-level PWM circulation scheme is presented in fig.14, consists of clock generator,

Modulo-*K* counter and a multiplexer circuit. Modulo-*K* counter makes control signals for
Multiplexer to select appropriate input PWM channel. Multiplexer circuit consists of (*K X K:1*) Module for PWM selection, and it selects the PWM channel based on control signals. This PWM circulation is based on simple multiplexer logic circuits, which makes the applicability of the algorithm very effective in a CPLD.

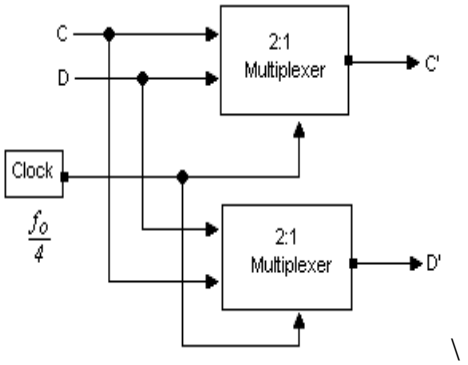

Fig 13: base PWM circulation for five-level

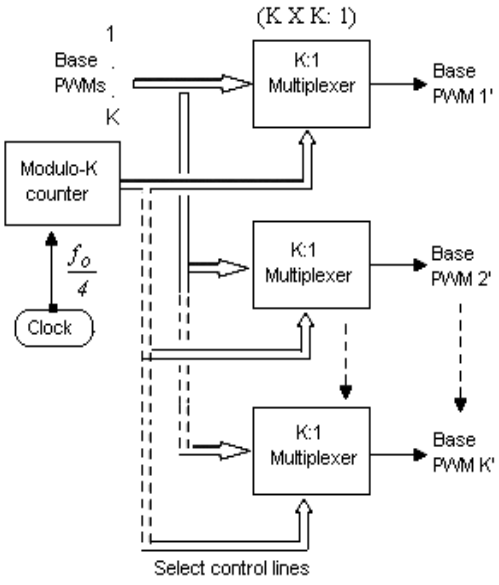

Fig 14: Scheme of base PWM circulation for *N*-level operation

4. Hybrid Modulation Controller

HMC combines SSP, and MSPWM, that produces SSHM pulses. It is designed by using a simple combinational logic and the functions for a five-level HPWM are expressed as

$$S1 = A\bar{B}C' + \bar{A}B \qquad S1' = A\bar{B}D' + \bar{A}B$$
$$S2 = \bar{A}\bar{B}C' + \bar{A}\bar{B} \quad \text{and} \quad S2' = \bar{A}\bar{B}D' + \bar{A}\bar{B}$$
$$S3 = \bar{A}\bar{B}C' + A\bar{B} \qquad S3' = \bar{A}\bar{B}D' + A\bar{B}$$
$$S4 = \bar{A}\bar{B}C' + AB \qquad S4' = \bar{A}\bar{B}D' + AB$$

Where *A* is a SSP, *B* is a FPWM, *C'* is a MSPWM for cell-I and *D'* is MSPWM for cell-II.

If SSP *A=1*, then *S1, S2, S1'* and *S2'* are operated with MSPWM, while *S3, S4, S3', S4'*are operated at FPWM. If SSP *A=0*, then *S1, S2, S1'* and *S2'* are operated at FPWM, while *S3, S4, S3'* and *S4'* are operated with MSPWM. Since *A* is a sequential signal, the average switching frequency amongst the four switches is equalized. Voltage stress and current stress of power switches in each cell is inherently equalized with this modulation. After every two fundamental periods, the HPWM pattern is changed so that the first module (*S1*, *S2*, *S3*, and *S4*) becomes the second module (*S1', S2', S3',* and *S4'*), and the second one shifts to the first. As a result, all inverter cells operate in a balanced condition with the same power handling capability and switching losses.

It is found that the proposed modulations offer lower THD compared to the conventional one, thus the superiority. Furthermore, it is noticed that higher the value of modulation index (M), lower the value of THD. Also, WTHD values are lower when the modulation index is closer to unity and when the carrier frequency increases. Throughout its linear modulation range, HPSC has the least harmonic distortion among SSHM schemes.

In order to show the feasibility of the proposed modulations, the spectral analysis was performed by using MATLAB/Simulink software and it is plotted in fig.15. The load resistance and inductance are 10Ω and the DC bus voltage is set at 100 V. The frequency of modulated wave and carrier wave are 50Hz and 1500 Hz respectively and the inverter is operated with linear modulation region.

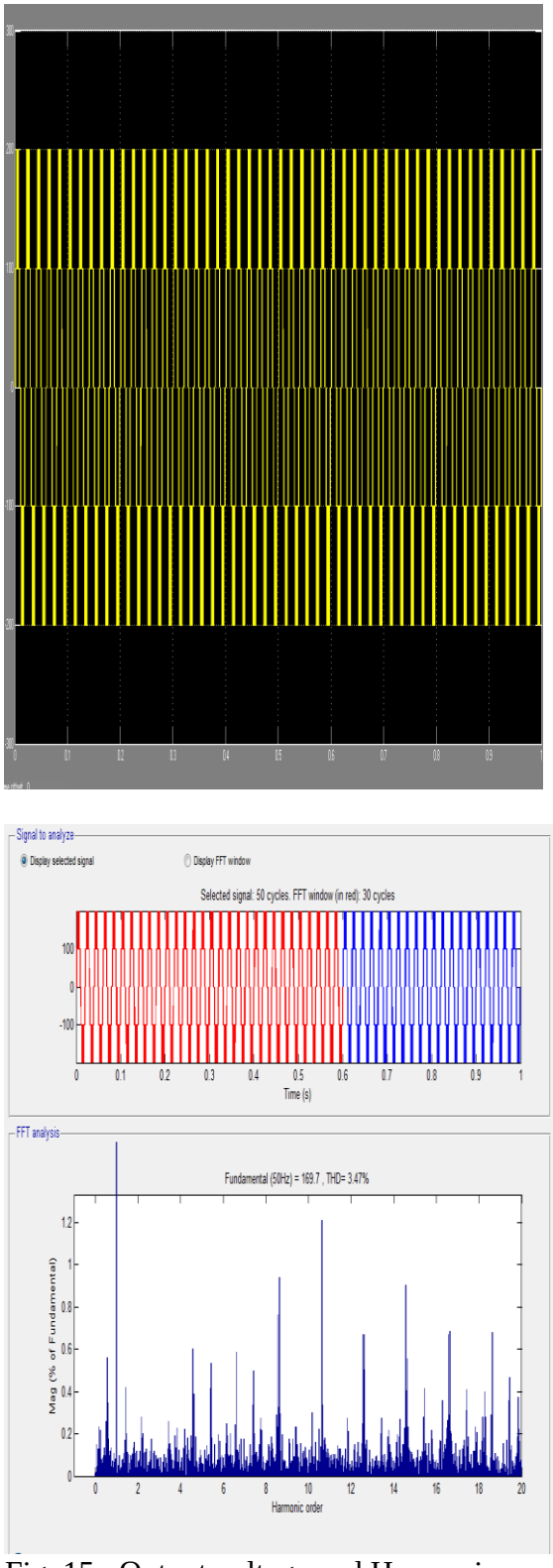

Fig 15 : Output voltage and Harmonic Analysis wave forms.

6. Conclusion

In this paper, a new family of SSHM techniques for CMLI, operating at a lower switching frequency is proposed. The proposed technique is applied to well-known MSPWM schemes; APOD, PSC, CBSVM, and SCSPWM. Compared to conventional MSPWM schemes, less number of commutations and considerable switching loss reduction is obtained while achieving the same fundamental voltage tracking. The harmonic performance of the SSHM schemes are analyzed in the entire range of modulation index and it seems to be good.

7. REFERENCES

[1] J.H.Kim, S.K.Sul, and P.N.Enjeti, " A carrier based PWM method with optimal switching sequence for a multilevel four-leg voltage source inverter," *IEEE Trans. Ind. Applic.*, Vol.44, No. 4, pp. 1239–1248, Jul. 2008.

[2] C.Govindaraju, K.Baskaran, "Performance analysis of cascaded multilevel inverter with hybrid phase-shifted carrier modulation," *Australian Journal of Electrical and Electronics Engineering*, Vol.7, No.2, pp.121-132, Jun. 2010.

[3] C.Govindaraju, K.Baskaran, "Efficient hybrid carrier based space vector modulation for cascaded multilevel inverter," *Journal of Power Electronics*, vol.10, No.3, pp.277-284, May 2010.

[5] J. Rodriguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[6] R. Teodorescu, F. Beaabjerg, J. K. Pedersen, E. Cengelci, S. U. Sulistijo, B. O.Woo, and P. Enjeti, "Multilevel converters—A survey," in *Proc. EPE Conf.*, 1999, pp. 2–11.

[7] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point clamped pwm inverter," *IEEE Trans. Ind. Appl.*, vol. IA-17, no. 5, pp. 518–523, Sep./Oct. 1981.

[8] T. Ishida, T. Miyamoto, T. Oota, K. Matsuse, K. Sasagawa, and L. Huang, "A control strategy for a five-level double converter with adjustable dc link voltage," in *Proc. Ind. Appl. Conf.*, Oct. 2002, vol. 1, pp. 530–536.

[9] S. K. Mondal, J. O. P. Pinto, and B. K. Bose, "A neural-networkbased space-vector pwm controller for a three-level voltage-fed inverter induction motor drive," *IEEE Trans. Power Electron.*, vol. 38, no. 3, pp. 660–669, May/Jun. 2002.

[10] N. Celanovic and D. Boroyevich, "A fast space vector modulation algorithm for multilevel three phase converters," *IEEE Trans. Ind. Appl.*, vol. 37, no. 2, pp. 637–641, Mar./Apr. 2001.

[11] S. Wei, B. Wu, F. Li, and C. Liu, "A general space vector pwm control algorithm for multilevel inverters," in *Proc. 18th Annu. IEEE APEC*, Feb. 2003, vol. 1, pp. 562–568.

[12] J. Holtz,W. Lotzkat, and A. M. Khambadkone, "On continuous control of pwm inverters in overmodulation range including six-step," *IEEE Trans. Power Electron.*, vol. 8, no. 4, pp. 546–553, Oct. 1993.

[13] H. Zhang, A. Von Jouanne, S. Dai, A. K. Wallace, and F. Wang, "Multilevel inverter modulation schemes to eliminate common-mode voltages," *IEEE Trans. Ind. Appl.*, vol. 36, no. 6, pp. 1645–1653, Nov./Dec. 2000.

[14] J. H. Seo, C. H. Choi, and D. S. Hyun, "A new simplified space-vector pwm method for three-level inverters," *IEEE Trans. Power Electron.*, vol. 16, no. 4, pp. 545–550, Jul. 2001.