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Performance Analysis for Multipliers Based Correlator

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ABSTRACT—
Here we are going to compares the use of multipliers and without Dsp slices cross-correlation for IEEE 802.16d orthogonal frequency division multiplexing (OFDM) timing synchronization on Xilinx Virtex- 6 and Spartan-6 field programmable gate arrays (FPGAs). We compare a multipliers correlation based design and pipelined correlator design to four different quantization's of in terms of resource utilization and power consumption. to make the design universal we have to use multipliers . Results show that multiplier system coefficient quantization can yield accurate timing synchronization, and does so at high clock speeds. Multiplier designs , and can be used where DSP Slice resources are insufficient, such as on low-power FPGA devices

Index Terms—Correlation, cognitive radio, field-programmable gate arrays (FPGA), IEEE 802.16 standards, orthogonal frequency division multiplexing (OFDM),Fast Fourier Transform(FFT) ,Inverse Fast Fourier Transform(IFFT) ,Symbol time offset (STO),Look up Table(LUTs)

I. INTRODUCTION

OFDM orthogonal frequency division multiplexing is modulation and multiplexing technique which is widely used in the wire and wireless communication system. OFDM is used in high speed mobiles. The main reason behind that OFDM transmission are introducing as a most used modulation technique because of its capacity of insuring high level robustness against interference.

As mention above OFDM technique used in wire and wireless technique various standard they are Fixed wi-fi system IEEE 802.11a standard, Mobile wi-fi system ieee802.11b standard ,Fixed wi-max system ieee802.11a standard, Mobile wi-max system ieee802.16e standard. The IEEE at 2005 introduce mobile wimax system (IEEE 802.16 standard) as strong competitor against most used 3g technology for the wireless system .And to creating more efficient mobile wimax system there is a method of a high level implementation of a high performance FFT for OFDM modulator and demodulator .To make OFDM more efficient DSP slice-based cross-correlation for IEEE 802.16 is designed for timing synchronization based on Xilinx Virtex-6 and Spartan-6 for FPGA field programmable gate arrays.[1] In OFDM system FFT and IFFT pairs are used in modulation and demodulation. As the OFDM system has multi path immunity that provide and easy implementation of FFT that's why OFDM technique becomes most popular modulation technique. But OFDM is sensitive to timing synchronization error. To rectified this sensitivity for the timing synchronization error the method is introduced in which frames are detected and method determine the beginning of data frame. There are lots of researches are done which has centralized idea to improve OFDM synchronization , its accuracy and performance of OFDM . to determine frequency offset and symbol timing, .Cyclic prefix (CP)-based methods were introduced [2]–[3], but this method is not sufficient to find the start of frame. To solve this, and to estimate the frequency offset OFDM frames begin with preamble symbols which can also be used [4]. To calculate the start of frame accurately also at low signal to noise ratio (SNR) Kishore and Reddy [5] presented an algorithm which require knowledge of the time domain preamble in the receiver. with help of this we can calculate cross-correlation metric between the known and received preamble symbols.

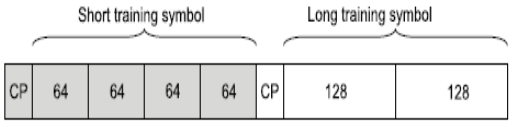

Fig. 1. Downlink preamble symbols for IEEE 802.16.

Complex calculation are required for the cross-correlation operation . As require synchronization method based upon the preamble symbol specified in IEEE 802.16d Kim and Park [6] has introduced two separate computation processes out of which first is autocorrelation is calculated for coarse symbol time offset (STO) and fractional carrier frequency offset (CFO) estimation to obtain more reliable frequency synchronization and to reduce hardware cost; and the second is, the fine STO and the integer CFO are estimated by performing cross-correlation between the received samples and known preamble. As we know FPGA is more flexible so it is used for OFDM as a base, as OFDM method is used for cognitive radios[7] . Various resources are present in latest FPGA which are used to implement cross-correlation. Here we are introduce the design of several correlators for timing synchronization with preamble symbols based upon IEEE 802.16d. We are replacing the specialized digital signal processing (DSP) Slices with help of multiplier based Xilinx Virtex-6 and Spartan-6 ..Here we have shortly studied , optimized FPGA designs, which is built to fit the FPGA architecture, and FPGA is further evaluate on the basis of their performance, utilization of resource, and most imp power consumption also timing synchronization accuracy, to understand whether a multiplier-based mapping is beneficial when using modern devices.

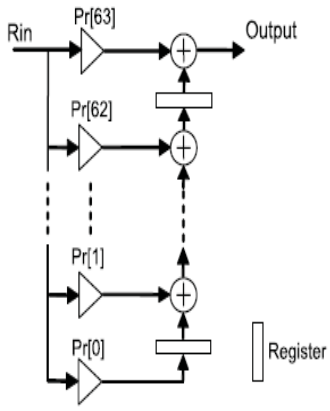

Fig. 2. Transpose direct form of the correlator.

II. IMPLEMENTATION OF CORRELATORS

As shown in Fig. 1 IEEE 802.16d [8] contains two consecutive OFDM symbols. CP is followed by the short symbol consists of four identical 64-sample fragments in time. This is followed by the long symbol which contains two repetitions of a 128-sample fragment and a CP [8]. To perform crosscorrelation The 64 samples in the short symbol are used. For timing synchronization with the received samples the correlators are designed to calculate cross-correlation with 64 constant coefficients. In this brief, we explore two approaches to implement such correlators. The first is based on Xilinx Virtex- 6 FPGA using multipliers, having standard approach to such an implementation. And The second uses multipliers correlation implemented on both a Xilinx Virtex-6 and a low-power Xilinx Spartan- 6 device. Both designs are designed to receive real and imaginary 16-b samples in Q1.15 fixed-point format. The output is the sum of 64 coefficient products, with each smaller than unity. So, the complex output words are in 21-b fixed-point Q6.15 format. If we want to implement such a design and if we are not considering FPGA architecture then synthesis tool may create a complications due to DSP block, so we are going to replace DSP blocks by multipliers .And if we want to design by using DSP block then there is compulsory availability of DSP blocks otherwise we cannot implement the design. So we have construct the universal design , by which we can calculate the correlator .This design also enjoy the flexibility of FPGA on Xilinx Virtex-6

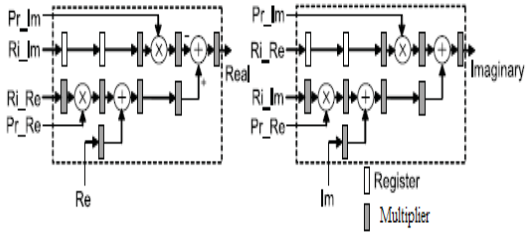

Fig. 3. Pipeline structure of the complex number multiply-add.

A. Design of Multipliers Based Correlator

Multiplication, multiply-accumulate, multiply-add, three-input add and many more functions are provided by configurable arithmetic unit which is given by multipliers present at Virtex-6.The system has permitted data path to be configured for various input combinations and register stage .Out of which three stage pipeline provide maximum performance. Multipliers are designed in such a way that they provide exactly the same structure of an FIR filter. And a system is made suited for implementation of correlation and it made it best method.

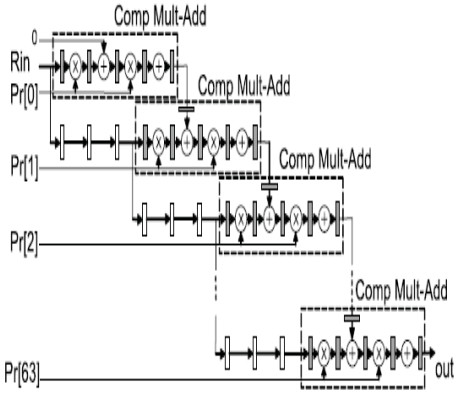

Fig. 4. Pipeline structure of correlator using multipliers

As shown in fig 2 multipliers in transpose direct form is the our first design using non –pipeling structure . with 64 coefficients, *Pr* corresponding to the 64 complex conjugated values of samples in the preamble. The output of the FIR filter in
transpose direct form can be expressed as

Output = $Pr[63]Ri + z{-}1(Pr[62]Ri + z{-}1(Pr[61]Ri + \cdots + z{-}1(Pr[0]Ri) \cdots))$. (1)

The coefficients are precomputed according to the IEEE 802.16d standard. As shown in fig 3 ,the second design is complex multiply –adds in a five –stage pipeline desigining using three-stage internal pipelining. *Ri_Re* is the real part and *Ri_Im* is the imaginary part of recived sample *Pr_Re* and *Pr_Im* similarly represent the complex conjugation ofknown preamble. The pipeline registers for the *Pr_Re*, *Pr_Im* are eliminated because they are considered to be of constant value. *Re* and *Im* are the real and imaginary parts of the previous multiply-add,
MAn−1. The output of these complex multiply-adds can be expressed
as

Output = $Ri\ Pr\ z{-}5 + z{-}4\ MAn{-}1$. (2)

The pipeline structure of the correlator is shown by fig 4. To handle received sample additional pipeline
register are required. Which are used to improve the performance,
The output of the pipelined correlator is

Output = $Pr[63]Ri(z{-}3)63z{-}5 + z{-}4 \times (Pr[62]Ri(z{-}3)62z{-}5 + z{-}4(Pr[61]Ri(z{-}3)61z{-}5 + \cdots + z{-}4(Pr[0]Ri\ z{-}5) \cdots))$

$= (z{-}3)63z{-}5\ (Pr[63]Ri + z{-}1(Pr[62]Ri + \cdots + z{-}1(Pr[0]Ri) \cdots))$. (3)

B. Design of Multiplierbased Correlator

In multiplier based design multiplication is done by using coefficients. It is considered that multiplierless correlation is more efficient, but as per the embedded hard multipliers in modern FPGAs multiplier based design is more favorable .Multiplier based system also provide synchronization accuracy . With the quantizations of 1, 0.5, 0.25, and 0.125 the coefficient sets are found by quantizing the 64 normalized preamble samples. Fig 5 shows the proposed structure for multiplier based correlators. Which is based on the transpose-direct form

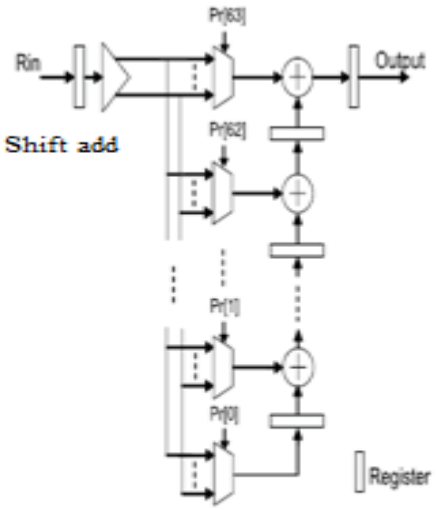

Fig. 5. Structure of multiplier based correlators

In which multipliers are used to multiply input samples by coefficients, Instead of actual multiplication we are using shif_add block and multiplier for the similar operation.The values for the quantized coefficient set are the different than the values of shift_add block, multiplexers and Pr[n]. As per the degree of quantization which is applied ,The shift_add blocks perform shift and add on the received samples. Without using 64 separate shift_add blocks we are using common shift add block to optimize resources in the case of small numbers of bit quantization . All possible values for 64 coefficients are calculated by using common shift add block. To generate the correlator output we select the corresponding values from shit add and we select values by using multiplexers. Which is based on the expressed coefficients $Pr[n]$ that are pre calculated on the basis of quantizing the 64 preamble samples.

Because of the constant values of the Pr[n] if we have synthesized the design the multiplexer is optimized as hard wired logic and the preamble cannot be changed. A real multiplexer used To support different OFDM preambles, instead of hard-wired logic, and the *Pr*[*n*] could be stored in a register. As result of this system provide more flexible solution and increased resource utilization.

C. Implementation Results

By using Xilinx ISE 13.2, targeting Xilinx Virtex-6 (V6) and Spartan-6 (S6) devices the design were synthesized and completely implemented. The results of implementation are reported in terms of the number of flip flops, 4 input LUTs ,occupied slices and their utilization are summarized in Table I.

As per the implementation result table implies that multiplier based correlator system is more efficient and useful as compare to the DSP based correlator . From the utilization table it is clear that as per the device utilization multiplier based system is more economical as it utilize very less device out of available. The natural availability of the flip flops are the 49,152 out of which the system used only 20% that is 10,224.Like wise

the flip flops system also enjoy the only 20% occupied slices. Not only flip flops but also the

TABLE I

Device Utilization Summary			
Logic Utilization	Used	Available	Utilization
Number of Slice Flip Flops	10,224	49,152	20%
Number of 4 input LUTs	4,100	49,152	8%
Number of occupied Slices	5,151	24,576	20%
Number of Slices containing only related logic	5,151	5,151	100%
Number of Slices containing unrelated logic	0	5,151	0%
Total Number of 4 input LUTs	4,100	49,152	8%
Number of bonded IOBs	50	640	7%
Number of BUFG/BUFGCTRLs	1	32	3%
Number used as BUFGs	1		
Average Fanout of Non-Clock Nets	2.39		

LUTs (Look up table) have the minimum utilization rather than it LUTs used only 8% of available device. From the above it is clear that multiplier based design utilize very less quantity of available device, along with that one more imp advantage is that the system used all slices containing related logic. So there is no wastage of circuitry . Due to which design become more efficient and cost free. In our system the utilization of slices containing unrelated logic is 0% which conclude that system does not involved in use less slices which make device more efficient and fast. New design has one more important advantage is that system used only one BUFGs that is Global clock buffer so percentage utilization is only 3%

III. SIMULATIONS AND CONCLUSION

Fig 6 pipeline correlateator simulation

Fig 7 Multiplier based correlator

The fig 6 and fig 7 has the simulation result of the low power synchronization result using VHDL . Here we are using the multiplier based system , instead of DSP slices.fig 6 shows the simulation of the pipeline correlator in which we are going to implement correlator using multiplier in the pipeline maner .And in figure 7 we have implement the correlator using multiplier which are design in a such a way that the system become universal and we can implement it on any FPGA system for the low power synchronization for the OFDM system. The multiplier based system on Virtex-6 FPGA has ideal resources for synchronizers to implement correlation . For synchronization for IEEE 802.16 OFDM system we have design multiplier based correlator for better performance. To obtained the higher clock speed we have used the pipelined correlator design. There is shortage of DSP slices on low-power low-cost devices such as the Xilinx Spartan-6,hence we use multiplier based system for low power implementation for such a devices. One more advantage of multiplier based system is as mention above the system is universal so it can be implement on any FPGA system.

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