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Pseudo Chaotic Sequence Generator based DS-SS Communication System using FPGA

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Abstract –
Spread spectrum (SS) technology is a data transfer technique designed to overcome the interference problems associated with narrow-band very high frequency and ultra high frequency Data transfer systems. Spread spectrum communication is used to reduce jamming of communication signal and provides a highly secure communication. In this paper we specifies the Field Programmable Gate Array (FPGA) implementation of a baseband spread spectrum communication system using pseudo-chaotic sequences (PCS) for spreading digital data.The sequence generator and the DS-SS (Direct Sequence Spread Spectrum) for a single user is implemented in FPGA as a prototype. The generated pseudo-chaotic sequences are investigated for autocorrelation, cross correlation and balance properties. The Bit error rate (BER) performance of the system is evaluated in multi-user environment under AWGN and reveal that the DS-SS system using pseudo-chaotic sequences as spreading sequences significantly outperforms the conventional PN sequences.
Keywords— digital communication, spread spectrum, pseudonoise,chaos, chaotic sequence generator.

I. INTRODUCTION

Spread Spectrum (SS) has been defined as a means of transmission in which the signal occupies bandwidth much in excess of the minimum necessary to send the information, the band spread is accomplished by utilizing a code which is independent of the data and a synchronized reception with the code at the receiver is used for de-spreading and subsequent data recovery. The SS Communications are mostly used today for Military, Industrial, Avionics, Scientific, and Civil uses. The merits of using SS include the following:

Low power spectral density.
As the signal is spread over a large frequency-band, the Power Spectral Density is getting very low, so other communications systems do not suffer from thiskind of communications. However the Gaussian Noise level is increasing.

The ability to utilize the Satellite payload channels, which is achievable as the transmitted signal is spread in such a way that it become noise like and thus would not interfere with the payload traffic. Interference limited operation. Security due to unknown random codes. As the applied codes are in principle unknown to a hostile user. This means that it is not easy to possible to detect the message of another user. Applying spread spectrum implies the reduction of multipath effects. Random access possibilities. As users can start their transmission at any arbitrary time.

Better anti-jam performance. The cost paid is the need of a larger bandwidth which already present due to the usage of the existing communication channels and the need for good synchronization at the receiver to detect the reception of the signal.

Spread spectrum techniques for digital communication were originally developed for military applications because of their high security and their susceptibility to interference from other interceptors[4]. Now a day spread spectrum techniques are being used in variety of commercial applications such as mobile and wireless communication. In order to spread the bandwidth of the transmitting signals, the binary pseudo-noise

(PN) sequences have been used extensively in spread spectrum (SS) communication systems. One of the most commonly used PN sequences in DS-SS is maximal length sequences (m-sequences)[5] . The

length of m-sequences depends on the number of shift registers. Good correlation properties can be achieved with m-sequences. The ability to predict future sequence is nevertheless possible though difficult. Therefore transmission is not completely secured[7].The number of sequences generated by Linear Feedback Shift Registers (LFSR) may be insufficient for wideband DS-SS with a very large number of users. In addition, LFSR techniques provide limited flexibility in incorporating security into multiple user systems [6].The use of chaotic sequences as spreading sequences has been proposed in the literature because of its sensitivity to initial conditions and has characteristics similar to random noise. However reliable electronic hardware implementations of chaos-based PN sequence generators based on recursion of maps realized by piecewise linear analogue functions and output quantization

have not been possible due to manufacturing process variations among different integrated circuit production lots, transistor mismatches and electronic noise[6]. The pseudochaotic sequence generator presented in this paper is the modified version of the generator presented in[6]. The pseudo-chaotic sequence generators presented in and are in the class of Non Linear Feedback Shift Registers (NLFSR).Many authors have shown that chaotic spreading sequence can

be used as an inexpensive alternative to the LFSR sequences such as m-sequences and Gold sequences[10]. The remaining sections of this paper are organized as follows. In section 3 the generation of pseudo- chaotic sequences and their suitability in multiple access is described. The FPGA implementation of DS-SS system along with PCS generator is presented in section 4. In section 5 a detailed discussion of the performance of the proposed scheme and some experimental results are presented. The paper is concluded with some remarks in section 7.

II. DIRECT SEQUENCE SPREAD SPECTRUM TECHNIQUE:

There are many types of spread spectrum techniques as:Direct sequence (DS), frequency hopping, time hopping and hybrid system. Direct sequence (Fig 1) contrasts with the other spread spectrum process, in which a broad slice of the bandwidth spectrum is divided into many possible broadcast frequencies. In general, frequency-hopping devices use less power and are cheaper, but the performance of DS-CDMA systems is usually more reliable. Thus, in this paper we will deal only with direct sequence spread spectrum method. In Direct Sequence-Spread Spectrum the base-band waveform is XOR by the PCS sequence in order to spread the signal. After spreading, the signal is modulated and transmitted.

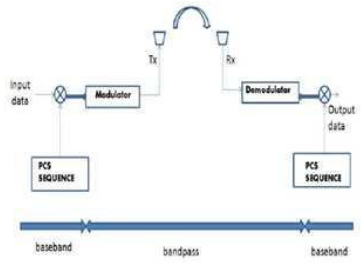

Fig1: DSSS Block Diagram

The bandwidth expansion factor - also called the Processing Gain (K) -, can be defined as the ratio between the transmitted spread spectrum signal bandwidth (B) and the bandwidth of the original data sequence (B message) where the Processing Gain is nearly the ratio of the spread bandwidth to the information rate R (bits/s) and it is much greater than unity.

$$K = \frac{B}{B_{message}} \approx \frac{B}{R}$$

Spread Spectrum transmitters use similar transmits power levels to narrow band transmitters. Because Spread Spectrum signals are so wide, they transmit at a much lower spectral power density, than narrowband transmitters. Spread and narrow band signals can occupy the same band, with little or no interference. Interference rejection capability arises from low mutual correlation between the desired signal and the interfering signal ensured by the codes.

This capability is the main reason for all the interest in Spread Spectrum today. The equation that represents this DS-SS signal is shown in equation.

$$Sss = \sqrt{(2Es/Ts)}[m(t) \otimes p(t)] \cos(2\pi fct + \theta)$$

Where:
m(t) is the data sequence,
Ts is duration of data symbol.
p(t) is the PCS spreading sequence, fc is the carrier frequency,
θ is the carrier phase angle at t=0

III. GENERATION OF PSEUDO-CHAOTIC SEQUENCES:

Pseudo noise (PN) is defined as a coded sequence of 1's and 0's with certain auto-correlation properties [4]. The system of sequences used in spread spectrum communication are usually periodic in that a

sequence of 1's and 0's repeats itself exactly with a known period. The m-sequence represents a commonly used periodic PN sequence. Such sequences are long periods and require simple instrumentation in the form of a LFSR. Indeed, they possess the longest possible period for this method of generation. A shift register of length m consists of m flip-flops (two state memory stages) regulated by a single timing clock. At each pulse of the clock, the state of each flip-flop is shifted to the next one down the line that is ext flip-flop. In a feedback shift register of the linear type, the feedback function is obtained using modulo-2 addition (XORed) of the outputs of the various flips-flops. The generated m-sequence is always periodic with a period of

N=2_-1 where m indicate is the length of the shift register.

The highlight of this paper is the PCS Generator, which generates a pseudo-chaotic PN sequence with good crosscorrelation and auto-correlation properties that is well suited

for DS-SS system. Because of long periodicity, it provides very high security and is capable of handling many users. It consists of a cascade of four basic cells with two 8-bit programmable registers each. The output of the last cell i.e. each bit of the last cell output are XORed together to obtain pseudo-chaotic sequence and also this bit is fed back to the system to maintain nonlinearity that's we called as(NLFSR).By increasing number of cells and size of the registers, we can increase the number of users and period of the sequence.Since the number of implementation possibilities are very high due to just changing only initial condition programmability, this new system of sequence is inherently more difficult to intercept[6].

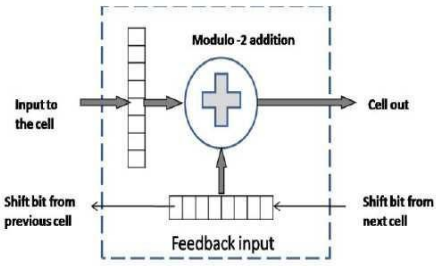

Fig.2.Basic NLFSR cell structure

Fig.2 shows a basic NLFSR cell, each cell consists of two 8-bit registers and a XOR function block. Initial conditions are set to both the registers. The contents of the two registers are XORed(modulo-2 addition) to obtain 8- bit output Cell out, which is used as input to the upper register of the next NLFSR cell. The contents of the two registers are altered for the next iterations by shifting the contents of the lower register towards left. The most significant bit that shifts out of the register is loaded into the least significant bit place of the feedback register of the previous cell. Similarly, the shifted bit from the next cell is moved into most significant bit place of the lower (feedback) register. The contents of the upper register are replaced by the 8- generator used in this paper consists of four such cells connected in series as shown in Fig.3.

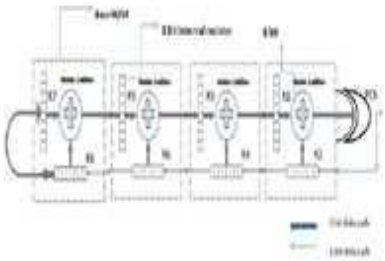

Fig.3.pseudo chaotic sequence generator

An exhaustive search was conducted to characterize the length of the sequences generated by the pseudo-chaotic finite state machines. In particular, the four stage cascaded structure in Fig. 2 was studied. The PCS generator contains eight 8-bit registers. These registers provide a total of 64 binary memory elements. Therefore, the PCS generator can be viewed as a sequential state machine with at most 264 possible states. The initial values to these registers can be initialized individually.

IV. FPGA IMPLEMENTATION OF DS-SS SYSTEMALONG WITH PCS GENERATOR.

In this paper, we have replaced the conventional PN sequence by PCS (pseudo-chaotic sequence) for a DS-SS system. The block diagram of the implemented DS-SS system with transmitter and receiver, and inter connection between them is shown in Fig. In this fig. shows that channel is the only connection between transmitter and receiver; assuming clock has been synchronized and channel is ideal.

bit output of the previous cell. The PCS

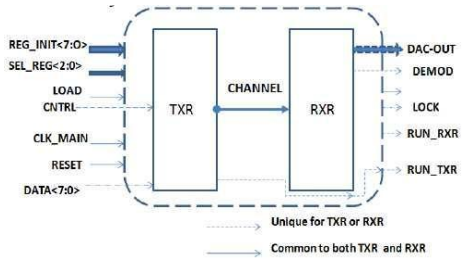

Fig.4.Block diagram of DS-SS with transmitter and receiver

A. TRANSMITTER.

In this DS-SS system, we spread the data bits using PCS sequence which are generated by using PCS generator as mentioned in section 3. To

generate PCS sequence, we need to initialize the 8 bit registers R1 to R8of PCS generator. To load eight registers of the PCS generator set load = 1 and using 3 pins of sel reg the corresponding registers R1 to R8 are selected. The 8 bit initial values to each of these 8 registers are loaded using 8 pin Reg init. After loading the initial values to all the 8 registers, Ready out pin gives an signal to the user. At the same time a signal ready is set to high which gives an indication to the control circuit that it can start its operation.

Initially before loading the initial values to the registers R1 to R8, the control circuit signals busy and done are not enabled i.e., busy = 1 & done = 0. As soon as ready = 1, then the signal busy = 0. The tracking and synchronization of the receiver can be done easily by sending first 8 bit data as "11111111". In that condition, the massage source sends a signal in the form of reload signal to the control circuit to indicate that it is ready to send the data. Once this happens the 8 bit data is sent parallely and stored in a buffer register of control circuit in the next clock cycle. After receiving the 8 bit data frame, the control circuit enables the PCS generator by setting the signal run = 1, also enables the multiplier by setting enable = 1 and indicates the buffer that it is busy by setting the signal busy = 1.

During this time the PCS generator starts generating the 32-bits of PCS sequence. The control circuit then transfers one bit at a time serially to the multiplier where it is multiplied by the 32-bits of generated PCS sequence resulting in a 32-bits of spread sequence and the same is transmitted.After the first data bit is spread by 32-bits of PCS sequence, the second data bit is received in the multiplier and is multiplied by the next 32-bits of the PCS sequence.

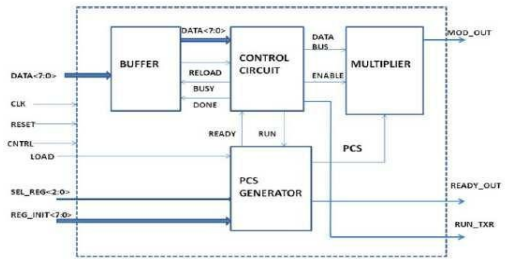

Fig. 5. Block diagram of transmitter

Hence the PCS generator generates a total of 256 bits to spread all the 8-bits of data.After transmitting all the 256 bits with respect to one frame of data i.e., 8-bits of data, the control circuit makes signal done =1 and busy = 0. At that time the control circuit is ready to accept next frame of 8-bits of data. In this way the operation of the transmitter repeats and maintain the gap between the two frames.

B**.** RECEIVER.

The internal block diagram of the receiver is shown in Fig(6) . consists of detector, control circuit, PCS generator and demodulator. The receiver mainly phase, the 8 bit registers R1 to R8 are again initialized with the same initial values used in the transmitter. This is indicated by setting ready = 1 by the PCS generator to the control circuit. During the training phase the control circuit keeps the signal ld = 1 and enable = 0 and run = 1. Now the detector is initialized with a training sequence i.e., the first 256 bits of the PCS sequence are loaded into the 8 lower registers, each with 32-bits of the detector.

In the detection phase, the control circuit resets ld = 0 and run = 0. During this phase the received data of 256 bits are loaded into the upper 8 registers of detector, each register with 32-bits and is compared with the bit pattern which is already stored in the lower 8 registers of the detector.

Upon reaching a certain threshold value, the detector sends a signal lock = 1 which is sent to the control circuit. The occurrence of the lock = 1 indicates the end of the detection phase and start of the dispreading phase.The control circuit now sets the signal enable = 1 and run = 1 by taking care on the frame gap durations previously considered during the transmission.

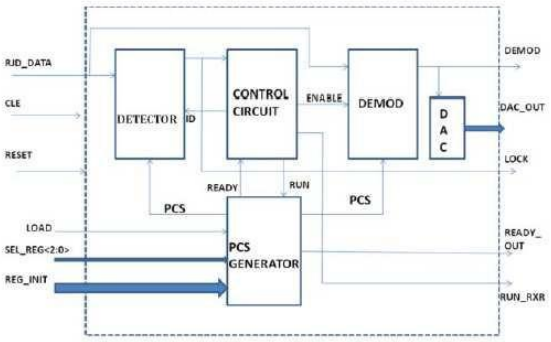

Fig.6. Block diagram of receiver

The control therefore shifts from the detector to the despreader where the incoming wideband data stream is multiplied by the sequence from the local PCS generator; the original narrow band data is obtained at the demod data pin and transfer to the DAC (digital to analog convertor).

C. DETECTOR.

The DS-SS system uses a technique called correlation for detection and synchronization of the system. The device used is known as correlator or detector. In this paper, we have used a modified version of conventional detector at the receiver to detect the signal from the transmitter and to achieve synchronization between the transmitter and receiver during the communication in DS-SS system that uses

chaotic sequence. The detection of signal from the intended transmitter at receiver and to achieve the synchronization between them is very important in DS-SS system specifically when the system uses pseudo-chaotic sequence.

When the control circuit of receiver sets ld = 1, the 32-bits of the PCS generator are loaded in to the Shift Register1 of 32-bit correlator whose simplified 8-bit version is shown in Fig.7. The detector consists of 8 such 32-bit correlators . Once all the 256 bits are loaded into Shift Register1 of eight 32-bit correlators, control circuit resets ld = 0, so that the received bits are started to load into the Shift Register2. As it receives each bit from channel, the detector multiplies each bit of shift register1 with the corresponding bits of shift register 2 and decides that the received bit is 1 else 0.

The cross-correlation and autocorrelation properties of the PCS sequences plays a very important role in avoiding the false triggering during the detection. The multiplication and summation takes place at higher clock rate, for that we can use single multiplier and summer to multiply and add all 32-bits of each correlator. This reduces requirement of hardware by the detector significantly.

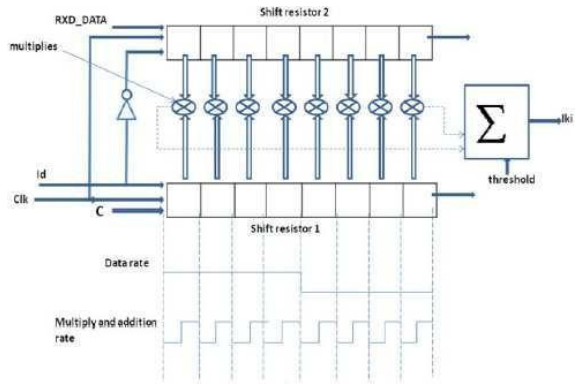

Fig.7 Bit correlator

V. PERFORMANCE OF THE PROPOSED SCHEME AND EXPERIMENTAL RESULTS.

In this paper the prototype was designed and implemented for a spreading sequence of length 32 bits because of hardware limitations. For practical applications the spreading sequence length can be increased to 1024 bits. Hence the performance of the system can be enhanced by increasing the length of the spreading sequence. Also in the detector, the number of bits considered for synchronizing transmitter and the receiver is limited to 64 bits for ideal Laboratory conditions. For real-time applications, the synchronizing bits can be further increased according to the performance requirements.

The maximum off-peak autocorrelation value and maximum cross correlation value decreases as the sequence length increases. Hence increasing the

VI. RESULTS.

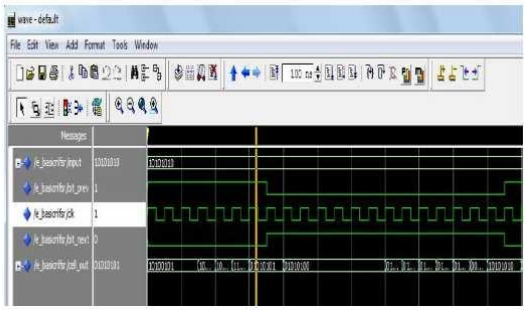

Fig.8 Output of basic NLFSR cell structure(shown in fig 2).

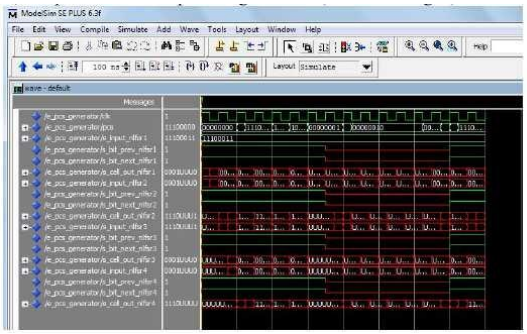

Fig.9 output of PCS sequence generator(shown in fig 3).

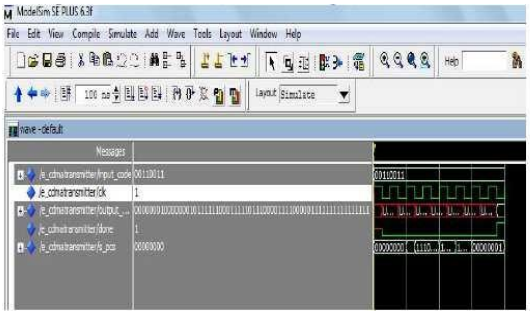

Fig.10 output of transmitter(shown in fig 5)

Fig.11 output of receiver (shown in fig 6)

VII. CONCLUSION.

The PCS generator discussed in this paper is based on the model discussed in [6]. The initial conditions of the PCS sequence generators can be randomly selected to produce pseudo-chaotic sequence with good correlation properties upon exhaustive comparison to be distinct sequences rather than phases of the same sequence. The family of pseudochaotic PN sequences proved good correlation properties than conventional m-sequences and hence it can be useful for DSSS.Pseudo-chaotic sequence generation with its robust digital implementation avoids many difficulties associated with analog chaotic circuits. The large set of system parameters (initial conditions and internal configuration of cells and generators) and the non-linear nature of the feedback generation circuitry lead to potential applications for programmable secure communication systems. Tests will have shown that simply using random selections of initial conditions can provide pseudo-chaotic PN sequences that are relatively long with good correlation properties. Based on these results it is worth noting that the sequences based on quantized maps derive many of their statistical properties from the specific architectures used to implement them. This flexibility provides an additional level of security on top of the inherent low-probability of intercept characteristics of PN sequences due to the difficulty of identify the underlying structure. Therefore the number of implementation possibilities is very high due to initial condition programmability, can be made software controlled and this new system of sequences is inherently more difficult to detect.

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