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A Survey on Design of Pipelined Single Precision Floating Point Multiplier Based On Vedic Mathematic Technique

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ABSTRACT
A typical processor devotes a considerable amount of processing time in performing arithmetic operations, particularly multiplication operations. Since, multiplication dominates the execution time of most DSP algorithms therefore high-speed multiplier is much desired .This paper presents a survey of different techniques for multiplication employing Vedic Mathematics and IEEE 754 Floating point format to improve speed of operation .

Keywords: Vedic Mathematics, Urdhva-triyakbhyam sutra, Floating Point multiplier,

I. INTRODUCTION

Multipliers are essential in implementation of systems realizing many important functions such as fast fourier transforms and multiply accumulate. Since, multiplication dominates the execution time of most DSP algorithms therefore high-speed multiplier is much desired. With an ever-increasing quest for greater computing power on battery-operated mobile devices, design emphasis has shifted from optimizing conventional delay time area size to minimizing power dissipation while still maintaining the high performance . The low power and high speed multipliers can be implemented with different logic style.

II. FLOATING POINT NUMBERS

The term floating point is derived from the fact that there is no fixed number of digits before and after the decimal point, that is, the decimal point can float. Floating point arithmetic is useful in applications where a large dynamic range is required maintaining the precision. Floating point numbers are one possible way of representing real numbers in binary format; the IEEE 754 standard presents two different floating point formats, Binary interchange format and Decimal interchange format. Multiplying floating point numbers is a critical requirement for DSP applications involving large dynamic range. Here we will focus on single precision format.

The Single precision format consist of 32 bits .The format is composed of 3 fields; Sign, Exponent and Mantissa. In case of Single, the Mantissa is represented in 23 bits and 1bit is added to the MSB for normalization, Exponent is represented in 8 bits which is biased to 127.The MSB is reserved for sign representation. When the sign bit is 1 that means the number is negative and when the sign bit is 0 that means the number is positive.

Fig1. Single precision format

III. VEDIC MATHEMATICS

The word "Vedic" is derived from the word "Veda" which means knowledge. The use of Vedic mathematics lies in the fact that it reduces the typical calculations in conventional mathematics to very simple ones. This is so because the Vedic formulae are proved to be based on the natural principles on which the human mind works . Vedic Mathematics is a methodology of arithmetic rules that allow more efficient fast implementation. This is a very interesting field and presents some effective algorithms. Vedic mathematics is mainly based on 16 Sutras (Or aphorisms) dealing with various branches of mathematics.

The ancient Vedic mathematics Sutra (formula) called Urdhva Tiryakbhyam (Vertically and Cross wise) Sutra which was traditionally used for decimal system in ancient India. This Sutra is shown to be a much more efficient multiplication algorithm than the

conventional counterparts. The research has also shown the effectiveness of this sutra to reduce the N×N multiplier structure. Urdhva Tiryakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. In this, the digits on the two ends of the line are multiplied and the result is added with the previous carry. When there are more lines in one step, all the results are added to the previous carry. The least significant digit of the number thus obtained acts as one of the result digits and the rest act as the carry for the next step .Initially the carry is taken to be as zero. Let's analyze 4x4 multiplications, say A3A2A1A0 and B3B2B1B0. Following are the output line for the multiplication result, S7S6S5S4S3S2S1S0. Let's divide A and B into two parts, say A3A2 & A1A0 for A and B3B2 & B1B0 for B. Using the Vedic multiplication technique, taking two bit at a time and using 2 bit multiplier block, we can have the following structure for multiplication.

A3A2 A1A0
X B3B2B1B0

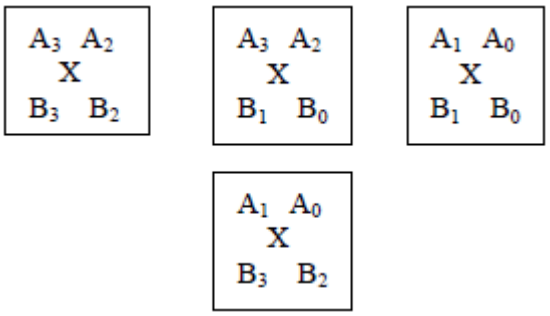

Fig 2. Block diagram presentation for 4x4 multiplications

So the final result of multiplication, which is of 8 bit, S7S6S5S4S3S2S1S0, can be interpreted as given below. The output of each multiplication is as given

A3A2
A3A2
A1A0
x B3B2 x B1B0 x B1 B0
--- --- ---
S33S32S31S30 S23S22S21S20 S13S12S11S10

A1 A0
x B3B2

S0S02S01S00

IV. LITERATURE SURVEY

Sumit Vaidya and Deepak Dandekar in 2010 made Delay-Power Performance Comparison Of Multipliers in VLSI circuit design. They made a comparative study among Array multiplier, Booth Multiplier and Wallace Tree multipliers which are standard approaches to have hardware implementation of binary multiplier which are suitable for VLSI implementation at CMOS level. Results shows that Booth Multiplier is superior in all respect like speed, delay, area, architectural complexity and power consumption. However Array Multiplier requires more power consumption and gives optimum number of components required, but delay for this multiplier is proved to be larger than Wallace Tree Multiplier. Hence for low power and for less delay requirement Booth's multiplier is suggested. FPGA implementation results shows that multiplier Nikhilam Sutra based on of Vedic mathematics for multiplication of binary numbers is faster than multipliers based on Array and Booth multiplier. It also proves that as the number of bits increases to N, where N can be any number, the delay time is greatly reduced in Vedic Multiplier as compared to other conventional multipliers. Vedic Multipliers has the advantages over other multipliers since it requires less power and regularity of structures. Author also proves that among the number of techniques for logic implementation at circuit level that improves the power dissipation, area and delay parameters in VLSI design, implementation of parallel Multiplier in Complementary Pass Transistor Logic (CPL) logic has significant improvement in power dissipation. However CPL requires more number of transistors to implement as compared to the CMOS. The Pass Transistor Logic (PTL) proved better over both the CMOS and CPL in terms of delay, power, speed and transistor count. The PTL outperforms the CMOS implementation in speed and great in power dissipation, with approximately same transistor count. When compared to CPL, PTL is faster and shows improvement in power and transistor count.[12]

Sumit Vaidya and Deepak Dandekar in 2011 proposed low power and high speed 8×8 Bit Vedic Multiplier. This paper presents a systematic design methodology for fast and delay efficient Vedic Multiplier based on the Vertical and Crosswise algorithm of Ancient Indian Vedic Mathematics. In this paper, general technique for N×N multiplication is proposed and implemented, which gives less delay for calculating the multiplication results for 8×8 Bit Vedic Multiplier. The multiplier cell of the adder is designed by using Pass Transistor (n-transistor), p-transistor used as cross coupled devices. Simulated

results for proposed 8×8 bit Vedic Multiplier circuit shows a great reduction in delay for 0.18 μm.[4]

S.Kokila, Ramadhurai.R2, L.Sarah in 2012 proposed method is 32x32 bit multiplication in terms of relatively high speed, low power, less area and less delay. They designed multiplier in VHDL, as its give effective utilization of structural method of modelling. Also, VHDL helps in the modular design where smaller block can be used to design the bigger one. For 32x32 bit multiplier, the architecture is decomposed in smaller 8x8 bit module. The simulation results showed that delay difference of vedic multiplier is very less compared to other multipliers. Thus it offers us method for hierarchical multiplier design. So the design complexity gets reduced for inputs of large no of bits and modularity gets increased [10].

P. Saha, A. Banerjee, A. Dandapat, P. Bhattacharyya in 2011 proposed a report on a 32×32 bit high speed low power multiplier design based on the formulas of Indian Vedic Mathematics. The implementation was done in Spice spectre and compared with the mostly used architecture like Wallace Tree Multiplier (WTM), Modified Booth Algorithm (MBA), Baugh Wooley Multiplier (BWM) and Row Bypassing and Parallel Architecture (RBPA).This novel architecture combines the advantages of the Vedic mathematics for multiplication which encounters the stages and partial product reduction. The architecture offered 29%, 31%, 35%, and 23% improvement in terms of propagation delay compared with Wallace WTM, MBA, BWM and (RBPA) based implementation respectively. Whereas the corresponding improvement in power is 17%, 26%, 29%, and 21% respectively compared with WTM, MBA, BWM and RBPA based architecture. [5]

Korra Tulasi Bai, J. E. N. Abhilash proposed a floating point multiplier in 2013. In this, author has designed 32x32 bit floating point multiplier based on Vedic Mathematics. The multiplier for the floating point numbers represented in IEEE 754 format can be divided in four different units:

- Mantissa Calculation Unit
- Exponent Calculation Unit
- Sign Calculation Unit
- Control Unit

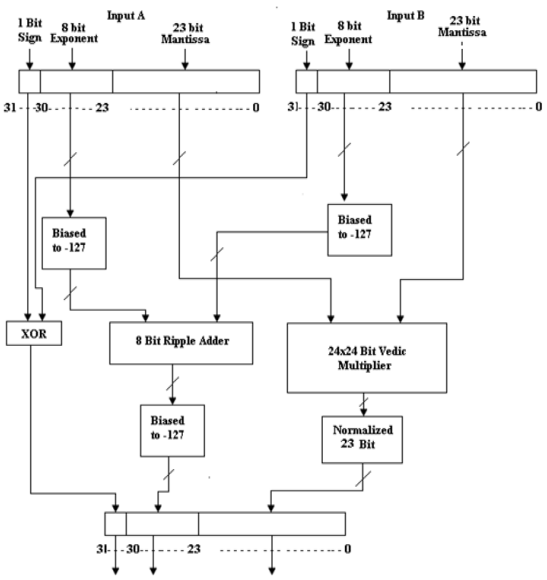

Fig 3. Architecture for Floating point Multiplier

Multiplication of two, 24 bit mantissa is done using the Vedic Multiplier. In this paper, the Exponent Calculation Unit is implemented using 8 BIT Ripple Carry Adder since ripple carry adder is easy to implement because of its simple layout as well as required low area . The Control Unit raises the flag when NaN, Infinity, zero, underflow and overflow cases are detected. Following algorithm is used for the multiplication purpose.[2]

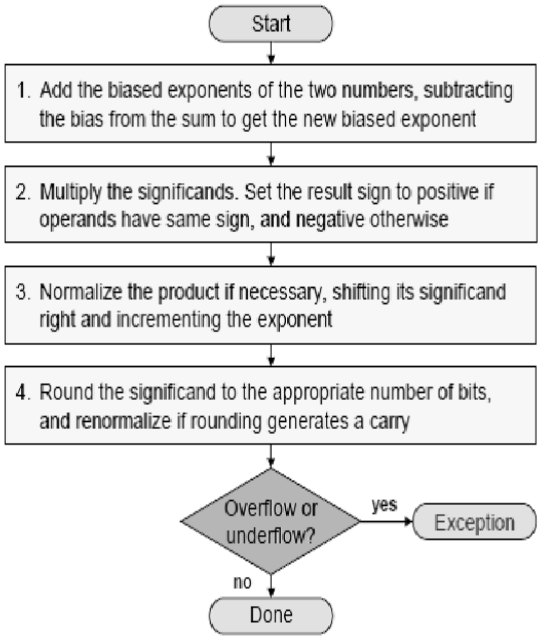

Fig 4. Algorithm for Floating point Multiplier

In 2006, Kavita Khare, R.P. Singh and Nilay Khare carried out Comparison of Pipelined IEEE-754 standard Floating Point Multiplier with Unpipelined Multiplier. Both Pipelined and Unpipelined multipliers are designed and analyzed and it is evidenced that pipelined multipliers are better in terms of device utilization, operating speed and power consumption. Author concluded that by increasing the number of pipelining stages the speed of operation can be effectively increased.[13]

Riya Saini and R.D.Daruwala in 2013 praposed implementation of Pipelined Double Precision Floating Point Multiplier This paper presents a fully parallel floating-point multiplier compliant with the IEEE 754 Standard for Floating-point Arithmetic. The proposed design offers low latency and high throughput. A comparison between simulated results and some previously reported implementations shows that this approach, in addition to the scalability feature, provides multipliers with significant improvements in area and speed. Thus it showed that pipelining is one of the popular methods to realize high performance computing platform. In pipelining technique multiple instruction executions are overlapped and the pipelined modules are independent of each other.

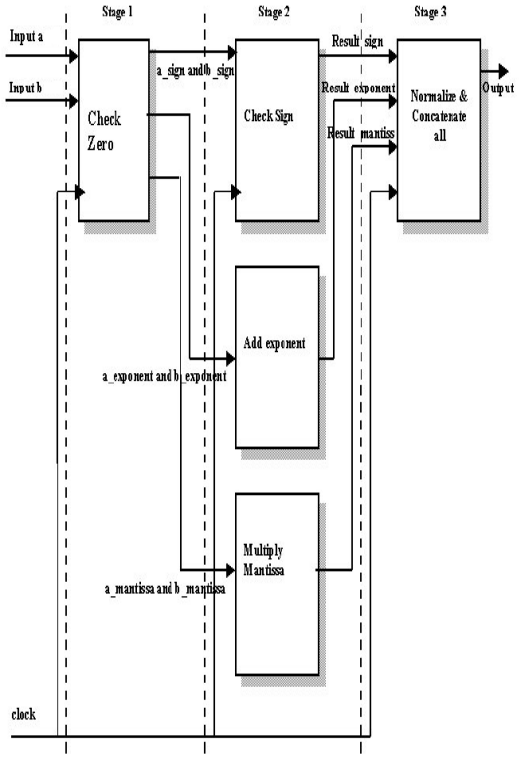

Fig 5. Architecture for pipelined Floating point Multiplier

With the help of pipelined architecture i.e. concurrent processing there will be less combinational delay which means faster response and better throughput with less latency as compared with sequential processing.[1]

V. PROPOSED WORK

If vedic mathematics technique is used for mantissa calculation in pipelined architecture of floating point multiplier, the speed of execution can be effectively increased with greater throughput. Thus proposed work is to implement pipelined single precision floating point multiplier using vedic mathematics.The proposed pipelined single precision floating point based on Vedic Mathematics is not implemented yet at ASIC design levels.

VI. PROPOSED METHODOLOGY

The proposed architecture can be implemented as follows:

1) VHDL implementation of 2x2 Vedic multiplier and its verification.
2) Implementing 32x32 Vedic Multiplier in VHDL using the designed components and its verification
3) Implementing 32x32 floating Multiplier in VHDL.
4) VHDL implementation and verification of 32x32-bit pipelined Multiplier.
5) Implementing 32x32 pipelined floating point Multiplier in VHDL using the designed components and its verification
6) Comparison and study of the results.

VII. CONCLUSION

Multiplying floating point numbers is a critical requirement for DSP applications involving large dynamic range. Proposed work will result in high performance pipelined floating point multiplier based on Vedic mathematics, which will meet the specifications like High Speed and Low Power Consumption

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