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Design and Optimization of Domino Logic Based ADC for Digital Synthesis

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Abstract
This paper proposes a 10 b 200 MS/s Domino logic based analog-to-digital convertor (ADC) for high-quality video systems By cascading many digital-like domino-logic cells whose propagation delay is influenced by an analog input voltage, a digital value is obtained at the end of the allowed ripple period by determining the number of cells that the ripple passed through. The sample-and-hold is simply a bootstrapped switch into a small sampling capacitor to minimize power consumption and delay of sample and hold circuit. The prototype ADC in a 0.18 μm CMOS technology demonstrates the measured differential nonlinearity and integral nonlinearity within 0.62 and 0.99 LSB, respectively. At 200 MS/s, the ADC shows a maximum SNDR of 52.8 dB and a maximum SFDR of 60.4 dB. The ADC with an active die area of 1.28 mm2 consumes 54.0 mW at 1.8 V.
Keywords— Analog-digital conversion, low power, scaling, synthesis.

I. INTRODUCTION

HIGH-DEFINITION televisions (HDTVs) offer a vastly improved quality compared with the existing signal standards such as National Television System Committee, Phase-Alternating Line, and Sequential Color with Memory. Two commonly employed HDTV systems, 720p and 1080i of the progressive and interlaced scanning types, respectively, ensure at least five times improvement of quality compared to the conventional analog approaches. Recently, with the increasing demand for high-quality imaging systems, the required specifications for the system analog front ends (AFEs) have become more and more strict and thus the analog-to-digital converter (ADC) is one of the most critical building blocks. The typical video signal chain of an HDTV system is illustrated in Fig. 1. The ADC in front of the main signal processor needs 8–10 effective number of bits while operating at a sampling rate exceeding 165 MS/s for low jitter, high image quality, and wide enough bandwidth. In addition, the ADCs in the video decoder require a 10 b resolution to digitize video analog inputs such as Pr, Y, and Pb into Cr, Y, and Cb. The video signal Y is a brightness portion while the Pr and Pb are color-difference portions of the signal. ADC applications requiring a high sampling rate of several hundred MS/s have been typically based on Flash, folding, sub-ranging, and pipeline architectures. Considering 10 b resolution and low power simultaneously with the high sampling rate, the pipeline architecture has been primarily employed [1]–[5].

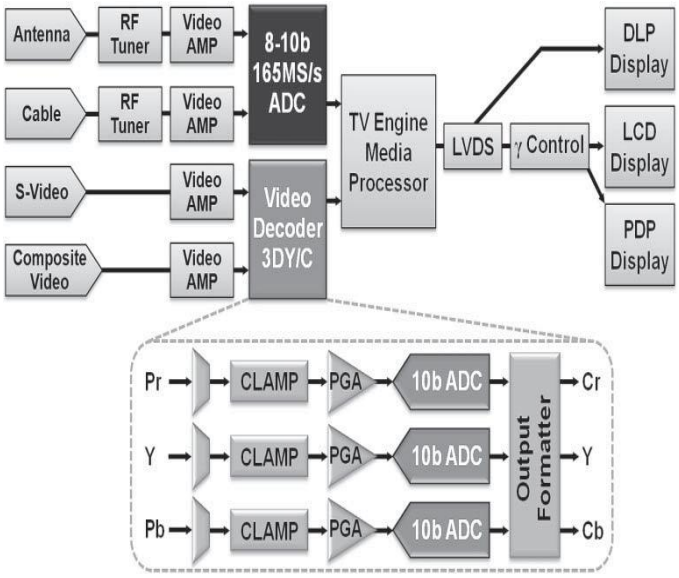


Fig. 1. Video signal chain of an HDTV system.

On the other hand, inventive calibration schemes in the digital domain have been proposed to reduce power consumption of high-performance ADCs; however, those schemes require additional circuits to remove nonlinear errors in the digital domain [6]. Another method to implement low power consumption with enhanced conversion speed is to employ multi-channel time-interleaved (T-I) techniques [7]. Unfortunately, the overall ADC performance based on T-I techniques tends to be degraded due to inherent mismatches between

parallel channels such as the gain, bandwidth, timing, and offset differences of amplifiers in each channel with the somewhat increased chip area.

This paper proposes a 10 b 200 MS/s Domino Logic ADC to improve the performance of conventional T-I ADCs. By cascading many digital-like domino-logic cells whose propagation delay is influenced by an analog input voltage, a digital value is obtained at the end of the allowed ripple period by determining the number of cells that the ripple passed through. The sample-and-hold is simply a bootstrapped switch into a small sampling capacitor. As each domino-logic cell passes the ripple, charge is kicked back onto the input capacitor, which creates a significant second harmonic. Distortion caused by even harmonics is canceled by implementing a pseudodifferential structure. The overall circuit implementation and operation scheme of the domino logic based ADC is described in Section III. The measured results of the ADC are summarized in Table I and compared in Table II and the conclusion is given in Section IV.

II. CIRCUIT IMPLEMENTATION

A. *Principle of Operation*

A domino-logic-based ADC is a cascade of several dynamic delay cells such as that in Figs. 1 and 2 to create a circuit, as depicted in Fig. 3. The basic operation is as follows: A clock Φis used to trigger the ADC such that, when Φ = 1 ($\overline{\Phi} = 0$), all of the domino cells are reset, and the input voltage is sampled with a sample-and-hold into node *V*in. The domino cells are reset through small nMOS and pMOS switches with inputs of Φ and $\overline{\Phi}$, respectively. This resets the internal nodes of all of the cells and creates a high-impedance state between input *V*in and the gate of pMOS *Mp*. After sampling,Φ = 0($\overline{\Phi} = 1$), and every domino cell is in a ready state with all of the transistors off and in a high-impedance state. The first cell in the chain is triggered by $\overline{\Phi}$, as shown in Fig. 4. This causes nMOS *Mn* to turn on and create a conduction path between *V*in and the gate of *Mp*. In this implementation, the sample-and-hold is a simple bootstrapped nMOS switch [9]; therefore, *V*in is not actively being driven. This causes charge sharing with the parasitic capacitance at the gate of *Mp* and the capacitance at node *V*in. If the voltage at *V*in is sufficiently low, the device*Mp* will turn on and trigger the next cell. The cells continue to trigger each other in series, and then, they are reset in parallel on $\overline{\Phi} = 1$. Digital outputs *D*0 through *Dn*, just before resetting, are a thermometer code that can be encoded into binary as the ADC result.

B. *Implementation Details*

Since the sampling rate of this ADC depends on the number of cells and the rate at which they can propagate the digital ripple, we want to design the cell to have as small of a delay as possible in order to achieve a high sampling rate. The critical transistors in the delay path are *Mn* and *Mp*, whereas the reset switches and the digital buffer are less critical and only add unwanted parasitic capacitance to the internal nodes of the domino cell. Therefore, the reset transistors are minimum sized, and the critical transistors are slightly larger. Increasing the sizes of *Mn* and *Mp* will also add parasitic capacitance that needs to be charged and discharged during operation. As this adds to power consumption, our design uses device widths for *Mn* and *Mp* that are just below twice the minimum for the process.

Fig. 2 shows that the gate of the device *Mp* is reset to positive supply *VDD*. This means that, when *Mn* is turned on, enough charge must be shared with *V*in in order to drop the gate voltage of *Mp* to *VDD* − *V*TH, where *V*TH is the threshold voltage for a pMOS before *Mp* starts to turn on *Mn* of the next domino cell. This takes a certain amount of time. By adding a diode connected device in series with the pMOS reset switch (see Fig. 3), the gate of *Mp* will be reset to near *VDD* − *V*TH instead. This reduces the amount of charge that needs to be moved from the gate of *Mp* and, ultimately, the amount of time before *Mp* starts to turn on *Mn*. This would be a dangerous scenario, with *Mp* right at the tipping point of triggering the next cell. This could prematurely start a second "false" ripple further down the chain before the "true" ripple ever reached the cell. However, when the pMOS reset switch closes, there is enough charge injection that it guarantees that *Mp* will be off. This allows the design to operate at a higher speed without increasing power consumption by eliminating this "waste voltage."

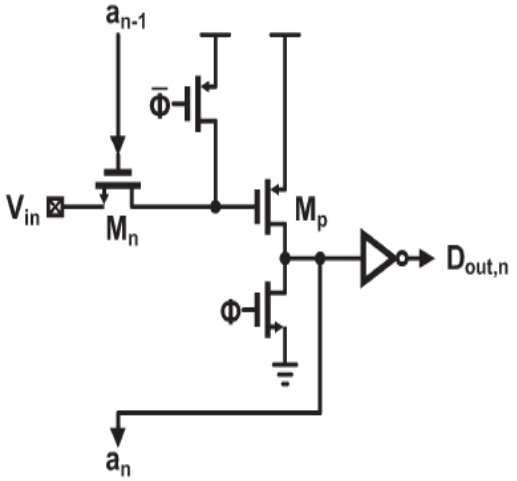


Fig. 2. Single "domino" cell. Input *V*in is sampled when Φ = 1 (i.e., $\overline{\Phi}$ =

0) while the cell is reset. On the transition to Φ = 0, the first domino cell is triggered such that *an*−1 = 1, which causes *an* = 1 after some short delay that is dependent on input *V*in. This transition continues to propagate through the chain until the evaluation period is over, and once more,Φ = 1.

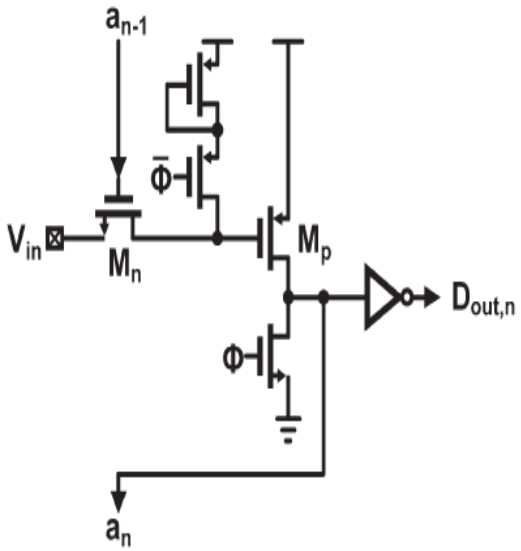


Fig. 3. Single "domino" cell with a shorter delay. The diode-connected device

causes the gate of pMOS*Mp* to be reset to a voltage lower than supply voltage *VDD* since there is a *V*TH voltage drop across the diode. By presetting the gate of*Mp* close to its threshold, the device is on the verge of tripping. Charge injection from the pMOS connected to $\overline{\Phi}$ raises the voltage slightly so that the cell does not trip early.

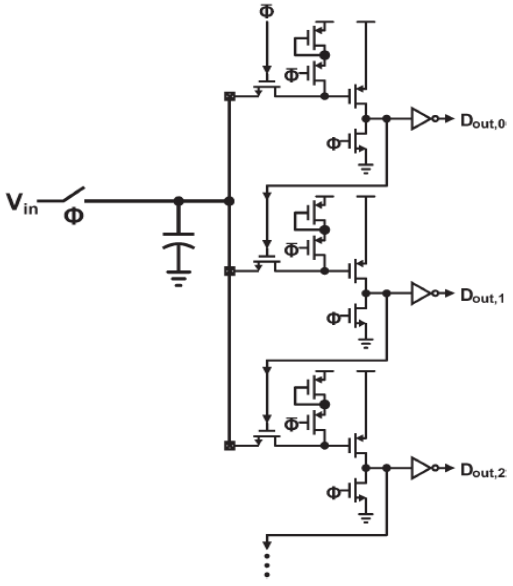


Fig. 4. This is an example of how multiple domino delay cells are combined

to form an ADC. DuringΦ = 1, the input is sampled onto the input capacitance while all of the domino cells are reset. WhenΦ = 0, all of the cells are ready to trigger, and the first cell (designated by its output, i.e., *D*out,0) is automatically triggered since the gate of its nMOS is tied to $\overline{\Phi}$ = 1. This starts a chain reaction as the cells begin to trigger in series until the end of the evaluation time. The number of cells that the trigger propagates through is related to the input.

III. MEASURMENT RESULT

The proposed 10 b 200 MS/s ADC is implemented in a 0.18 μm Technology. The measured differential nonlinearity (DNL) and integral nonlinearity (INL) are within 0.62 and 0.99 LSB, respectively, as illustrated in Fig. 5.

The typical FFT spectrum of the ADC measured with an input frequency 4 MHz at 200 MS/s is plotted in Fig. 6. The measured dynamic performance of the ADC is summarized in Fig. 13. The signal-to-noise-and-distortion ratio (SNDR) and spurious-free dynamic range (SFDR) in Fig. 7 are measured at different sampling rates from 20 to 200 MS/s with an input frequency of 4 MHz. The measured SNDR and SFDR are maintained over 52.8 and 60.4 dB up to 200 MS/s. The dynamic performance of the prototype ADC measured with increasing input frequencies at a sampling rate of 200 MS/s is illustrated in Fig. 8. the SFDR and SNDR performances are degraded due to the sampling time mismatch. However, using the input sampling scheme with a 50% duty cycle, the SNDR and SFDR at the Nyquist input frequency are measured to be 49.5 and 57.2 dB, respectively. The prototype ADC with the proposed input sampling scheme shows the considerably improved dynamic performance compared to the ADC based on the conventional input sampling scheme.

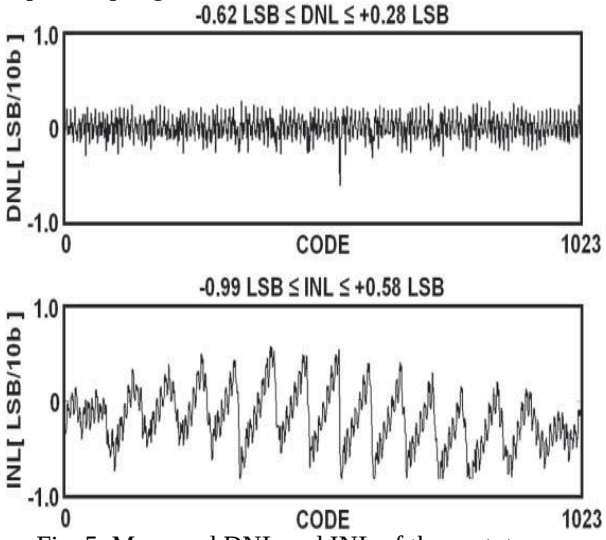


Fig. 5. Measured DNL and INL of the prototype ADC.

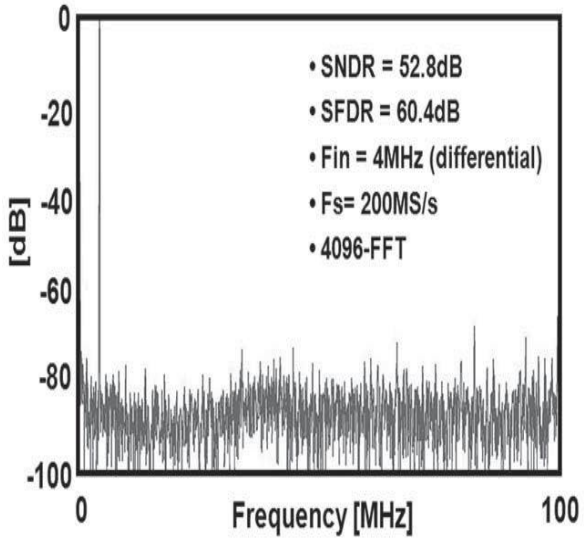


Fig. 6. Measured FFT spectrum of the proposed ADC.

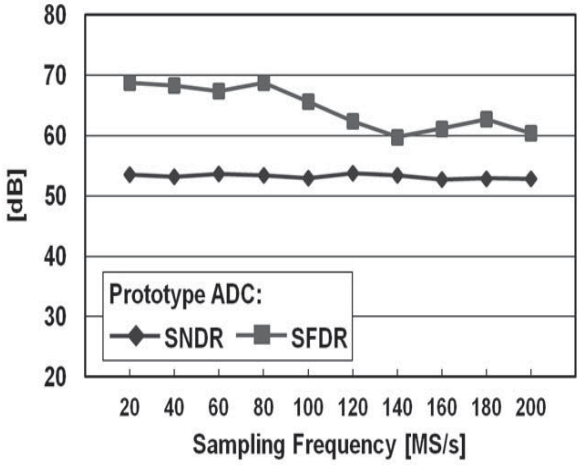


Fig. 7. Measured SFDR and SNDR of the ADC depending on fs.

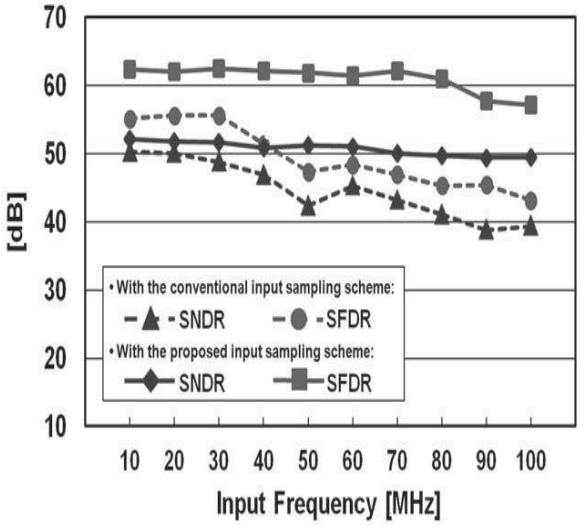
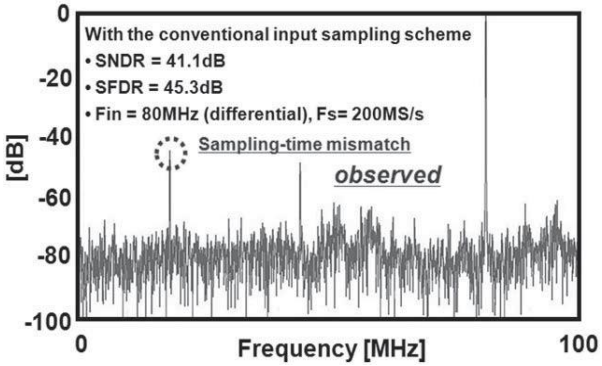


Fig. 8. Measured SFDR and SNDR of the ADC depending on a fin at 200 MS/s.

The FFT spectrum of the conventional input sampling scheme is compared to the proposed input sampling scheme, as shown in Fig. 9(a) and (b). The harmonic component at [fs/2 - fin], indicated with the dotted circle, is mostly generated by the sampling-time mismatch of each channel [12].The sampling-time mismatch effect of the conventional ADC is improved greatly in the proposed ADC, as observed in Fig. 9(a) and (b).



(a)

The performance of the prototype ADC is summarized in Table I. The performance of the ADC is compared with the up-to-date reported various CMOS ADCs at a 10 b resolution and a sampling rate exceeding 200 MS/s, as shown in Table II. The figure of merit (FoM), defined as (2), of the prototype ADC is 1.11 pJ/conversion-step, including the power consumption of the on-chip reference generator. Although the prototype ADC is implemented in a 0.18 μm CMOS process, it shows somewhat better power efficiency than the ADCs in deep sub-micron technologies:

$$FoM = Power/(2^{ENOB} \times 2ERBW)$$

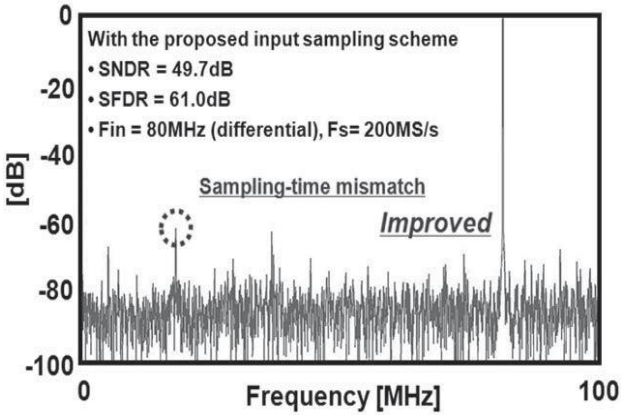


Fig. 9. FFT spectrum of the ADC measured with a fin of 80 MHz based on (a) conventional and (b) proposed input sampling schemes.

TABLE:I
PERFORMANCE SUMMARY OF THE DOMINO LOGIC BASED ADC

Resolution	10 bits
Conversion Rate	200 MS/s
Process	0.18 μm
Input Range	1.2 Vp-p (Differential)
Max.DNL/Max.INL	0.62 LSB/0.99 LSB
SNDR	52.8 dB (@*f*in = 4 MHz)
SFDR	60.4 dB (@*f*in = 4 MHz)
ADC Power Consumption	54.0 mW@1.8V
Die Area	1.28 mm2 (= 1.16 mm × 1.10 mm)

TABLE: II
PERFORMANCE COMPARISON OF RECENTLY REPORTED 10 b ADCS AT SAMPLING RATE HIGHER THAN 200 MS/S

	Speed (MS/s)	Supply (V)	Power (mW)	Area (mm2)	DNL/INL (LSB)	On-Chip I/V Ref.	Process (Technology)	FoM (pJ/Conv.)
This Work	*200*	*1.8*	*54.0*	*1.28*	*0.6/1.0*	*O*	*0.18 μm*	*1.11*
[8]	*200*	1.0	5.4	0.19	0.4/1.4	*O*	65 nm	0.06
[1]	*200*	1.2	104.0	4.90	0.6/0.8	*O*	0.13 μm	2.08
[9]	*200*	1.8	128.0	0.79	0.6/1.1	X	0.18 μm	-
[10]	204	1.0	9.2	0.22	0.7/0.9	*O*	65 nm	0.16
[4]	205	1.0	111.0	1.00	0.5/0.5	*O*	90 nm	1.74
[5]	205	1.2	92.5	0.52	0.2/0.6	X	0.13 μm	0.38
[11]	210	1.2	52.0	0.38	0.6/1.4	X	0.13 μm	0.80

IV. CONCLUSIONS

The domino logic based ADC implemented in a 0.18 μm CMOS technology occupied an active area of 1.28 mm2 and the measured DNL and INL were within 0.62 and 0.99 LSB, respectively. At 200 MS/s, the prototype ADC demonstrates a maximum measured SNDR of 52.8 dB and a maximum SFDR of 60.4 dB, consuming 54.0 mW at a 1.8 V supply voltage.

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