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Design and Implementation Power Optimizer Using Quaternary Logic

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Abstract
Implementation of quaternary logic is been proposed in terms of flip-flops performed with higher speed, considerable power optimization and precise organized processing is obtained in CMOS based arrangements of flip-flop such that scaling of values preamble with single digit based quaternary addition. Energy efficiency in VLSI based processor is necessary and been performed in terms of quaternary flip-flop. There is an optimization of power with increase of threshold voltage values in terms of its redundancy of bits. Design of quaternary flip-flop based optimization and quantization of Micro-Core based SIMD processor to achieve minimum rescaled value of resolution in terms of power optimization. This estimation of quaternary flip-flop based optimized values and enhanced data-transfer resulting in higher speed with power reduced to 0.675µW CMOS simulation in corresponding to its CMOS based design implementation.

Keywords—CMOS, power optimization, preamble, VLSI, SIMD, Micro-Core.

I. INTRODUCTION

Small yet circuit driving capability high, the rescaled combination of multiple-valued current-mode circuitry and differential-pair circuitry enables to implement energy-efficient circuits.

II. PROBLEM DEFINITION

As is considered to reduce the delay for the precision in processing of SIMD based processor it is required for Vertical (V-Channel) and Horizontal (H-Channel) [2] optimization with power optimization and increase in speed with respect to gates for various quaternary states. Providing low power with increased threshold voltage V_T as in terms V_T >> P optimized (reduced).

III. PROBLEM ANALYSIS

There is a consideration of sates in terms of values having a symmetrical value in terms of its transition from absolute low< medium low< medium high< absolute high.

Power dissipation in CMOS VLSI chips has been getting a serious problem in recent nanoscaling regime. Power density in VLSI chips is increased by scaling k0.7, where k (> 1) is a device scaled value, causing a doubling of the power dissipation every 6.5 years. It is assumed that the power dissipation in CMOS chips will increase steadily as a natural result of device scaling. From the viewpoint of the technology trend in special-purpose VLSI processors, its performance improvement is still strongly requested in multimedia-application fields. Especially, large-scaled parallel arithmetic operations must be performed in such VLSI processors. Hence, energy efficiency is one of the most important factors in the recent high-performance VLSI processors. In order to solve the above problem, energy-efficient multi-core VLSI processors have been intensively developed in recent era. Since the use of the differential-pair circuit makes input voltage swing

IV. OBJECTIVE

Design of processing element using Quaternary differential logic [4]. Under this objective, different processing elements are designed for MPSoC SIMD processor [3]. With reference to master latch and threshold detector the variation of power in terms of its optimized values is obtained from 1.0V to 3.0V which is pre-scaled from 0.39V to 0.49 V at 0.675µW.

An implementation of basic gates for implementation of Quaternary D flip-flop provided for threshold detection [5] referred to mater latch confined with its slave latch CMOS based output generator of V-Ch and H-Ch based CMOS [3] format as shown in reference to Fig. 1 and Fig. 2.

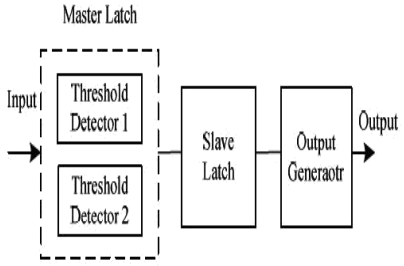

Fig 1. Quaternary D-flip flop

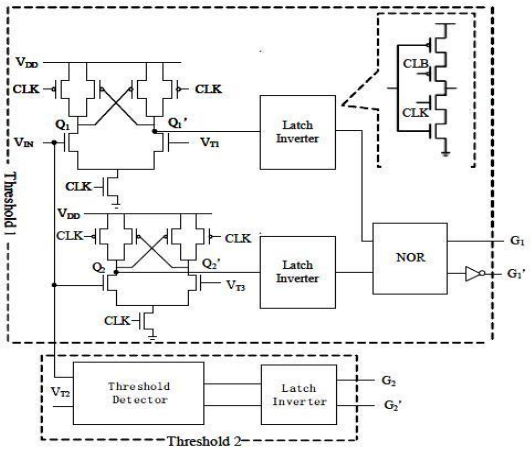

Fig 2. Block diagram of Master Latch

V. METHODOLOGY

It has been seen as in CMOS based implementation from the master latch to slave latch [7] there is considerable increase in its threshold values such that VT1>VT2>VT3 considerable speed is increased with respect to G output and G' inverted output thus, optimizing the power at a reduced rate [5] as shown in reference to table shown below Table (1).

When the MVs (Multi Valued) quaternary values are beenconsidered in terms of its master latch and threshold detectors [8]with respect to latch inverter at 3.0 V with considerableclock pulse there is optimization [6] of time period as speedrate is been increased with respect to the result. As consideredoptimized system based enhancing in detection with one bit addition is considered with respect to real time values to for provided integrated approach [4] to inverter based layout. In terms of various simulations an integrated environment based with Tanner Tools is been used compatible with operating systems based on 32-bit Windows XP, Windows 7 with supported DOS environments.

VI. RESULT

Then considering the relative values of power with accuracy of single bit addition for states (Q_1 Q_1'), (Q_2 Q_2') CMOS based values up to ± 0.06 to ± 0.04 as shown in table 2 below compared with (G_2 G_1) from table 1 obtains the result of simulations 1 and 2.

Threshold Voltage	Power
0.39 v	1.24 µW
0.45 v	1. 07 µW
0.49 v	0.675 µW

Table 2. Threshold Voltage vs. Power

Thus, the real time dynamic resistance values obtained for the CMOS based quaternary D-flip flop logic is R1 =3.2µΩ, R2 =2.4µΩ and R3 =1.4µΩ.

V_{IN}	(Q_1 Q_1')	(Q_2 Q_2')	(G_2 G_1)
0	0,1	0,1	0,0
1	1,0	0,1	0,1
2	1,0	0,1	1,1
3	1,0	1,0	1,0

Table 1. Quaternary values with provided outputs (G1, G2)

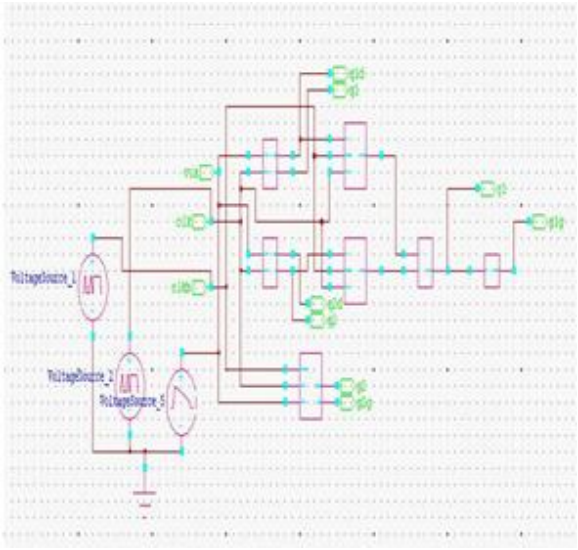

Fig 3. Simulation 1(a) Schematic of Master Latch

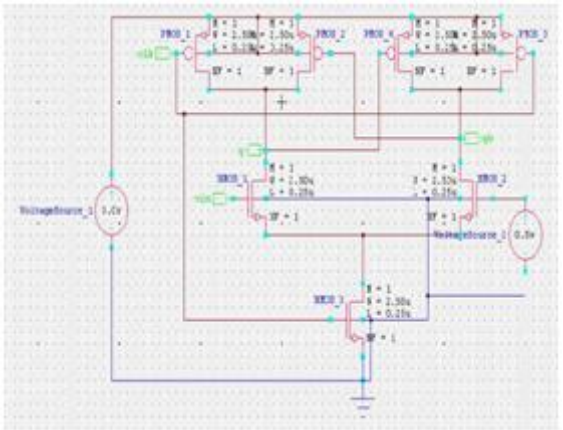

Fig 4. Simulation 1(b) Schematic of Threshold Detector

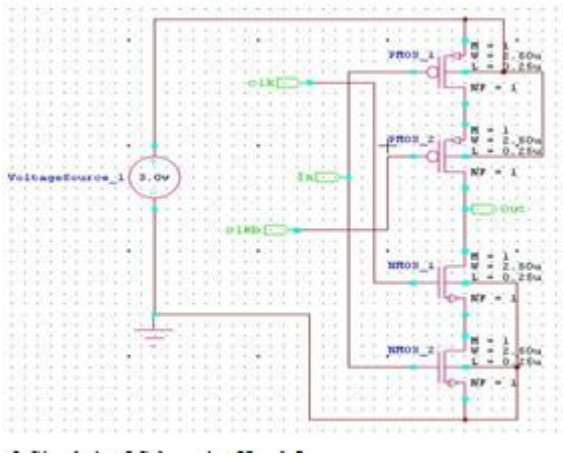

Fig 5. Simulation 2 Schematic of Latch Inverter

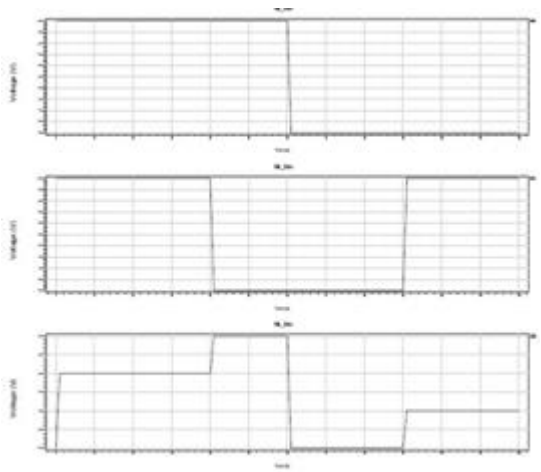

Fig 6.Result waveforms in terms Threshold scaling with Optimized Power

VII. CONCLUSION AND FUTURE SCOPE

The rescaled combination of multiple-valued current-mode circuitry and differential-pair circuitry enables to implement energy-efficient circuit. In fact, the power dissipation and VLSI based MPSoC counts of the proposed PE based MEs, respectively, under almost the same delay in comparison with those of the two-bit binary CMOS implementation. By using multiple-valued current-mode logic, the complexity of wires would be reduced, which could result in higher-speed with reference to dynamic scaled data transfer.

CMOS implementation of D-flip flop can be obtained with higher end precision to Micro-Core based SIMD with optimization of power. This provides with an open scope in terms latch enabled master slave with reference to inter cascading of quaternary logic based flip-flops thus intensifying the power optimization.

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