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VHDL Implementation of DSSS-CDMA Transmitter and Receiver (Hash function)

Gaurav P. Channe
(Department of Electronics Engineering, RTMNU Nagpur University, Maharashtra
Email: abhi_anj65@yahoo.com)

ABSTRACT
In past few years, lot of research is performed in both industries and academics into the development of CDMA. In DS-SS CDMA multiple signal channels occupy the same frequency band being distinguished by the use of different spreading codes. Digital cellular telephone system and personal communication system uses CDMA communication. In this system a base station communicates with number of mobile stations. A mobile station to based stations uplinks makes use of one frequency band and another frequency band being used for all of the down links from base station to mobile station. This project describes the direct sequence Code Division Multiple Access wireless transmitter device using field programmable gate array which has been adopted in many wireless access technology. We are implementing four separate digital blocks using VHDL approach to form Transmitter System using PN code generator, Clock Synchronizer, Parallel to serial converter and BPSK modulator. Receiver system design includes BPSK demodulator, Serial to Parallel Converter, PN Code generator and comparator. The XILINX ISE 9.2i software is to be used for design synthesis and simulation, the VHDL program is to be used for coding and FPGA for compiling and downloading the simulation. The DS CDMA wireless transmitter has to be design to transmit data rate up to 1.2 Mbps. A transmitter and Receiver components have been designed individually using Bottom-up approach. The designs then are combined and defined by component declaration and port mapping. This project concentrates on application of VHDL simulation and FPGA compiler to Wireless Data components.
Keywords **-** DSSS, VHDL, BPSK modulator and demodulator, PN Code Generator, FPGA.

I. Introduction

Direct sequence code division multiple access (DS-CDMA) technique allows improved privacy and security, increased capacity. Also it is spectrally efficient and high quality digital cellular system. VHDL implementation of DS-CDMA transmitter and receiver has been proposed in this project.

DS-CDMA is a type of spread-spectrum communication system in which multiple signal channels occupy the same frequency band, being distinguished by the use of different spreading codes. CDMA communication is employed in, for example, digital cellular telephone systems and personal communication services. In these systems, a base station communicates with a plurality of mobile stations, one frequency band being used for all of the up-links from the mobile stations to the base station, and another frequency band being used for all of the down-links from the base station to the mobile station Spread spectrum modulation technique as implemented in the Code Division Multiple Access (CDMA) principle offers many real advantages over existing time division or frequency division approaches. These advantages have been proven in military and aerospace applications in the past forty years. Because of this heritage, the overall complexity of the first generation CDMA systems tend to render themselves unsuitable for cost conscious consumer products, notably in cordless telephones and wireless PABX applications. This paper will describe an alternate implementation of the basic CDMA principle with user cost benefit trade-off as the primary focal point.

II. Literature Survey

Cellular technology has grown tremendously both in terms of traffic and services, the need for data high speed data transmission has increased, The mobile telecommunication industry faces the problem providing technology that be able to support a variety of services ranging from voice communication with a bit rate of few Kbps to wireless multimedia in which bit rate up to 2 Mbps, This tremendous growth has also been fueled by the recent improvements in the capacity of wireless links due to the use of multiple access techniques.

The idea is to transmit signals simultaneously through a linear band limited channel without inter channel or inter symbol interference. To design multi channel transmission must concentrate on reducing cross talk between adjacent channels.

One of the most promising cellular standards is IS-95 CDMA system. The advantages of CDMA standard over other standards are security, optimum subscriber power management, efficient power control, compatibility, multipath fading. The forward link frequency of CDMA is in the range of (869-894) MHZ and the reverse link frequency is in the range of (824-849)MHZ, In mobile communication transmission from the base station to mobile user are on the forward link and the transmission from mobile user to base station are on the reverse link. In the recent years the CDMA on FPGA platform has attracted attention of academic research and industry.

III. Multiple Access Techniques

Multiple Access method allows many simultaneous users to use the same fixed bandwidth frequency spectrum. For mobile phone systems the total bandwidth is typically 50 MHz, which is split in half to provide the forward and reverse links of the system. Sharing of the spectrum is required in order to increase the user capacity of any wireless network. FDMA, TDMA and CDMA are the three major methods of sharing the available bandwidth to multiple users in wireless system. Among these multiple access techniques CDMA provides less interfered and more secured type communication hence is more important.

3.1. Frequency Division Multiple Access

In Frequency Division Multiple Access available bandwidth is subdivided into a number of narrower band channels. Each user is allocated a unique frequency band in which to transmit and receive on. During a call, no other user can use the same frequency band. Each user is allocated a forward link channel (from the base station to the mobile phone) and a reverse channel (back to the base station), each being a single way link. The transmitted signal on each of the channels is continuous allowing analog transmissions. The channel bandwidth used in most FDMA systems is typically low (30 kHz) and channel only support a single user.

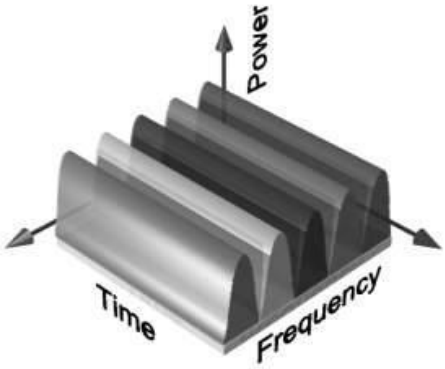


Fig. 1 FDMA

3.2. Time Division Multiple Access

Time Division Multiple Access (TDMA) divides the available spectrum into multiple time slots, by giving each user a time slot in which they can transmit or receive TDMA systems Transmit data in a buffer and burst method, thus the transmission of each channel is non-continuous. The input data to be transmitted is buffered over the previous frame and burst transmitted at a higher rate during the time slot for the channel. TDMA cannot send an analog signal directly due to the buffering required, thus is only used for transmitting.

3.3. Code Division Multiple Access

Code Division Multiple Access (CDMA) is a spread spectrum technique that uses neither frequency channels nor time slots. With CDMA, the narrow band message (typically digitized voice data) is multiplied by a large bandwidth signal that is a pseudo random noise code (PN code). All users in a CDMA system use the same frequency band and transmit simultaneously. The transmitted signal is recovered by correlating the received signal with the PN code used by the transmitter.

CDMA technology was originally developed by the military during World War II. Researchers were spurred into looking at ways of communicating that would be secure and work in the presence of jamming. Some of the properties that have made CDMA useful are:

Anti-jam and interference rejection

Information security

Accurate Ranging

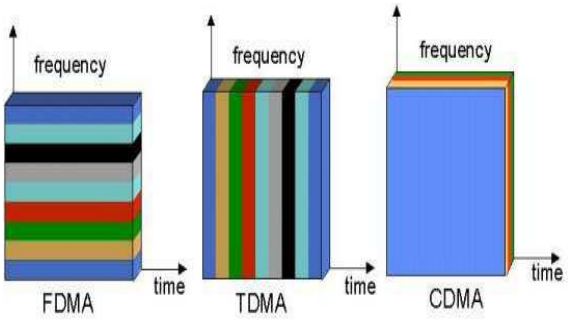


Fig. 2 Types of Multiple Access Schemes.

IV. Spread Spectrum Techniques

Based on the modulation method the CDMA technique can be classified into three categories.
CDMA: direct sequence (DS)
CDMA: frequency hopping (FH)
CDMA: time hopping (TH)

4.1. Direct Sequence CDMA Generation

DS-CDMA is achieved by spreading the data signal by a pseudo random noise sequence (PN code), which has a chip rate higher than the bit rate of the data. The PN code sequence is a sequence of ones and zeros (called chips), which alternate in a random fashion. The PN code used to spread the data can be of two main types. A short PN code (typically 10-128 chips in length) can be used to modulate each data bit. The short PN code is then repeated for every data bit allowing for quick and simple synchronization of the receiver. Alternatively a long PN code can be used. In DS-CDMA the spreaded signal is modulated by a RF carrier. For the modulation, various modulation techniques can be used, but usually some form of phase shift keying (PSK) like binary phase shift keying (BPSK), differential binary phase shift keying (D-BPSK), quadrature phase shift keying (QPSK), or minimum shift keying (MSK) is employed.

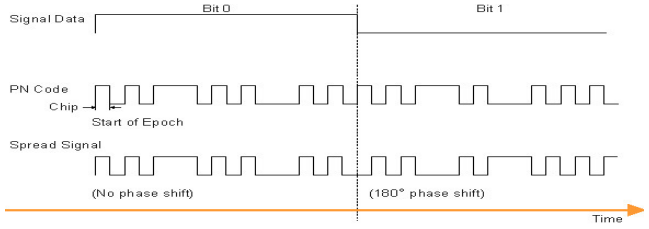


Fig. 3 Direct sequence signals

In DS-CDMA the data signal is directly modulated by a digital, discrete time, discrete valued code signal from this direct multiplication that the direct sequence CDMA gets its name.

V. Hardware and Software Design and Implementation.

5.1. Specifications

Clock: 8MHz,
Data Rate: 1.4MBS,
Frame length: 35s,
Soft handover: Yes,
Number of Input bits: 5,
Spreading codes: hashed sequence,
No of bits in PN sequence: 7,
No of PN sequence: 128,
Type of Modulation: BPSK,
Type of demodulation: BPSK demodulation

5.2. *Synthesis*

Front end Design Entry: VHDL,
Backed synthesis: Xilinx Spartan II FPGA Following tools are used while developing, testing, implementing and programming the CDMA transmitter and receiver blocks.

5.3. CDMA Transmitter

Code Division Multiple Access (CDMA) is used in spread spectrum systems to enable multiple-access. It is a transmission technique in which the frequency spectrum of a data-signal is spread using a code uncorrelated with that signal and unique to every addressee. As the applied codes are selected for their low cross-correlation values, it is possible to make a distinction between the different signals. An initiator knows the code of the intended addressee and is so capable of activating the desired communication link.

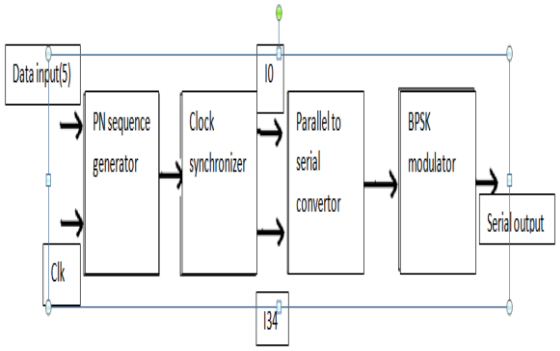


Fig. 4 CDMA transmitter

The main blocks of CDMA transmitter are listed below.

- PN sequence generator
- Clock synchronizer
- Parallel to serial convertor
- BPSK modulator

5.3.1. PN sequence generator

The important block of DS-CDMA communication system is the PN sequence generator. Here we are using HASH function for generation of PN Sequence.

Hash Function: A hash function is any well-defined procedure or mathematical function that converts a large, possibly variable-sized amount of data into a small datum, usually a single integer that may serve as an index to an array. The values returned by a hash function are called hash values, hash codes, hash sums, checksums or simply hashes.

The following steps are as follows for the hash Algorithm

- Take N bits PN sequence initialized with zeros
- Take a count of N bits length
- If count is greater than 0 and less than N/2, then perform xnoring of pnseq(count)=1 With pnseq(count-1).
- Else if count is less than or equal to N/2, then perform xoring of pnseq(N-count) with pnseq(count)
- Else if count is equal to 0 then assign 1's to pnseq

Hashed sequence versus M-length sequence –

Hashed sequence used here gives less cross correlation .

– Good Autocorelation, Unique coding, Channel interference is less

5.3.2. Parallel to Serial Converter

A parallel to serial converter for converting incoming parallel, byte sized, data supplied at a first data rate to single bit serial data includes a shift register in which several bytes of the incoming data are stored simultaneously and thereafter serially transmitted there from. The parallel to serial converter includes latching devices in which the incoming data bytes are stored prior to being transferred to the shift register. Since successively arriving bytes of data are stored in successively selected ones of the latching devices, the data rate (device speed) of the latches is permitted to be only a fraction of the first data rate associated with the incoming bytes of data resulting in a fast, yet inexpensive, circuit.

5.3.3. Binary Phase-Shift Keying (BPSK*)*

BPSK (also sometimes called PRK, Phase Reversal Keying, or 2PSK) is the simplest form of phase shift keying (PSK). It uses two phases which are separated by 180° and so can also be termed 2-PSK. It does not particularly matter exactly where the constellation points are positioned, and in this figure they are shown on the real axis, at 0° and 180°. This modulation is the most robust of all the PSKs since it takes the highest level of noise or distortion to make the demodulator reach an incorrect decision. It is, however, only able to modulate at 1 bit/symbol (as seen in the figure) and so is unsuitable for high data-rate applications when bandwidth is limited.

5.4. DS-CDMA RECEIVER

The receiver is by far the most complicated part of the communication system. The receiver must perform several different tasks. Mainly they are demodulation, synchronization, and dispreading. A DS-CDMA receiver is based on a correlator, which utilizes correlation properties of the PN codes . The correlators attempt to match the incoming received signal with each of the candidate prototype waveforms (PN sequences) known a priori to the receiver. Since we deal with the discrete signals in practice, the discrete form of the correlation of two discrete signals is given as

$$Rxy(k) = \sum_{n=0}^{N-1} x(n)\, y(k+1) \qquad \text{.....(1)}$$

Equation (1) is the fundamental equation implemented in software and hardware. The hardware implication is that the implementation of a correlator is based on a multiplier accumulator circuit. At the receiver, the same PN sequence used in the transmitter is correlated with incoming signal. Block diagram of the receiver is shown

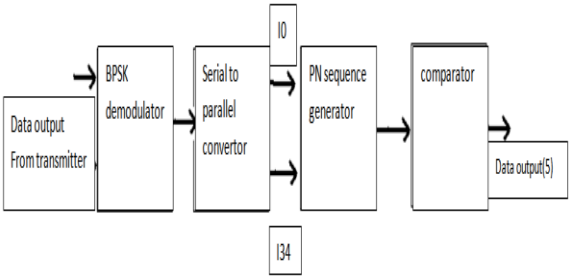


Fig. 5 CDMA Receiver

5.4.1. Demodulation

The first task of the receiver is to demodulate the signal. This is simply put a frequency shift of the received signal. Here BPSK demodulator is used to demodulate the signal. The output of BPSK demodulator is serial which is fed to serial to parallel converter.

5.4.2. Serial to Parallel Converter

The design of a serial-to-parallel converter that reads a serial bit-stream input and produces an n-bit output. When no data is being transmitted to the serial port, keep it at a value of '0'. Each n-bit value requires m clock cycles to read it. On the m+1 clock cycle, the parallel output value can be read. In the first cycle, a '1' is placed on the serial input. This

assignment indicates that an n-bit value follows. The next n cycles transmit each bit of the value. The most significant bit is transmitted first. The m cycle transmits the parity of the n-bit value. It must be '0' if an even number of '1' values are in the n-bit data, and '1' otherwise

5.4.3. Synchronization

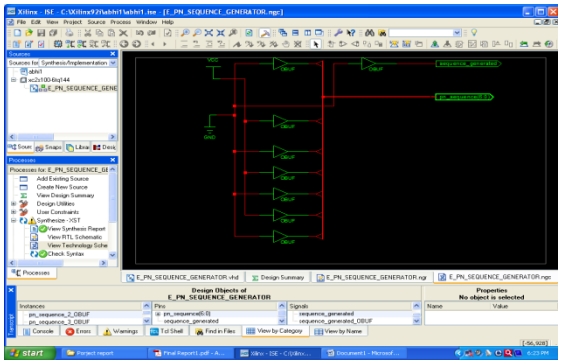
One of the major problems in the transmission is to make sure that the transmitter and receiver are synchronized. Without a precise synchronization a correct transmission will not be possible. In this project, control signal is used to indicate whether receiver and transmitter are properly synchronized.

5.5.4. Despreading

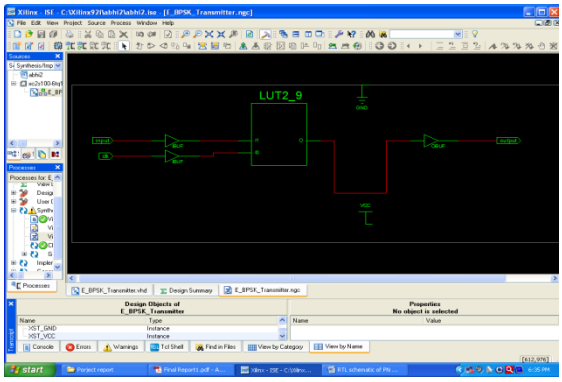
After the equalizing the received bits needs to be despread. Multiplying the spread signal with the known PN-sequence performs the despreading. Note that the length of the PN-sequence may vary between different transmissions. After the despreading of the signal, N number of bits will represent one original bit, i.e. an error free transmission would yield N number of equal bits for each original bit.For the PN sequence in the receiver, it was mentioned that it should be an exact replica of the one used in the transmitter. Once, the incoming PN code is correlated with the locally generated one, we can despread the signal. After the signal gets multiplied with the PN sequence, the signal despreads.

VI. Result

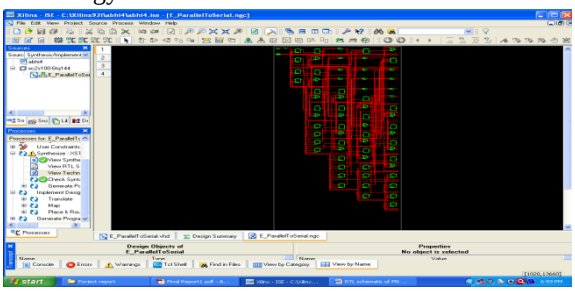
Technology Schematic of PN sequence Generator



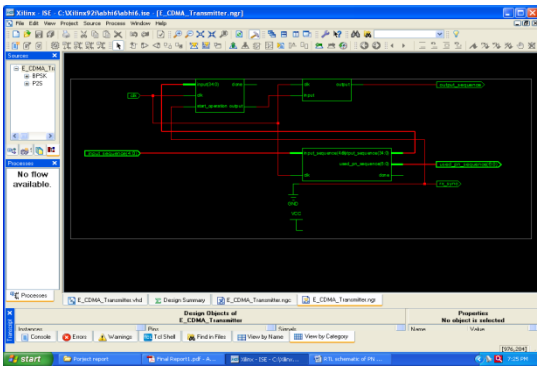
Technology Schematic of BPSK Transmitter



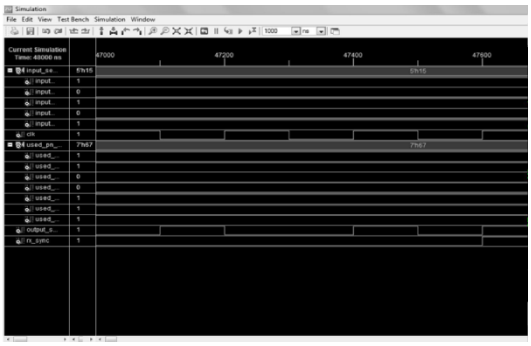
Technology schematic of Parallel to Serial convertor



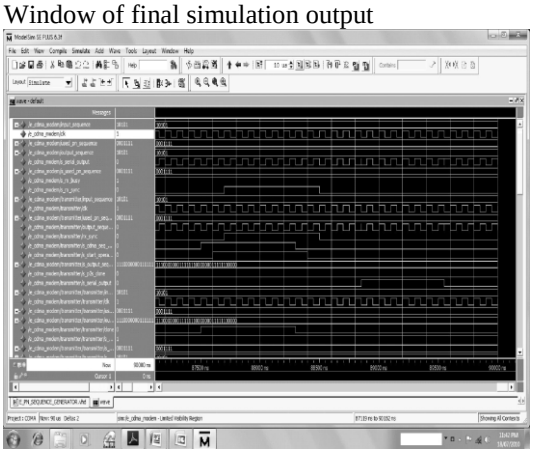
RTL schematic of CDMA Transmitter



Simulation of CDMA Transmitter



Window of final simulation output



VII. Conclusion

CDMA is one of the most important multiple access technique .In this project the transmitter and receiver were implemented on FPGA. After synthesis simulations are agreed before synthesis simulations. The transmitter was connected to the receiver before

synthesis was done to verify functionality of the transmitter and receiver. This has been tested using an arbitrary chosen data stream, where these data have been transmitted through implemented transmitter and then received by our implemented receiver.

A comparison has been done between the transmitted and received data and satisfactory results have been achieved.

DSSS technique in VHDL has the following advantages

- The design is fully reconfigurable the number of bits and PN sequence can be changed very easily
- Useful for both FPGA and ASIC implementations.

Future scope

The security of the data can be increased if we can use complex techniques for PN coding or using complex polynomial function for LFSR which are understood by the person who knows the actual format. The BPSK modulation is used in this and if we have used other advanced modulating techniques output frequency can be increased and this can be transmitted to long distances .

Acknowledgment

Gaurav Pradip Channe is a M-Tech.(VLSI Design) student and a research scholar in the Department of Electronics from PCE , affiliated to RTMNU Nagpur, Maharashtra, India. He received the B.E. degree from RTMNU University Maharashtra in 2011. His current research interests are in communication protocols for wireless ad hoc networks and complicated digital circuits.

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