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A REVIEW ON 4 BIT FLASH ANALOG TO DIGITAL CONVERTOR

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Abstract :
This paper presents the review of Analog to Digital Convertor (ADC). For ADC there are mainly four different methods, Flash ADC, Pipelined ADC, Successive Approximation ADC, Sigma Delta ADC. The Flash ADC is the Fast ADC. For Designing the ADC, the parameters important are Static and Dynamic. In static parameters Differential Non Linearity Error (DNLE), Integral Non Linearity Error (INLE) and in dynamic parameters Signal to Noise Ratio (SNR), Effective Number of Bits (EONB), Spurious-Free Dynamic Range (SFDR), Dynamic Range (DR). The design issues which consist first CMOS inverter used in CDC architecture, MUX based Decoder and DAC.
Key Words : ADC, DNLE, INLE, SNR, EONB, SFDR, DR, CDC, Mux based Decoder.

I.   Introduction

Analog to digital convertor circuit converts analog signal into digital signal. Analog signal is the signal whose amplitude is continuously changing with respect to time But in the Digital signal the amplitude and time is discrete. The ADC is characterized by three factor speed, area, and power consumption, the cost of ADC is varying from application to application.

For considering the speed of ADC we have to design the ADC with small voltage supply and we have to shrink the size of ADC, for this application we are designing Flash ADC with Clocked Digital Convertor (CDC) configuration which eliminates the resistive network required for generation of internal reference voltage.

Types of ADC
1.   Sigma Delta ADC.
2.   Successive Approximation Register   (SAR) ADC.
3.   Pipelined ADC.
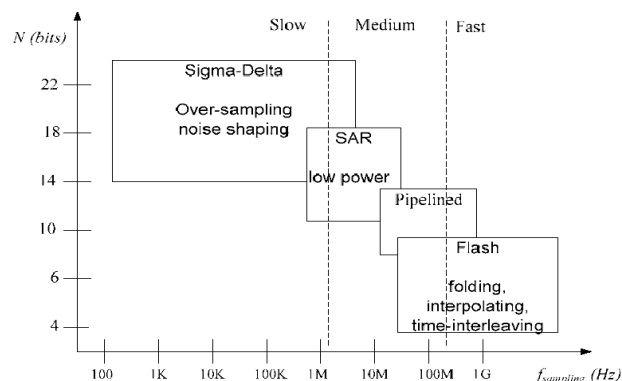4.   Flash ADC.
Comparison between different ADC [9]

Figure 1 : Comparison of different ADC[9]

Flash ADC : The flash ADC operates at very high speed with lower resolution. It is also called a parallel ADC due to its parallel operation.
Pipelined ADC : The pipelined ADC can operate at a high speed, but it is slower than the flash. It covers a wide range of applications because of its flexible resolution and speed.
Successive Approximation Register ADC : The SAR ADC is suitable for low power and medium-to-high resolution applications with medium speed.
 Sigma-Delta ADC : The Sigma Delta ADCs are used for high resolution and low speed applications.

ADC Parameters

The parameters of an ADC can be obtained from the data sheet of ADC. The parameters are classified into two categories
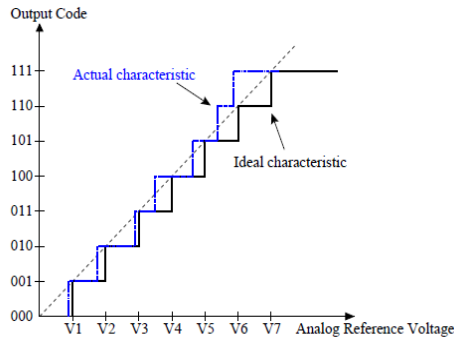
1) Static Parameters

Figure 2: Staircase transfer function of ADC[9]
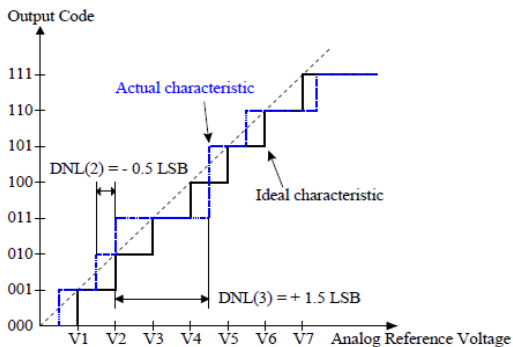
i) Differential Non Linearity Error (DNLE)

Figure 3: Differential Non-Linearity error[9]
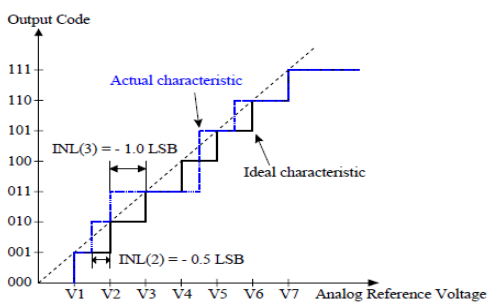
ii) Integral Non Linearity Error (INLE)

Figure 4: Integral Non-Linearity error[9]

2) Dynamic Parameters.

i) Signal to Noise Ratio (SNR)

The SNR is defined as, it is the ratio of signal power to the noise power.

SNR = (Signal power) / (Noise power)

$(SNR)_{db}$ = (Signal power) - (Noise power)

In Ideal Case, $(SNR)_{db}$ = 6.02N+1.76

Where N= Resolution of ADC.

The SNR analysis gives you the noise quantity in the ADC

ii) Effective Number of Bits (EONB)

The Effective number of bit is totally depend on the input signal it is defined as,

ENOB = (SNR-1.76) / 6.02

The ENOB will decrease by increasing the input frequency because the noise is totally depend on the input frequency as frequency increases the noise increases as a result SNR decreases.

iii) Spurious-Free Dynamic Range (SFDR)

It is ratio of Signal power to the highest amplitude of the harmonic.

SFDR = 20 log(Signal power/ highest amplitude of the second harmonic)

SFDR is the most important factor to distinguishing the input signal from the undesired spur. For analysis of SFDR Fast Fourier Transform plot (FFT) is required.

iv) Dynamic Range (DR)

It is defined as, it is ratio of largest output signal change over smallest output signal change.

DR = 20 log(largest output signal change / smallest output signal change

Design Issue

1. Clocked Digital Comparator
2. Transistor Inverter Quantizer (TIQ)
3. CMOS Inverter as Phase Shifter
4. CMOS Inverter as Quantizer
5. Transmission Gate
6. Multiplexer Based Decoder
7. Digital to Analog Convertor (DAC)
8. Working of ADC-DAC

Clocked Digital Comparator [8]

For conversion of analog signal into digital signal requires the quantizer, sampler and encoder. In clocked digital comparator shown in fig. 8, the first stage consist of two inverter the first inverter is acting as the quantizer by settling the comparator voltages for comparison and the second inverter is acting as the logic level inversion, the need of second inverter is arises due to the output of first inverter. In ADC and DAC structure the output should be same as the input signal but the first inverter inverts the input and later on we'll get the output out of phase so for nullifying the phase shift we have to add the second inverter.
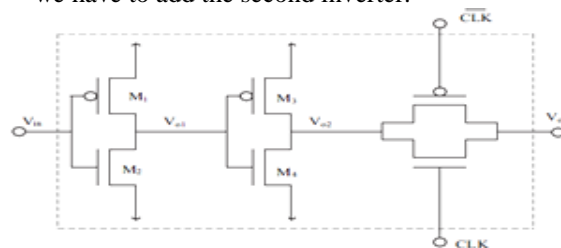

Figure 5 : Clocked Digital Comparator [8]

Transistor Inverter Quantizer (TIQ) [8]

Comparator structure is most pivotal part in FADC architecture. The role of comparator is to compare the input signal with reference voltage and gives the respective logic levels (1 and 0) the comparator converts the input signal into only two logics (logic1 and logic 0) depending on the values of input, if the values of input is greater than threshold value then it'll give logic 1 else it'll give logic 0.
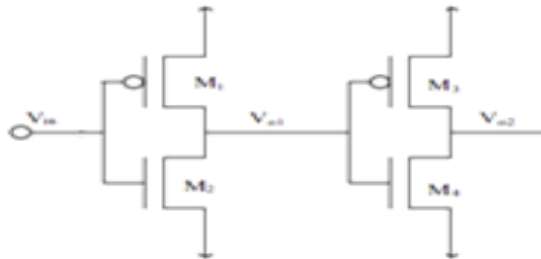

Figure 6 : Transistor Inverter Quantizer [8]

The TIQ shown in fig 9 is the first stage of CDC, it is use for generating the internal reference voltage which is required for comparison, the internal reference voltage is generated using number of methods like resistive ladder network, systematically varying the size of transistor. In TIQ the internal reference voltage is generated by systematic varying the width of NMOS and PMOS we are keeping the length of transistor is same because the length of transistor is depend on the technology.

CMOS Inverter as Phase Shifter [8]

The inverter provides phase shift, amplification, quantization stages. Let us consider the signal given to the clocked digital comparator is sine wave then inverter gives the output negative of sine wave, $x(t)=A*\sin(wt)$ as input inverter gives $x_1(t)=A*\sin(wt+pi)$
further solved this equation by applying some mathematical relationship
$\sin(A+B) = \sin A*\cos B+\cos A*\sin B$
$x_1(t)= A*\sin(wt)*\cos(pi)+A*\cos(wt)*\sin(pi)$
$x_1(t)= - A*\sin(wt)$
[As $\cos(pi)=-1$ and $\sin(pi)=0$]

CMOS Inverter as Quantizer [9]

The Clocked Digital Comparator compares the input voltage with reference voltage generated by varying the width of each comparator depending on the value of reference voltage each comparator gives its logic level. The four bit comparator requires fifteen comparator since they will generate their respective fifteen levels in this way they are acting as quantizer.

Transmission Gate [8]

The second stage consist of transmission gate, the use of transmission gate is for sampling the signal as

we know the transmission gate work on clock signal if the transmission gate is positive edge enabled clocked then it works only for positive edges that means it only pass the logic for positive edge and blocked the logic for negative edge that's why we generally called transmission gate as the switch.

The frequency on which clocked operates called as sampling frequency and the sampling frequency should be more than twice of input frequency, so the clocked digital comparator is acting as the quantizer and sampler. It can be shown that the Vm point on the VTC of a CMOS inverter, which is shown in Fig. 10, can approximately be given by the following equation

$$V_m = \frac{\sqrt{\frac{\mu_p W_p}{\mu_n W_n}}(V_{dd} - |V_{Tp}|) + V_{Tn}}{1 + \sqrt{\frac{\mu_p W_p}{\mu_n W_n}}}$$

Figure 7 : Formula for Finding Internal Reference Voltage [8]

where Vtn and Vtp are the threshold voltages for NMOS and PMOS devices, respectively; and Kn = (W/L)n . mn Cox Kp = (W/L)p . mp Cox.

Multiplexer Based Decoder [6]

The multiplexer based decoder circuit uses 2:1 Mux so we required 11 Mux for implementing 15 inputs. The 2:1 Mux required two input signals with one select line, the select line should vary between two logics 0 to 1 depending on the select line the Mux'll transmit the logic, the truth table of 3 bit thermometer code itself expressing the logic the M.S.B. bit of binary input equal to middle bit of thermometer code because it follows the twin logic.
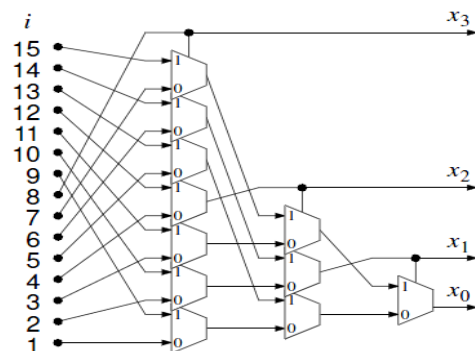

Figure 8 : Multiplexer Based Decoder [6]

The working principal of multiplexer based decoder is shown in table 1 and in table 2 the M.S.B bit of the output is equal to the T_2 bit of input (Middle bit) and L.S.B. of output is equal to the value of T_1 and T_2 respectively. In this design 11 multiplexer are used because in first stage there are 15 inputs for

implementing 15 input 7 mux are used in the second stage 3 mux are used the output of middle multiplexer is acting as select line in the second stage while in last stage 1 mux is required.

Table 1: conversion of 3-bit thermometer code to binary code [6]

Thermometer code			Binary Code	
T_3	T_2	T_1	B_2(MSB)	B_1
0	0	0	0	0
0	0	1	0	1
0	1	1	1	0
1	1	1	1	1

Digital to Analog Convertor (DAC) [8]

The DAC configuration shown in fig 12 consist of a network of resistor alternating in value of R and 2R. Starting from bottom of network the 2R resistor is connected to the Vref- the digital input decides which resistor is switched to Vref- and Vref+.
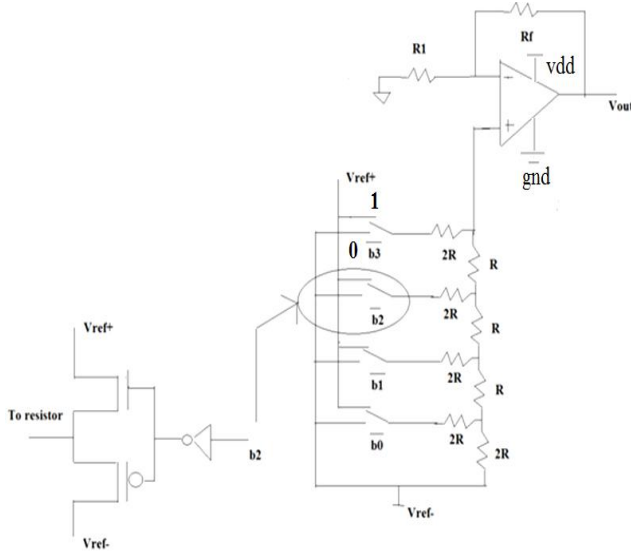

Figure 9: Digital to Analog Convertor [8]

Working of ADC-DAC [8]:

The fifteen comparator are worked depending on their internal reference voltage as the input signal amplitude crosses the threshold value of reference voltage respective comparator works that's why they are generating the thermometer code, as the input signal crosses

maximum value of amplitude then all comparator moves to the saturation region they produces the output equal to logic 1.

After interfacing ADC and DAC together they must produce the output same as the input

signal which is shown below, the threshold voltage are laying in the range from 0.653 to 1.02 volt for this range only the ADC produce the respective binary bits for below this range the output equal to zero and above this range the output equal to one. In this design the clocked is use the effect of clocked is showing on the output for positive interval of clocked the logic is generating and for the negative interval it produces zero output.

The above logic is valid only when the amplitude of input signal starts from zero and reaches toward the maximum value as the amplitude falls from the maximum value toward zero value the effect of mobility arises. As we know the mobility of electron is equal to the three times the mobility of hole the output is not same as the input.

When the input is at logic zero the pmos produces the output equal to logic one but if you observe as the pmos conducts it'll connect to the vdd (positive supply) supply it required some delay but in case of nmos when it conducts it'll connect it to ground (negative supply) it will connect to the ground fast as compare to pmos that's why the output is not exactly same as the input.

Conclusion :

By considering all these we can design the 4 bit Flash ADC and find all the given parameters. Compare these parameters with the standred parameters.

References

[1.] Navneet Kaur, Gurpurneet Kaur "Investigation of Fast Switched CMOS Inverter using 180nm VLSI Technology" International Journal of Computer Applications (0975 – 8887) Volume 51– No.15, August 2012 .

[2.] 2. Mingzhen Wang, Hongxi Xue "Design Optimization of CMOS CDC Comparators" Proceeding of 978-1-4577-0603-5/11/$26.00©2011 IEEE 2011

[3.] 3. Meghana Kulkarni, V. Sridhar, G.H. Kulkarni, "4-Bit Flash Analog to Digital Converter Design using CMOS-LTE Comparator", Proceeding of 978-1-4244-7456-1/10/$26.00©2010 IEEE 2010

[4.] Meghana Kulkarni, V. Sridhar, G.H. Kulkarni, "The Quantized Differential Comparator in Flash Analog to Digital Converter Design", Proceeding of International Journal of Computer Network & Communication (IJCNC), Vol 2, No. 4, July 2010

[5.] Ali Tangel, Kyusun Choi, " The CMOS Inverter as a Comparator in ADC Designs", Analog Integrated Circuits and Signal Processing, 39, 147-155, 2004

[6.] Erik Säll and Mark Vesterbacka " A multiplexer based decoder for flash analog to digital convertor ", Proceeding of 0-7803-8560-8/04/$20.00©2004 IEEE, 2004

[7.] Jincheol Yoo, Kyusum Choi and Tangel, "A 1-GSPS CMOS flash A/D convertor for system on chip application", IEEE computer society workshop on 19-20 April 2001 Page (s):135-139

[8.] M. Wang, "High Speed Low Power CMOS flash analog to digital convertor for wideband communication system-on-a-chip " PhD Dissertation, The Wright State University, 2007.

[9.] J. Yoo, "A TIQ Based CMOS Flash A/D Converter for System-on-Chip Applications," Ph.D. Dissertation, The Pennsylvania State University, May, 2003.