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Implementation of Vedic Complex Multiplier for Digital Signal Processing

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Abstract—
Basic and heart of all DSP are its multiplier. Speed of multiplier determines the speed of the DSP.In DSP fast multiplication is very important for convolution, Fourier transforms, and Multiplication is the most basic operation with deep and thorough arithmetic computation. Latency and throughput are two important parameter associated with multiplication performed in DSP.
In this paper VHDL implementation of complex number multiplier using ancient Vedic mathematic. By using "Vedic Mathematic "concept can skip carry propagation delay. The "Urdhva Tiryakbhyam" sutra was selected for implementation since it is applicable to all cases of multiplication. Meaning of "Urdhva Tiryakbhyam" is vertically and crosswise. The partial product and sum are generated in single step which reduce carry propagation from LSB to MSB.The main feature of proposed system are flexibility. The important feature of this project is to improve the speed of complex multiplier using Vedic mathematics. The implementation of Vedic mathematics and their application to complex multiplier ensure reduction of propagation delay. The proposed system is design using VHDL and is implemented through Xilinx ISE 9.1i navigator series. The combinational delay obtained after the synthesis is compared with Booth's complex multiplier. Vedic complex multiplier can bring great improvement in the DSP performance.
Keywords- *Vedic multiplier, Urdhava tiryakbhyam, VHDL, DSP.*

I. INTRODUCTION

Multiplier is important components of many high performance systems such as FIR filters, microprocessor, digital signal processor, etc.Complex number multiplication is important in Digital single processing(DSP),specially in DIT-FFT twiddle factor multiplied with input is complex number, Image processing(IP).To implement Discrete Fourier Transform(DFT),Discrete Cosine Transform(DCT),Fast Fourier Transform(FFT) and wireless communication imaging, complex multiplier are required. Complex numbers mostly depend on extensive number of multiplication. Four real number multiplication and two additions or subtractions are involve in complex number multiplication .Multiplication is done by AND operation & addition is done by OR operation. Carry needs to be propagated from the least significant bit (LSB) to most significant bit (MSB) when binary partial products are added in real number multiplication. Competence of multiplier is based on variation of speed, area and configuration. After binary multiplication, the overall speed is drop down by addition and subtraction [4][5].

Vedic mathematic is extracted from four Vedas, which is an upya-veda of Atharva-veda.Vedic Mathematics is based on 16-sutras and 16-sub sutras invented in (1884-1960).In Vedic mathematics there are sutras Nikhilam Navatascaraman Dasatah and Urdhva Tiryakbhyam used for multiplication[1]. Our targeted Vedic sutra (algorithm) which is suitable for all cases of multiplication is Urdhva Tiryakbhyam.

A multip lier is one of the basic hardware blocks in complex multiplier used in most digital signal processing sy stems. With advances in technology , many researchers have tried to design multip liers which offer high speed and low power consumption,

In this paper high speed complex multiplier is design using Vedic mathematics. In this work, we try to present complex multiplication operations and the imp lementation of these using both booth's as well as Vedic mathematical methods in VHDL language [1]. We highlight a comparative study of both approaches in terms of gate delays.

II. THE VEDIC MULTIPLICATION METHOD

The Vedic Mathematics is an ancient mathematic invented by Jagadguru Shankaracharya

Bharati Krishna Teerthaji Maharaja. Vedic mathematic is based on 16 sutra and 16 sub-sutra. These sutra have been traditionally used for multiplication of two numbers. The proposed complex number multiplier is based on the Urdhva Tiryakbhyam sutra. In this work the same ideas are applied to binary number system as well as decimal number system, to make the proposed algorithm compatible with the digital hardware.

Vedic multiplication based on Urdhava Tiryakbhyam sutra is discussed below

A. Urdhva Tiryakbhyam sutra

The basic meaning of Sanskrit word is "Vertically and crosswise". It is applicable to all multiplication. The vertical and crosswise multiplication can be implemented starting either from left hand side or from right hand side [7][8].

Significance of vertically is straight above multiplication and significance of crosswise is diagonal multiplication and add them. In "Urdhva Tiryakbhyam sutra" multiplication is done in single line manner, implies the increase in speed by reducing propagation delay [9][12]. This sutra traditionally used for multiplication of decimal numbers. In this paper same ideas apply for binary number system.

It literally means "Vertically and crosswise". It is based on a novel concept t through which the generation of all partial products can be done with the concurrent addition of these partial products. Since the partial products and their sums are calculated in parallel. To calculate the product, the multiplier is independent of the clock frequency of the processor. Thus the multiplier will require the same amount of time and hence is independent of the clock frequency. The Multiplier has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other multipliers. Therefore it is time, space and power efficient

"Urdhva Tiryakbhyam sutra" to binary number system knowledge that multiplication of two bit is done by AND operation and it is implemented by using AND operation. General multiplication procedure using "Urdhva Tiryakbhyam sutra" is illustrated below.

The below figure shows multiplication of (4x4) bit number, performance is starting from right hand side. Corresponding expression as follows:

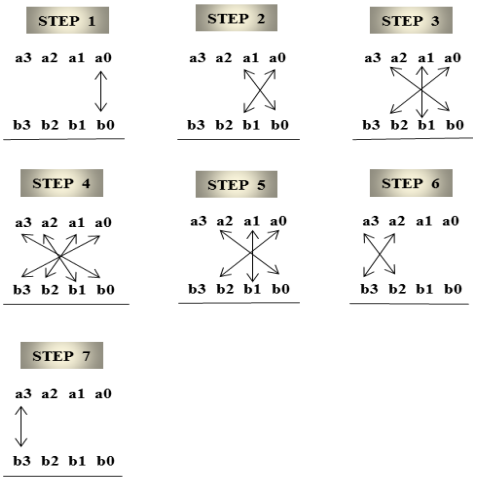

Figure 1: Line diagram for multiplication of two 4 - bit numbers.

Firstly, least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits of the two numbers from least significant position. Next, all the four bits are processed with crosswise multiplication and addition to give the sum and carry. The sum is the corresponding bit of the product and the carry is again added to the next stage multiplication and addition of three bits except the LSB. The same operation continues until the multiplication of the two MSBs to give the MSB of the product.

Thus we get the following expressions:

$$r0 = a0b0 \quad (1)$$

$$c1r1 = a1b0 + a0b1 \quad (2)$$

$$c2r2 = c1 + a2b0 + a1b1 + a0b2 \quad (3)$$

$$c3r3 = c2 + a3b0 + a2b1 + a1b2 + a0b3 \quad (4)$$

$$c4r4 = c3 + a3b1 + a2b2 + a1b3 \quad (5)$$

$$c5r5 = c4 + a3b2 + a2b3 \quad (6)$$

$$c6r6 = c5 + a3b3 \quad (7)$$

With c6r6r5r4r3r2r1r0 being the final product [3] [4] [8].

The Hardware architecture realization of multiplier of Urdhava Tiryakbham shown in figure 2.All the partial product are calculated parallel and delay is

associated to time taken by carry to propagate through adder.

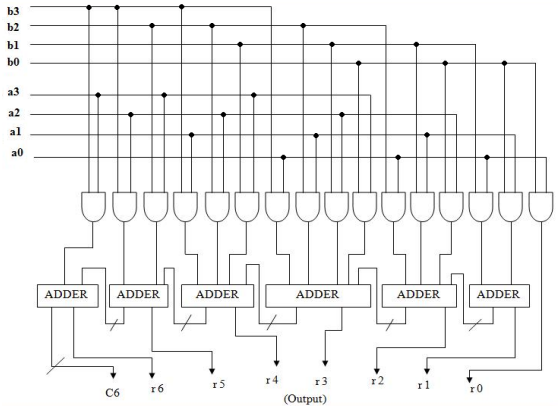

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Figure 2: Hardware architecture of the Urdhava tiryakbhyam multiplier. [6]

III. COMPLEX MULTIPLIER

Complex number consists of two component known as Real part(R) and Imaginary part (I).
For implementing complex number multiplication, require real part and imaginary part.

$$R + j\,I = (a + j\,b)\,(c + j\,d) \qquad (1)$$

(a + j b) is first complex number,
(c + j d) is second complex number,

From equation(1) gives two separate final result to calculate real and imaginary part .The real part of the output can be computed using (ac-bd), and the imaginary part of the result
can be computed using (bc+ad). Thus four separate multiplications and addition/subtraction are required to produce the real as well as imaginary part numbers [9] [10] Multiplication is performed by using "Urdhva Tiryakbhyam sutra".

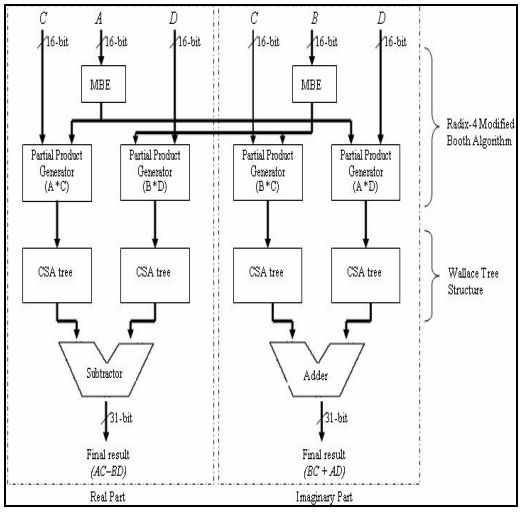

Figure3: Block diagram of Complex Multiplier. [2]

Complex Multiplication Algorithm :(a+jb) (c+jd) = R+jI.

<Input>:

A and B:
(a+jb) and (c+jd) both are complex number.
(a+jb) and (c+jd) both are inputs.
Real part of A = a;
Imaginary part of A = b;
Real part of B = c;
Imaginary part of B = d;

<Output>:
Result: R and I are the real and imaginary part of complex number.

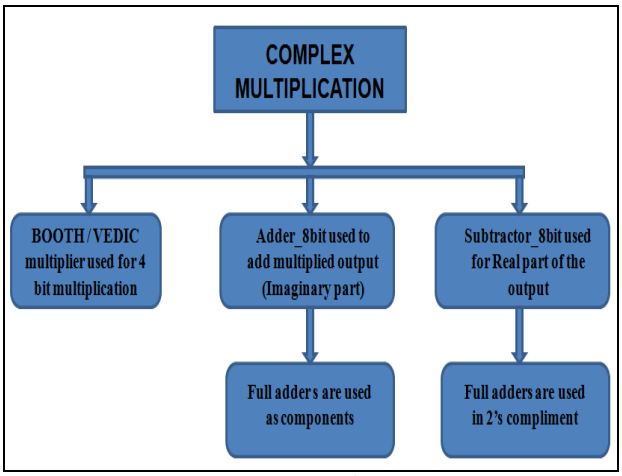

Figure 4:.Proposed methodology for complex number multiplication

IV. DESIGN & IMPLEMENTATION

The Vedic Complex Multiplier is implemented using VHDL and also other multipliers like booth multiplier are also imp lemented. The entire code is comp letely sy nthesizable. The sy nthesis is done using Xilinx Sy nthesis Tool (XST) available with Xilinx ISE 9.1i simulator. The design is op timized for speed and area using Xilinx.
Table 1 indicate the area consumed and speed taken to do the implementation for 4-bit Vedic complex & Booth complex multipliers. Table 2 indicate the area consumed and speed taken to do the implementation for 4-bit & 8-bit Vedic complex. While Figure 6 & 7 indicates the RTL schematic of the 4 bit Vedic complex multiplier and Booth's complex multiplier. Figure 8 & 9 indicates the simulation waveform for 4-bit Vedic complex multiplier and Booth's complex multiplier.
The speed taken to do the implementation for 4-bit Vedic complex, Booth complex multipliers are given in below Charts(Figure 5).

TABLE 1:
DEVICE UTILIZATION SUMMARY

Algorithm(4bit)	NO. of Slices	NO. of 4 input Slices	NO. Of IO's	Delay in ns.
Vedic complex	84	147	33	18.41
Booth's complex	100	174	33	19.66

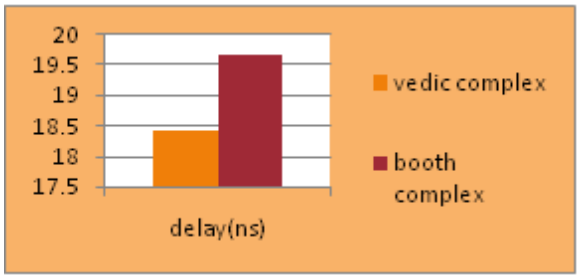

Figure5:Comparison of 4 bit Multipliers with respect to delay

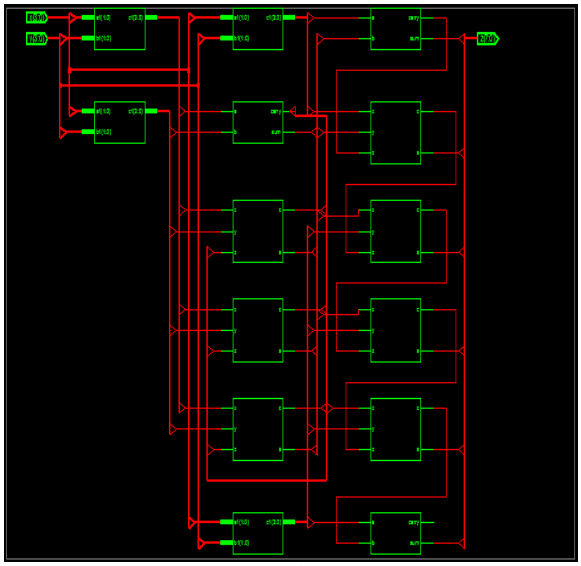

Figure 6: RTL schematic of Vedic complex multiplier.

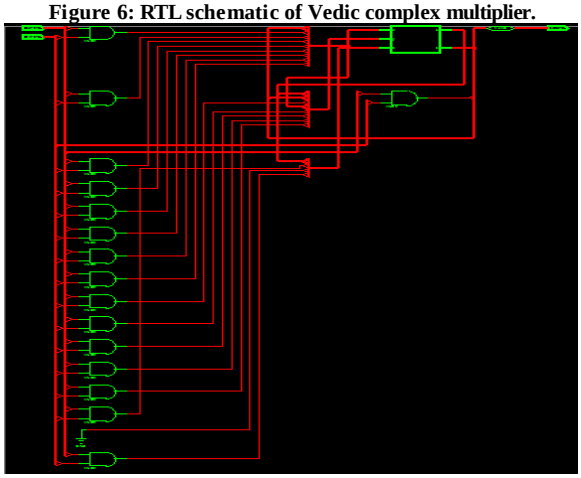

Figure 7: RTL schematic of Booth's complex multiplier.

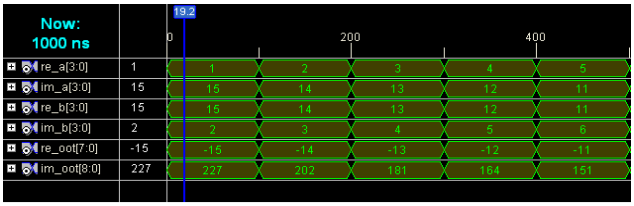

Figure8:Simulation waveforms for 4-bit complex multiplication (Vedic)

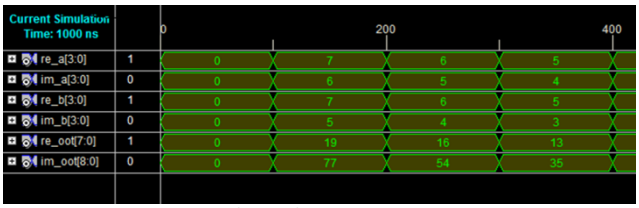

Figure9:Simulation waveforms for 4-bit complex multiplication (Booth's)

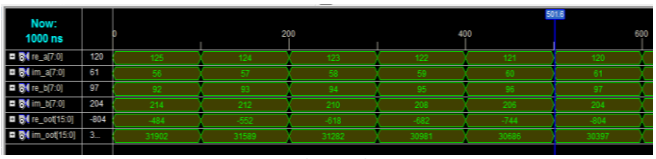

Figure10:Simulation waveforms for 8-bit complex multiplication (Vedic)

TABLE II:
DEVICE UTILIZATION SUMMARY

Vedic Complex Multiplier	NO. of Slices	NO. of 4 input Slices	NO. Of IO's	Delay in ns.
4x4	84	147	33	18.41
8x8	385	674	64	30.90

V. EXPERIMENTAL RESULTS

The work presented in this paper was implemented using VHDL and logic simulation was done using Xilinx ISE simulator and synthesis was done using Xilinx project navigator. The design was synthesized for Spartan3 (xc3s200-5-ft256) device. The obtained results are presented in table 1, and waveforms for 4-bit complex multiplication using Urdhva Tiryakbhyam and Booth's algorithm is shown in figure 8 & 9 respectively. The device utilization in case of Vedic complex is less (No. of Slices: 84 out of 1920 - 4%, Number of 4 input LUTs: 147 out of 3840 - 3%, Number of bonded IOBs: 33 out of 173 - 19%) compared to Booth's complex (No. of Slices: 100 out of 1920 - 5%, Number of 4 input LUTs: 174 out of 3840 - 4%, Number of bonded IOBs: 33 out of 173 - 19%). The delay required by Vedic complex multiplier is 18.41 ns, while it is 19.66 ns for Booth's complex. The device utilization in case of Vedic complex is less (No. of Slices: 385 out of 1920 - 20%, Number of 4

input LUTs: 674 out of 3840 - 17%, Number of bonded IOBs: 66 out of 173 - 36%)

Vedic complex multiplier has the greatest advantage as compared to other complex multipliers over gate delays and regularity of structures. The results also suggest that Vedic complex multiplier is faster than other complex multipliers and thus this is extremely advantageous.

VI. CONCLUSION

Vedic Mathematics gives us a clue of symmetric computation. Vedic mathematics deals with various topics of mathematics such as basic arithmetic, geometry, trigonometry, calculus etc. All these methods are very efficient as far as manual calculations are concerned. The proposed Vedic complex multiplier proves to be highly efficient in terms of the speed. The main advantage is delay increases slowly as the input bits increases. Most of the important DSP algorithms, such as convolution, discrete Fourier transforms, fast Fourier transforms, digital filters. Since the multiplication time is generally far greater than the addition time, the total processing time for any DSP algorithm primarily depends upon the number of multiplications. Hence, this multiplier can be used to implement the above DSP algorithms.

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