International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622
International Conference On Industrial Automation And Computing (ICIAC- 12-13 April 2014))

RESEARCH ARTICLE OPEN ACCESS

Design of 8 Bit Vedic Multiplier for Real & Complex Numbers Using VHDL

Mr.Swaroop A. Gandewar1, Prof. Mamta Sarde2
Mtech. Department of Electronics (Communication), Abha Gaikwad-Patil College Of Engineering, Nagpur
Email: sagandewar@gmail.com
Asst. Professor, Mtech. Department of Electronics (Communication), Abha Gaikwad-Patil College Of Engineering,Nagpur
Email: mmsarde@gmail.com

ABSTRACT
This paper proposed the design of 8 Bit Vedic Multiplier using the techniques of Ancient Indian Vedic Mathematics that have been modified to improve performance. Vedic Mathematics is the ancient system of mathematics which has a unique technique of calculations based on 16 Sutras. The work has proved the efficiency of Urdhva tiryakbhyam – Vedic method for multiplication which strikes a difference in the actual process of multiplication itself. It enables parallel generation of intermediate products, eliminates unwanted multiplication steps with zeros and scaled to higher bit levels. So the design complexity gets reduced for inputs of larger no of bits and modularity gets increased. The proposed Vedic multiplier is coded in VHDL (Very High Speed Integrated Circuits Hardware Description Language), synthesized and simulated using EDA (Electronic Design Automation) tool – Xilinx9.1i The main design features of the proposed system are the reconfigurability and flexibility
Keywords **-** EDA , Urdhva tiryakbhyam, Vedic multiplier, VHDL

I. INTRODUCTION

Vedic mathematics[2] is the name given to the ancient system of mathematics, or, to be precise, a unique technique of calculations based on simple rules and principles with which any mathematical problem can be solved – be it arithmetic, algebra, geometry or trigonometry. The system is based on 16 Vedic *sutras* or aphorisms, which are actually word formulae describing natural ways of solving a whole range of mathematical problems. Vedic mathematics was rediscovered from the ancient Indian scriptures between 1911 and 1918 by Sri Bharati Krishna Tirthaji (1884- 1960), a scholar of Sanskrit, mathematics, history and philosophy [1]. He studied these ancient texts for years and, after careful investigation, was able to reconstruct a series of mathematical formulae called *sutras*. Bharati Krishna Tirthaji, who was also the former Shankaracharya (major religious leader) of Puri, India, delved into the ancient Vedic texts and established the techniques of this system in his pioneering work, *Vedic Mathematics* (1965), which is considered the starting point for all work on Vedic mathematics. According to Mahesh Yogi, *The* sutras *of Vedic Mathematics are the software for the cosmic computer that runs this universe*. A great deal of research is also being carried out on how to develop more powerful and easy applications of the Vedic *sutras* in geometry, calculus and computing. Conventional mathematics is an integral part of engineering education since most engineering system designs are based on various mathematical approaches. The need for faster processing speed is continuously driving major improvements in processor technologies, as well as the search for new algorithms. A multiplier is one of the key hardware blocks in most digital signal processing systems. With advances in technology, many researchers have tried to design multipliers which offer either of the following- high speed, low power consumption, regularity of layout and hence less area or even combination of them in multiplier. The Vedic mathematics approach is totally different and considered very close to the way a human mind works. In this work, we try to present multiplication operations and the implementation of these using both conventional, as well as Vedic mathematical methods in VHDL language [1].

II. THE VEDIC MULTIPLICATION METHOD

The proposed Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed

algorithm compatible with the digital hardware. Vedic multiplication based on Urdhava Tiryakbhyam

2.1 Urdhava Tiryakbhyam sutra:

The proposed Vedic multiplier is based on the "Urdhva Tiryagbhyam" sutra (algorithm). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. It is a general multiplication formula applicable to all cases of multiplication. It literally means "*Vertically and Crosswise*". It is based on a novel concept through which the generation of all partial products can be done with the concurrent addition of these partial products. The algorithm can be generalized for n x n bit number. Since the partial products and their sums are calculated in parallel, the multiplier is independent of the clock frequency of the processor. Due to its regular structure, it can be easily layout in microprocessors and designers can easily circumvent these problems to avoid catastrophic device failures. The processing power of multiplier can easily be increased by increasing the input and output data bus widths since it has a quite a regular structure. Due to its regular structure, it can be easily layout in a silicon chip. The Multiplier based on this sutra has the advantage that as the number of bits increases, gate delay and area increases very slowly as compared to other conventional multipliers

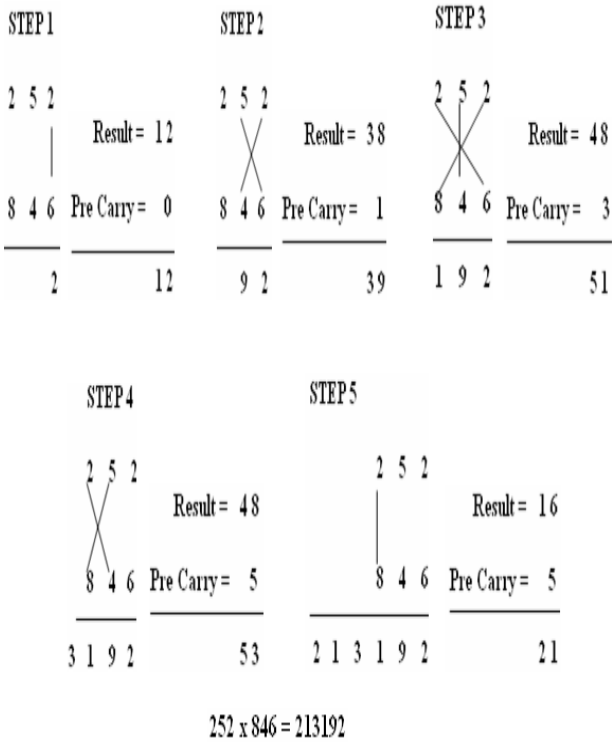

Fig. 1 Multiplication of two decimal numbers – 252 x 846

Algorithm for 8 X 8 Bit Multiplication Using Urdhava Tiryakbhyam (Vertically and crosswise) for two Binary numbers [8]-

A = A7A6A5A4 A3A2A1A0
X1 X0
B = B7B6B5B4 B3B2B1B0
Y1 Y0
X1 X0
* Y1 Y0

F E D C
CP = X0 * Y0 = C
CP = X1 * Y0 + X0 * Y1 = D
CP = X1 * Y1 = E
Where CP = Cross Product

To illustrate the multiplication algorithm, let us consider the multiplication of two binary numbers a3a2a1a0 and b3b2b1b0. As the result of this multiplication would be more than 4 bits, we express it as... r3r2r1r0. Line diagram for multiplication of two 4- bit numbers is shown in Figure 2 which is nothing but the mapping of the Figure 1 in binary system. For the simplicity, each bit is represented by a circle. Least significant bit r0 is obtained by multiplying the least significant bits of the multiplicand and the multiplier

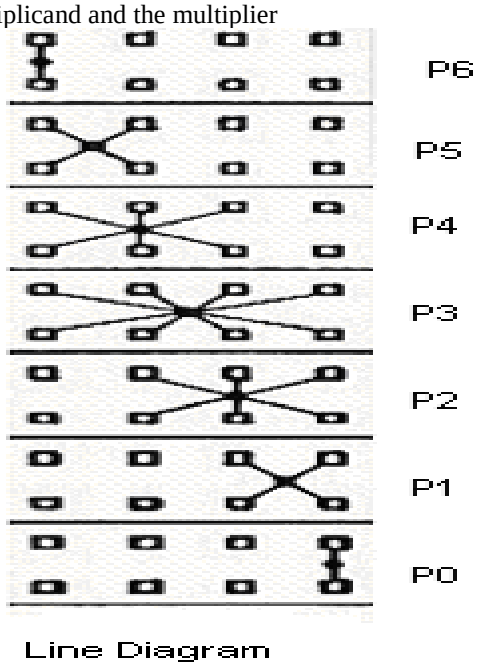

Figure 2 Line Diagram

Firstly, least significant bits are multiplied which gives the least significant bit of the product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the product and the carry is added in the output of next stage sum obtained by the crosswise and vertical multiplication and addition of three bits

of the two numbers from least significant position. Next, all the four bits are processed with crosswise multiplication and addition to give the sum and carry. The sum is the corresponding bit of the product and the carry is again added to the next stage multiplication and addition of three bits except the LSB. The same operation continues until the multiplication of the two MSBs to give the MSB of the product. For example, if in some intermediate step, we get 110, then 0 will act as result bit (referred as rn) and 11 as the carry (referred as cn). It should be clearly noted that cn may be a multi-bit number Thus we get the following expressions:

r0=a0b0*;* (1)
c1r1=a1b0+a0b1*;* (2)
c2r2=c1+a2b0+a1b1 + a0b2*;* (3)
c3r3=c2+a3b0+a2b1 + a1b2 + a0b3*;* (4)
c4r4=c3+a3b1+a2b2 + a1b3*;* (5)
c5r5=c4+a3b2+a2b3*;* (6)
c6r6=c5+a3b3 (7)

With c6r6r5r4r3r2r1r0 being the final product. Hence this is the general mathematical formula applicable to all cases of multiplication. The hardware realization of a 4-bit multiplier is shown in Figure 3. This hardware design is very similar to that of the famous array multiplier where an array of adders is required to arrive at the final product. All the partial products are calculated in parallel and the delay associated is mainly the time taken by the carry to propagate through the adders which form the multiplication array

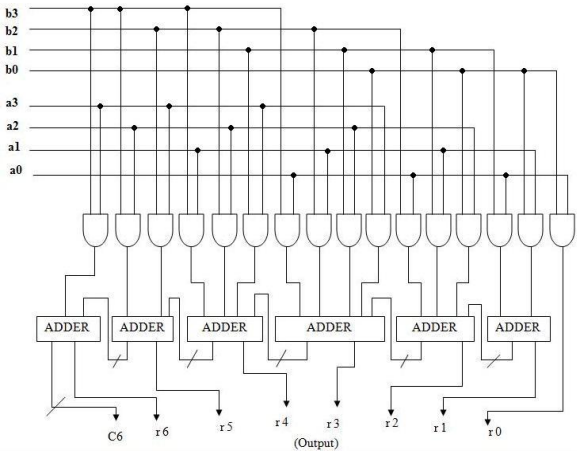

Figure 3: Hardware architecture of the Urdhava tiryakbhyam multiplier. [6]

III. Design & Synthesis of Vedic Multiplier

The Vedic multiplier is implemented using VHDL. The functional verification through simulation of the VHDL code was carried out using ModelSim SE 6.0 simulator. The entire code is completely synthesizable. Xilinx ISE 9.1i Tool has been used for design and testing various multiplier implementations. Design entered in the form of VHDL code. Various simulations are done for early testing. Input has been given through a text file.

Generalized Algorithm for N x N bit Vedic Multiplier

We can generalize the method as discussed in the previous sections for any number of bits in input. Let, the multiplication of two N-bit binary numbers (where N = 1, 2, 3…N, mustformbeof2 ^{N})in *A* and *B* the where A = A_N.....A_3

A A and B = B ….B B . The final multiplication result 2 1 N 3 2 1

will be of (N + N) bits as S = $S_{(N+N)}$....S_3 S_2 S_1.

Step 1: Divide the multiplicand A and multiplier B into two equal parts, each consisting of [N to (N/2)+1] bits and [N/2 to 1] bits respectively, where first part indicates the MSB and other represents LSB.

Step 2: Represent the parts of A as A_M and A_L, and parts of B as B_M and B_L. Now represent A and B as A_M A_L and B_M B_L respectively.

Step 3: ***For A X B, we have general format as shown in Fig.4***

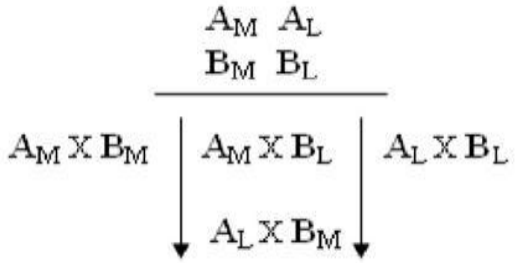

Fig.4. General format of vedic multiplication

IV. Vedic Multiplier for 8x8 bit Module

The 8x8 bit Vedic multiplier module as shown in the block diagram in Fig. 5 can be easily implemented by using four 4x4 bit Vedic multiplier modules as discussed in the previous Section multiplications,

A_3 A_2 A_1 A_0 and B= B_7 B_6 B5B_4 B_3 B_2 $B_1$$B_0$. The output line for the multiplication result will be of 16 bits as –S_{15} S_{14} S_{13} S_{12} S_{11} S_{10} S_9 S_8 S_7 $S_{6b}$$S_5$$S_4$ S_3 S_2 S_1 S_0.

Lets divide A and B into two parts, say the 8 bit multiplicand A can be decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as: decomposed into pair of 4 bits AH-AL. Similarly multiplicand B can be decomposed into BH-BL. The 16 bit product can be written as:

Using the fundamental of Vedic multiplication, taking four bits at a time and using 4 bit multiplier block as discussed we can perform the multiplication. The outputs of 4x4 bit multipliers are added accordingly to obtain the final product. Here total

three 8 bit Ripple-Carry Adders are required as shown in Fig. 5.

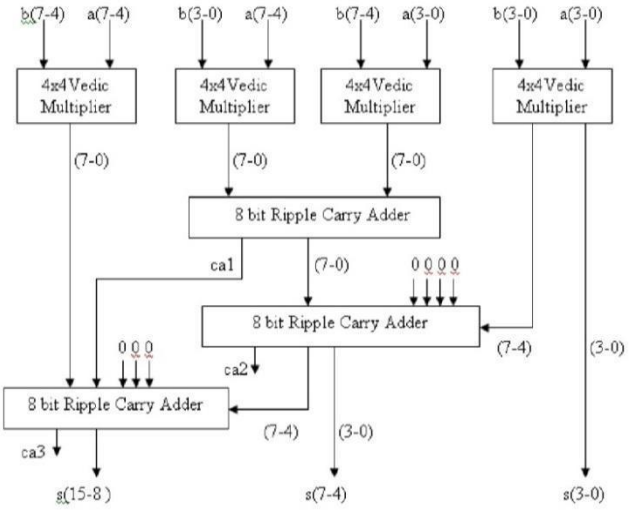

Fig. 5 Block Diagram of 8x8 bit Vedic Multiplier

V. CONCLUSION

This paper presents a highly efficient method of multiplication – "Urdhva Tiryakbhyama" based Sutra on Vedic mathematics. It is a method for hierarchical multiplier design which clearly indicates the computational advantages offered by Vedic methods. The computational path delay for proposed 8x8 bit Vedic multiplier is found to be 28.27 ns. It is observed that the Vedic multiplier is much more efficient than Array and Booth multiplier in terms of execution time (speed). An awareness of Vedic mathematics can be effectively increased if it is included in engineering education

V. Results

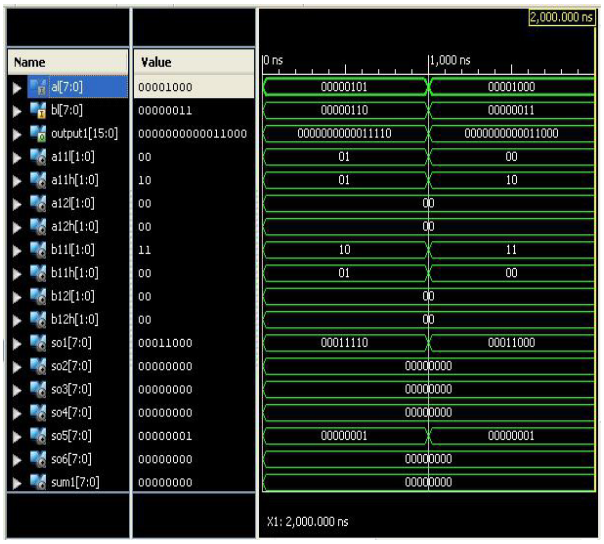

Fig.6. Simulation Result of 8x8 bit Vedic Multiplier (5X6=30 & 8x3=24)

REFERENCES

[1] J. S. S. B. K. T. Maharaja, Vedic mathematics, Delhi: Motilal Banarsidass Publishers Pvt Ltd,(2010).

[2] Pavan Kumar,A.Radhika, "FPGA Implementation of high speed 8-bit Vedic multiplier using barrel shifter", 2013 IEEE Paper

[3] M.Nagaraju, R.Surya Prakash, B.Vijay Bhaskar "High Speed ASIC Design of Complex Multiplier using Vedic Mathematics"International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 3, Issue 1, January -February 2013, pp.1079-1084

[4] Pushpalata Verma, K. K. Mehta, "Implementation of an Efficient Multiplier based on Vedic mathematics Using EDA Tool"International Journal of Engineering and Advanced Technology (IJEAT) ISSN: 2249 – 8958, Volume-1, Issue-5, June 2012

[5] Prabir Saha, Arindam Banerjee, Partha Bhattacharyya, Anup Dandapat, "High speed ASIC design of complex multiplier using vedic mathematics" , Proceeding of the 2011 IEEE Students' Technology Symposium 14-16 January, 2011, lIT Kharagpur, pp. 237-241.

[6] Shamsiah Suhaili and Othman Sidek, "Design and implementation of reconfigurable alu on FPGA", **3**rd International Conference on Electrical & Computer Engineering ICECE 2004, 28-30 December 2004, Dhaka, Bangladesh, pp.56-59

[7] Parth Mehta, Dhanashri Gawali "Conventional versus Vedic mathematical method for Hardware implementation of a multiplier", 2009 International Conference on Advances in Computing, Control, and Telecommunication Technologies

[8] Poornima M, Shivaraj Kumar Patil, Shivukumar , Shridhar K P , Sanjay H "Implementation of Multiplier using Vedic Algorithm "International Journal of Innovative Technology and Exploring Engineering (IJITEE) ISSN: 2278-3075, Volume-2, Issue-6, May 2013 Note that the journal title, volume number and issue number are set in italics.