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Design of complex fuzzy logic arithmetic unit for floating number

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Abstarct
This paper introduces several algorithms and compares the computational complexity first. Second, we introduce two FFT (Fast Fourier Transform) architectures and it includes of pipelined based architecture and memory based architecture. Because we cost a lot of area size in multiplication, we reduce the multiplication in each stage. And then we use the CORDIC (Coordinate Rotation Digital Computer) operator to reduce the computation of twiddle factor.

I. Introduction

FPGAs (Field Programmable Gate Arrays) are among the most popular types of ASICs. In SRAM-based FP-GAs, which are the focus of this paper, any k-input Boolean function is implemented by using 2k bits of look-up table.

The majority of technology mapping methods are de-signed to map a Boolean network into the XILINX XC3000 FPGA circuit structure, where each CLB has 25 bits of SRAM LUT capable of implementing Boolean ex-pressions with up to inputs. As the FPGAs has become more popular, the FPGA architecture has evolved. In the new SRAM-based FPGA architectures, such as XILINX AT&T's ORCA [5], a configuration of a single CLB becomes more difficult to use.

For example, some substantial limitations are imposed on the mapping procedure for XILINX XC4000 FPGAs. Two of three inputs to the upper-level look-up table (H-LUT) should be outputs of the lower-level look-up table. The second important restriction is that only two outputs are allowed in one CLB, either directly or via ip ops. Restrictions mentioned above limit direct applicability and e ciency of the many previously developed algorithms to this new architecture.

In this paper the MOFL (Multi-criteria Optimization using to the set, where X is a set But fuzzy sets are di erent from classical sets in that they allow partial or gradual degrees of membership. A fuzzy set A over X is de ned as a set of ordered pairs:

Fuzzy Logic) technology mapping algorithm for complex CLB structures, particularly for the XILINX XC4000 family of FPGAs, is introduced. The input to the MOFL technology mapping procedure is a DAG of Boolean expressions. Prior to the technology mapping, the SIS logic optimizer is applied to logic input.

The proposed algorithm utilizes memory resources of CLBs in order to obtain better timing performance with-out sacri cing area.

Most of the known mapping algorithms [4], [3], are based on decomposition of the input network, presented usually in a graph form, into a set of fanout-free trees or a set of small pieces of graphs. When the network is de-composed into a set of trees, a technology mapper loses the exibility of mapping over the boundaries of trees. The proposed technology mapper does not decompose the DAG network into trees but directly uses the graph as a source structure for the technology mapping algorithm to retain exibility in optimizing delays.

This paper presents parallel hardware implementationsofinterval type-2 FLC for the purpose control which canaccommodate much larger rule bases than the previous hardware implementations mentioned above. This will create bespoke co-processors that can perform functions such as fuzzification and type reduction. The proposed system iscurrently utilised as part of a larger embedded Interval Type- Fuzzy Engine

Management System Numerous timing comparisons were undertaken between theco-processors and equivalent sequential floating implementations

II. Background of fuzzy logic

A classical (crisp) set is normally de ned as a collection of elements or objects. For a given set A X, each element x 2 X either belongs to the set or does not belong

$$\tilde{A} = f(x; \tilde{A}(x)) \; j \; x \; 2 \; Xg;$$

where $\tilde{A}(x)$ is a membership function which associates with every member x of X a number in the interval [0,1],

representing the degree of membership of x in A.

To represent fuzzy sets, linguistic variables are generally used [8]. The values of linguistic variables are not numbers but words or sentences in a natural or arti cial language. For example \age" is a linguistic variable whose values can be \young", \old", \very old" and so on. Fig. 2 represents an example of membership function \young" de ned graphically for the linguistic variable \age".

Fuzzy decisions are made using plain language rules describing relations between linguistic variables and thier values de ned by membership functions. Rules are stated in a simple IF/THEN format and input values can be combined using and or or operations. Min and max are most commonly used functions for fuzzy intersection (and) and union (or) operators, but other functions were also proposed [15] for more sophisticated applications. (See Sec. III.A)

III. Multi-criteria Optimization Using Fuzzy Logic

In many cases, solutions of engineering problems re-quire an achievement of several goals simultaneously. In FPGA mapping, there are several objectives to be achieved: area, delay, routability and others. All these objectives can not be opmitized in the same time, be-cause they may contradict to each other. Thus, the best compromise for multiple objectives is a solution which balances them.

The multi-criteria optimization problem can be pre-sented as selection of x 2 X which optimizes the decision

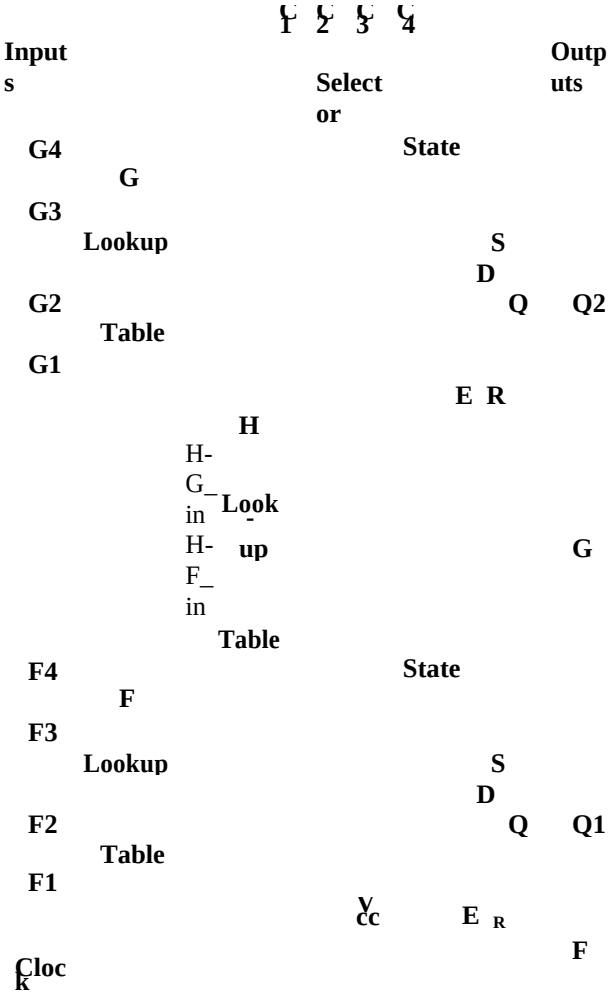
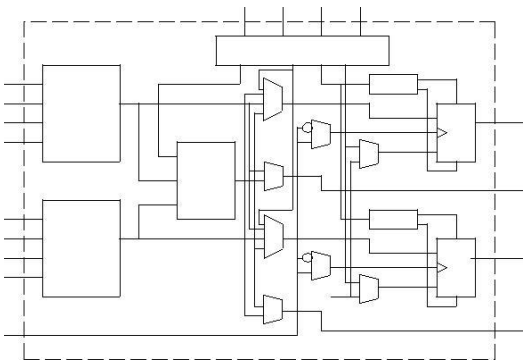


Fig. 1. The architecture of XC4000 FPGA CLB young 1



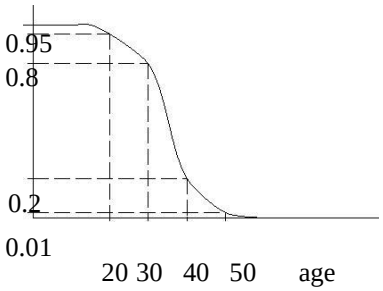


Fig. 2. Membership function \young" for the linguistic variable \age"

function D(x)

D(x) = f(C1 (x); C2(x); ; Cn(x)

where X is a solution space and Ci's are criteria de ned over the set X.

In the proposed MOFL system, the multi-criteria op-timization procedures are used for selection of nodes to be mapped into each CLB. The decision function D(x) is implemented by a multilevel function of fuzzy logic oper- ators de ned by fuzzy rules. Fuzzy logic model is selected because classical models are poorly suited for a solution with multiple criteria and varying degrees of importance of di erent objectives during design process.

In the following subsections, fuzzy logic operators used in this work and the methodology of balancing multiple criteria of varying importance are described in detail.

I. Application

The decision-making process can be represented in fuzzy logic form by a set of some rules, which include combinations of and and or operators. Such representa-tion allows to re ect complex interactions between goals in decision-making.

In many fuzzy logic applications, min and max opera-tors have been used as fuzzy intersection (and) and union (or). But min and max are not the only possible opera-tors to model intersection and union. The operators in fuzzy logic are divided into two categories: compensatory operators and non-compensatory operat ***Fuzzy logic decision making procedure***

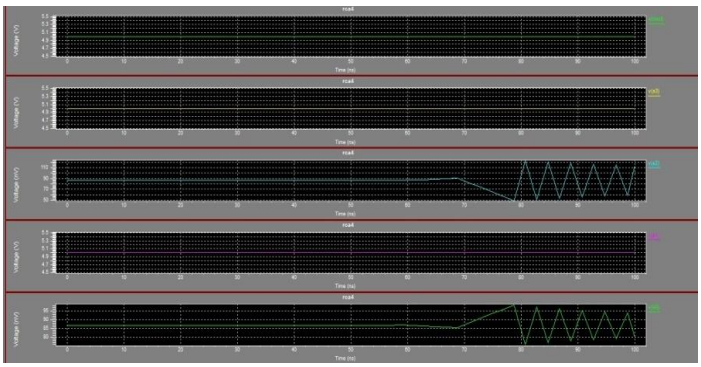
Example of Hierarchical FZDM: Fig. ***8*** illustrates a hierarchical FZDM. In this and other FZDM's described below, each block represents a linguistic value and is implemented as an OOP object.Depending on the context, a linguistic value can be either an objective or a criterion that is used to define an objective. For example, linguistic value ***5*** can be the objective ***good placement,*** linguistic value **y** can be the criterion ***strong connectivity to partial placement*** and linguistic value *z* can be the criterion ***almost within a feasible interval.*** Fuzzy logic.

Practicle Aspects

The proposed MOFL technology mapper was imple-mented with approximately 7000 lines of C code. In order to demonstrate performance of the mapper, 25 benchmark circuits were selected from the set of MCNC test cases. All test cases were chosen from the combinational multi-level examples.

XILINX's FPGA development system, called XACT, includes various subsystems such as FPGA design edi-tor, technology mapper, placement and routing system, timing analyzer and others. Among them, the Partition, Placement, and Route (PPR) program performs technol-ogy mapping and layout for the XILINX XC4000 series FPGAs. It was observed that the updated version of the XILINX mapper emphasised routability and timing per-formance rather than area. It does not pack CLBs as tightly as possible to improve routability and timing.

For the 25 test cases, the MOFL technology mapper used on average 2.3% more CLBs than XILINX. In con-trast, the number of maximal CLB levels was reduced by 27.7%, which resulted in 11.6% reduction of the max-imal delay of circuits after layout. The di erence be-tween ratios of reduction in numbers of levels and delay is mainly due to input and output circuitry, which is inde-pendent of the technology mapping procedure. Run time for the MOFL mapper does not exceed the run time of the XILINX mapper.



CONCLUSION

This paper presents characterization, justification, classification of fuzzy logic-based CAD tools for digital design. It is demonstrated that application of fuzzy logic is beneficial on all

hierarchical levels of the design process. It allows to merge traditional numeric techniques with the domain information available in the linguistic form and, as a result, to improve quality of design solutions. Fuzzy logic structures are shown to be used in constructive and iterative procedures. Short descriptions of several tools are accompanied by the experimental data and comparison of design solutions is obtained by different tools for popular benchmark

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