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16-Bit Arithmetic And Logic Unit Design Using Mixed Type of Modeling In VHDL

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Abstract
This paper explains the design and implementation of 16-bit ALU (arithmetic and logic unit) using VHDL by using mixed style of modeling in Xilinx ISE 8.1i. The ALU takes two16-bits numbers and performs different principal arithmetic and logic operations like addition, multiplication, logical AND, OR, XOR, XNOR. The major focus of concern in this ALU is the multiplication operation using radix-4 booth algorithm and bit-pair recording technique which increases the speed of multiplication operation. We had followed modular programming approach so that our ALU is sub divided into smaller logical block. All the modules in arithmetic and logical unit design are realized using VHDL design[1]. The top level design consists of arithmetic unit and logic unit which is implemented by using mixed type of modeling. Designing of this ALU is done by using VHDL and simulated using Xilinx ISE 8.1i[1].

I.   Introduction

The main aim of our paper is to design a 16 bit Arithmetic Logic Unit which is a digital circuit that performs arithmetic and logical operations using VHDL[5]. The ALU is a key block of the central processing unit (CPU) of a many system. Field Programmable Logic Arrays (FPGAs) have been growing at a rapid rate in the past few years. FPGA [2] is a special type of logic chip that can be programmed which supports thousand of gates and provide flexibility and low cost which is suitable for implementing a prototype system. The existence of CAD software to support FPGAs has grown in sophistication and it makes most user designs are now complete system and go to production as an FPGA. This paper will discuss on FPGA design style using a 16-bit ALU as design hardware. Generally, the methods that used to implement the 16-bit ALU are using schematic based entry and VHDL based entry. Implementation of 16-bit ALU using VHDL includes a mixed type of description. The top level

of design is using a schematic based entry. Finally this paper will discuss the methods that are used in designing the 16-bit A L U in term of the flexibility, area consumption and timing analysis. The analysis will give the user more understanding in designing digital system using FPGA design style and give them a choice which depends on the design requirements. [2]
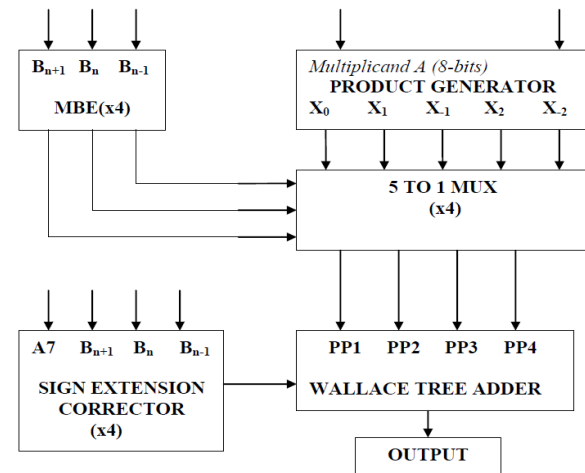
II.   Design Of 16bit- ALU.

When designing the ALU we will follow the principle "Divide and conquer" in order to use modules, some of which can be re-used. An Arithmetic unit does the following task: Addition, Addition with carry. Now first of all we start with making one bit Full Adder, then a 4-bit Carry look ahead Adder using four numbers of Full Adder and at last a 16-bit Carry look
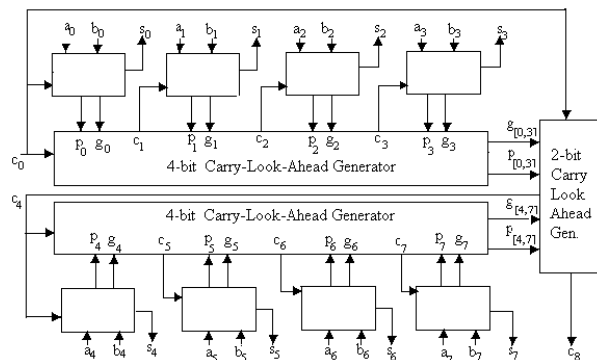
III.   Architecture Of 16bit-ALU

The proposed 16-bit ALU consists of one arithmetic unit and logic unit. Using the principle

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of regularity, the arithmetic unit is divided into different blocks which perform the operations such as: addition & multiplication. But, the main focus of concern in this arithmetic unit is on addition & multiplier unit. We have used carry look ahead adder for addition because Carry Look Ahead Adder is in between the spectrum of all adders, having a proper tradeoff between time and area complexities, and for multiplication we use Radix-4 Booth algorithm and bit pair recording techniques.

The reason for choosing this technique is to Boost up the speed of 16-bit ALU. Similarly, the logic unit is also divided into various blocks which perform the operations such as: AND, OR, XOR, XNOR,

"Figure1 8-Bit Carry Look Ahead Generator (Using 2-Bit CLA)."

Complexity and propagation Delay for n-bit Carry Look Ahead structure
$A_{CLA} = O(n) = 14n$
$T_{CLA} = O(\log n) = 4 \log 2n$.

IV. Multiplier Unit

Booth Multiplication Algorithm (Radix – 4)[4] One of the solutions realizing high speed multipliers is to enhance parallelism which helps in decreasing the number of subsequent calculation stages. The previous version of Booth's multiplier (Radix – 2) had two drawbacks[6].

a) The number of add / subtract operations became variable and hence became inconvenient while designing Parallel multipliers

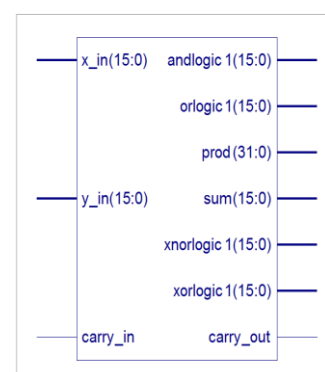b) The Algorithm becomes inefficient when there are isolated 1s.

This problem is bypass by using Radix 4 Booth's Algorithm which can scan strings of three bits with the algorithm given below[3].
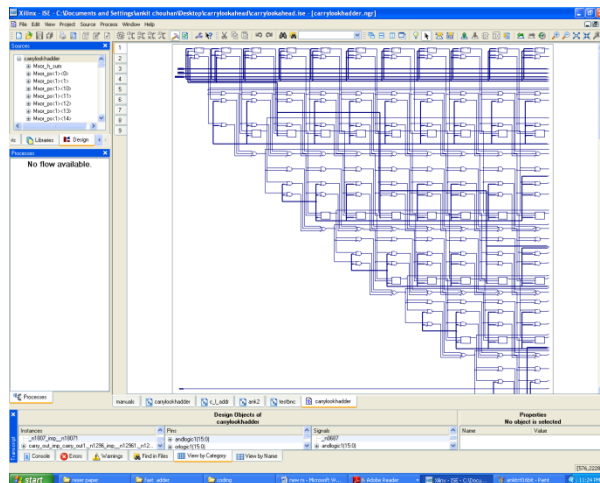

"Figure2 -Architecture of designed Booth Multiplier in the Paper."

"Table 1. Radix-4 recoding"

Quartet value	Signed digit value
000	0Y
001	+1Y
010	+1Y
011	+2Y
100	-2Y
101	-1Y
110	-1Y
111	0

V. Synthesis Result

5.1 RTL view

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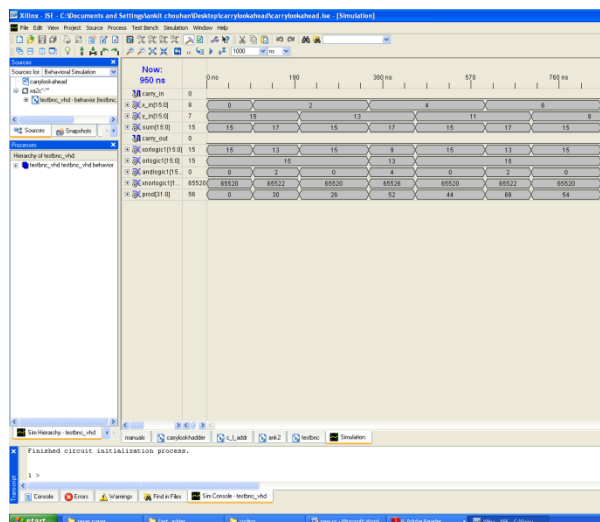*(ICETMEE- 13th-14th March 2014)*

5.2 Technology View

VI.   Simulation

Behavioral simulation is shown below

VII.   FPGA Design Entry

The ST102 has been designed specifically to work with Xilinx ISE CAD tools including the free Web pack tools available from the Xilinx website. The low cost standard expansion connectors allow new peripheral board, including wire-wrap or manually soldered boards to be quickly designed and used. The ST102 board ships with a power supply   so designs can be implemented immediately without the need for any additional cable.[7]   The ST102 board has been designed to offer an unembellished, low cost system for designers who need a flexible platform to gain exposure to the Spartan 2 device, or for those who need to rapidly prototype FPGA-based design. The ST102 board provides only the essential supporting device for the Spartan 2, and

routes all available FPGA signal to standard expansion connectors. Included on the board are 2.5VDC and 3.3VDC regulators, a JTAG configuration circuit that uses a standard parallel cable for programming[9].
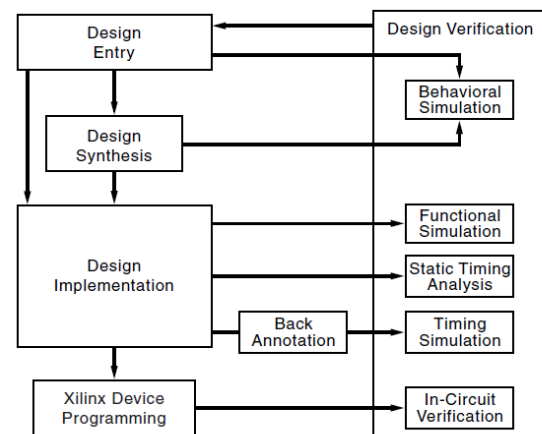

Figure3 -FPGA Design Entry

"Figure4 ST102 Block Diagram"

VIII.   Conclusion

This paper presented a new idea to design 16-bit ALU of a processor. This has been implemented in SPARTAN-3E FPGA device. FPGA design offers greater design flexibility. The design is compact and is upgradable without any change in hardware. Here, the synthesis tool optimizes the design architecture of the FPGA for the ALU. Hence, additional features can be added to the existing design without any changes in hardware. The ALU is synthesized and simulated. The ALU of a processor is configured using each block designed.The main advantage of the proposed 16-bit ALU design is the achievement of increase in the speed of ALU operation so that the time consumption will be reduced. This is because of the fact that the proposed ALU performs the addition by using carry look ahead adder instead of convolution adder & also multiplication operation

is performed by Radix-4 booth algorithm and bit-pair technique which reduces the number of multiplier bits to half (here 16-bit to 8-bit) so that the number of partial products generated will be reduced by a factor of 2 as compared to normal multiplication using general algorithm[8].

Thus the time required to perform the addition of the partial products will be reduced to half so that the speed of multiplication will be enhanced. Therefore, the overall speed of the 16- bit ALU is increased.

References

[1] Rupali Jarwal1, "4-Bit Arithmetic And Logic Unit Design Using Structural Modelling" In VHDL International Journal of Engineering Research & Technology (IJERT) Vol. 2 Issue 3, March – 2013 ISSN: 2278-0181

[2} Mohd Zin , Rosnah, "Analysis of FPGA design methods using AN 8 Bit ALU" Masters thesis, Kolej Universiti Teknologi Tun Hussein Onn.

[3} M.Jayaprakash, "Design and Analysis of Low Power and Area Efficient Multiplier" International Journal of Electrical, Electronics and Mechanical Controls ISSN (Online) : 2319-7501 Volume 3 Issue 1 January 2014 Manuscript ID : ISSN23197501-V3I1M2-012014 suggestion for fast multipliers," IEEE Trans. Electron. Comput., Feb. 1964.

[4] A.D. Booth, "A signed binary multiplication technique," Quarterly J. Mechan. Appl. Math., vol IV. Part 2, 1951.

[5] O.L. MacSorley, "High speed arithmetic in binary computers," Proc. IRE, Jan. 1961.

[6] H. Sam y A. Gupta, "A generalized multibit recoding of two's complement binary numbers and its proof with application in multiplier implementations," IEEE Trans. Comput., Aug. 1990, pp.1006-1015.

[7] Kanika Kaur, "Implementation Of Alu Using Fpga" International Journal of Emerging Trends & Technology in Computer Science (IJETTCS)
Volume 1, Issue 2, July – August 2012 ISSN 2278-6856

[8] Paresh Kumar Pasayat "FPGA based implementation of 8-bit ALU of a RISC processor using Booth algorithm written in VHDL language"
International Journal of Engineering Research & Technology (IJERT) Vol. 2 Issue 8, August – 2013

[9] Scientech Technologies Pvt. Ltd. Lab manual of VLSI Trainer ST102.