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A Review on an Efficient Architecture of Pipeline ADC for High Speed Applications

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ABSTRACT
Most of the high computing applications today use ADC (Analog to Digital converters) to convert the transmitted information. While converting a data from A-to-D or D-to-A creates multiple problems when signals are represents in digital. This paper presents a review of the most popular types of Analog to Digital converters like, direct conversion (Flash) ADC, pipelined ADC, successive-approximation resister (SAR) ADC, and sigma delta ADC. In the conversion process some parameters like resolution, conversion rate, quantization error, signal to noise ratio (SNR), spurious-free dynamic range (SFDR), dynamic range (DR) and effective number of bits (ENOB). The performance of the ADC is measured by differential Non-linearity error (DNL), Integrated Non linearity error (INL) and quantization error which are also defined. The main focus here is to compare between different types of ADC.
Keywords - VLSI, Integral Non Linearity, Differential Non Linearity, Pipeline ADC, SNR, DDC, PCM, Residue amplifier.

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I. INTRODUCTION

In their normal state, Sequence carrying variables like voltage, current, charge, temperature and pressure are contained by analog structure. On the other hand, used for processing, transmission and storage purposes, it is frequently further convenient to represent information in digital shape. An opamp circuit is required to produce a signal voltage in the range of 0v to 1v with an accuracy of 1mv or 0.1%. The effects of component non-idealities, drift, aging, noise and imperfect wires and interconnections, even moderate accuracy requirement may be difficult to meet. A suitable conditioning in an analog input signal, is A-to-D conversion [1] is processed in digital form by the processor block. Once processed, signal is D-to-A converted and reused in analog form. The A-D converter be operated at a speed of fs samples per second. To keep away from any aliasing phenomenon, the analog input must be band restricted so that its maximum frequency component is less than fs/2. The ADC input [2] is held stable through the translation process, indicating that the ADC must be preceded by sample and hold amplifier [5] to freeze the band limited signal is immediately prior to each conversion. The D-to-A converter is operated at the equal speed fs of the ADC; it is equipped with appropriate circuitry to eliminate any output glitches arising in connection through input code changes. The staircase filter is used to ease the effects of quantization noise. In various high computing applications like Digital signal processing (DSP), direct digital control (DDC), digital audio mixing, recording and play back, pulse-code modulation (PCM) communication, data acquisition, computer music and video synthesis and digital multimeter instrumentation.

II. PERFORMANCE SPECIFICATIONS

A digital converter shows various parameters, which makes huge impact on the performances and computing capabilities [4]. Here is this section an ideal performance of a digital converter is discussed with their mathematical models.

A string of n bits, $b_1\ b_2\ b_3\ \_\ \_\ \_\ b_n$, forms an n-bit word. The quantity 'D' can be represented as $D = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ \ldots\ldots + b_n 2^{-n}\ \ldots\ldots 1$ is called the fractional binary value. Depending on the bit pattern, D can assume 2^n equally spaced values from 0 to $1\text{-}2^{-n}$. The lower limit is reached when all bits are 0, the upper limit when all bits are 1, and the spacing between adjacent values is 2^{-n}.

A/D CONVERTERS (ADCS)

An ADC provides the opposite function of a DAC. An analog input V_I and produces an output word $b_1\ b_2\ \ldots\ b_n$ of fractional value D_0 such that

$$D_0 = b_1 2^{-1} + b_2 2^{-2} + b_3 2^{-3} + \ldots + b_n 2^{-n} = \frac{V_I}{KV_{FSR}} = \frac{V_I}{V_{FSR}} \ldots\ldots\ldots \quad 2$$

an ADC includes two different control pins: the START pin deals about the ADC has to start conversion, and the End of Conversion (EOC)pin is to deals about the conversion is complete. The output code may be in either parallel or serial form. The devices like LCD or LED displays are designed to drive directly through ADCs. The input to an ADC is a transducer signal [7] proportional to the transducer supply voltage V_S, or $V_I = \alpha V_S$ as $D_0 = \alpha V_S/KV_S = \alpha/K$, indicating a reference-independent conversion, called ratiometric conversion. This technique allows for high accurate conversions using references of only modest quality.

The ideal characteristics of a 3-bit ADC with V_{FSR} = 1.0 V. The conversion process isolates the analog input range into 2^n intervals called code ranges. All values of V_I within a given code range are represented by the same code, refers to the midrange value.

III. ADC SPECIFICATIONS

To get a discrete value the analog input is infinite valued quantity and an error will be produced as a result of quantization. This error is recognized as quantization error [9], Q_e, and it is defined as the difference between the actual analog input and the value of the output given in voltage. Quantization error calculated as

$$Q_e = V_{IN} - V_{staircase} \quad \ldots\ldots\ldots\ldots \quad 3$$

and $V_{staircase} = D.\frac{V_{REF}}{2^N} = D.V_{LSB}$ $\ldots\ldots\ldots\ldots$ 4

If Q_e= 0V i.e. Q_e to be between ± ½ LSB,

A. Differential Nonlinearity Error (DNLE)

DNL is defined as the difference between actual code width of a nonideal converter and that of an ideal converter. Therefore,

DNL = Actual width of step – Ideal width of step.

The ideal step width = 1/8 V_{REF}. Therefore,

$$V_{Idealstepwidth} = \frac{1}{8}.V_{REF} = 1\ LSB \quad \ldots\ldots\ldots \quad 5$$

The entire DNL is taken to be ±1LSB and the quantization error is belongs to the DNL [8]. Missing codes data if DNL is >+½ LSB or < – ½ LSB.

B. Integral Nonlinearity Error (INLE)

The integral nonlinearity error is the "best fit" is for first and last code transition straight line is drawn joining the end points. The difference between the ADC code transition points and the straight line is called INL. (Set the other errors are zero).

C. Monotonicity

The converter is monotonic when the analog amplitude level of the converter increases with increasing digital code. The missing output codes will never appears for any analog input signal in a Non-Monotonicity of ADC [12].

$$|INL(k)| \quad \frac{1}{2} \quad LSB \text{ for all } k \quad \ldots\ldots\ldots \quad 6$$

This shows that DNL errors are reduced to 1 LSB or less than one LSB, i.e.

$$|DNL(k)| \quad 1 \quad LSB \text{ for all } k \quad \ldots\ldots\ldots \quad 7$$

The monotonicity is proved from the above expression.

D. Gain And Offset Error

Offset error says that the there is a difference between the value of the first code transition and the ideal value of ½ LSBs. The offset error is a constant value. The quantization error becomes ideal after the initial offset voltage is overcome. The difference in the slope of a straight line drawn through the transfer characteristic and the slope of one of an ideal ADC is Gain error or scale factor error.

E. Signal To Noise Ratio (SNR)

An ADC represents the ratio of the largest RMS input signal to a converter to the RMS value [12] of noise is called signal to noise ratio. It is denoted in dB.

$$SNR = 20\log\left(\frac{V_{in(max)}}{V_{noise}}\right) \quad \ldots\ldots\ldots\ldots \quad 8$$

If the input signal is a sinewave when a peak-to-peak value equal to the full-scale reference voltage of the converter, then the RMS value for

$$V_{in(max)} = \frac{V_{REF}}{2\sqrt{2}} = \frac{2^N(V_{LSB})}{2\sqrt{2}} \quad \ldots\ldots\ldots \quad 9$$

The RMS value of error signal is equal to noise, Q_e

$$Q_{e,RMS} \frac{V_{LSB}}{\sqrt{12}} \quad \ldots\ldots\ldots\ldots \quad 10$$

Therefore, an ideal ADC of a SNR is

$$SNR = 20\ \text{Log}\ \frac{\frac{2^N(V_{LSB})}{2\sqrt{2}}}{Q_{e,RMS}} \quad \ldots\ldots\ldots\ldots \quad 11$$

$$SNR = 6.02N + 1.76 \quad \ldots\ldots\ldots\ldots \quad 12$$

For example, a 12-bit ADC will have an SNR [13] of 74dB.To measure spectrum analyzer is not required. Instead, to examine the data in digital form use Discrete Fourier Transform.

F. Spurious Free Dynamic Range (Sfdr)

The ratio of maximum signal component to the largest distortion component at the output of a data converter is called SFDR. Amplitude spectrum of analog to digital converter output is shown in figure 1.

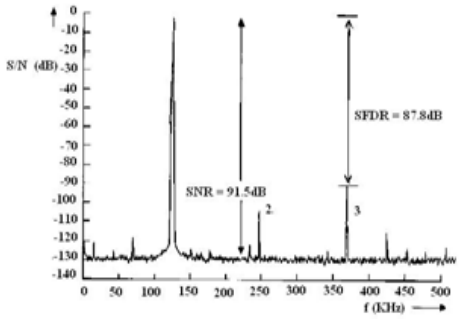

Figure 1: representation of SFDR

When the maximum signal is applied to the converter SFDR is generated. The generated SFDR is measure using spectrum analyzer.

G. Effective Number Of Bits (ENOB)

Nyquist criteria and ENOB are measured for the comparison between converters. ENOB [14] is expressed as

$$\text{ENOB} = \frac{\text{SNR}_{(\text{measued})} - 1.76}{6.02} \quad \ldots\ldots \quad 13$$

ENOB is considered to compare the various architecture of the converter for different performance.

H. Bit Error Rate (BER)

Many steps to be followed while performing the conversion process in ADCs. The defective code is generated during the wrong steps are taken while conversion. Sometimes the ADC results end up with error in output due to metastable state in a comparator (logic level not equal to '1' or '0').BER explains to determine the occurrence of an error in the conversion technique. The reference BER range generally varies between 10^{-10} and 10^{-15}.

I. Figure Of Merit (FoM)

The FoM is used to differentiate between various architectures and their performance of ADCs. The mathematical modeling for Figure of Merit is written as

$$\text{FoM} = \frac{\text{Power}}{2f_{in}\,2^{\text{EOB}}} \text{ and } 2f_{in} \text{ is the Nyquist frequency} \quad 14$$

J. Dynamic Range

The value varies between full scale to the signal which is detected at the minimal level is considered as Signal to noise dynamic range of the respective converter (generally SNDR = 0).

$$\text{DR(dB)} = 10\log\frac{\text{Maximum Signal Power}}{\text{Smallest Signal Power}} \quad \ldots\ldots\ldots\ldots \quad 15$$

IV. Adc Architectures

The conversion speed of an ADC in comparator is limited by time taken to finish the entire conversion. The major difference between the conversion process of flash ADCs and successive approximation ADCs are conversion takes place at a time and conversion for a single bit at time respectively. The major limitation of SAR ADC is delayed conversion because it carries through bit by bit conversion in a sequence but it is easy to design and implement. The flash ADCs design complexity grows exponentially when the same ADCs are used for fast processing. The architectures like pipeline, multistep and folding ADCs follows the conversion methods number of bits at a time though two versatile conditions of flash ADCs. The two factors like circuit complexity and speed of conversion are equally balanced from the flash ADC.

A. Flash Adc

The parallel ADC is known for its fastest speed of operation to complete shorter conversion times. The parallel or flash converter translates the analog signal to digital in one clock cycle. It is the fastest of all converters. The architecture of flash ADC is shown in Figure 2.The reference voltage, V_{REF} is divided in 2^N levels. Both of these values is fed to a comparator and thus needs 2^{N-1} comparators and 2^N resistors. The thermometer code is obtained at the comparator output after comparing the reference voltage with the input voltage. The N bit equivalent digital code is obtained from the priority encoder [14]-[16] by reading a thermometer code.

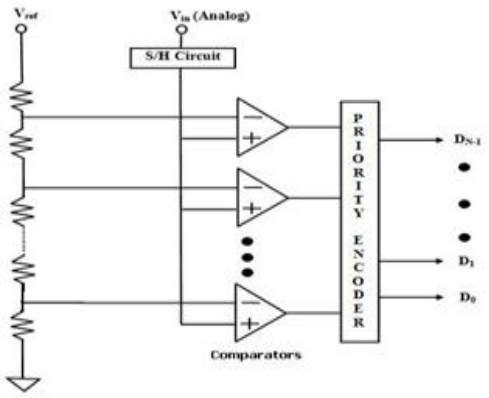

Figure 2: Architecture of Flash ADC

The bipolar conversion can be achieved by connecting a resister string between $+V_{REF}$ and $-V_{REF}$ of the positive and negative analog inputs. The flash ADC is suitable for the 8 bit and lesser resolution, if it increases by one bit the area doubles thereafter. If a 9-bit converter needs511 comparators where a 10-bit ADC needs1023 comparators.

The accuracy of flash ADC is controlled by a various factors like resolution and comparator

offsets along with the reference voltage levels. The performance of conversion is decay as the number of bits increases on the comparator which intern increases the load on the sample and hold circuits. Pipeline and multistep ADCs are constructed with the help of Flash ADCs. Increased power and area consumption is the major limitations of flash ADC.

Errors Sources In Flash Adc

Clock Jitter

Signal to noise ratio in an ADC leads to occur Jitter when there is reduction in sampling rate. Frequencies of large analog inputs are noticed by Jitter. The parameters like sampling clock source and low-jitter impact on getting accurate results on an ADC.

B. Multistep Adc

The n step ADC contains (n-1) blocks of subrange in its architecture. Every multistep ADC consists of a residue amplifier, course ADC and DAC as shown in figure 3. It is possible to complete in single clock cycle by considering the multiphase clock for the entire conversion. The clock difficulties can be avoided in multistep ADC generally by limiting the number of steps not exceeding more than two. This technique can be achieved can be using 2-phase clock scheme.

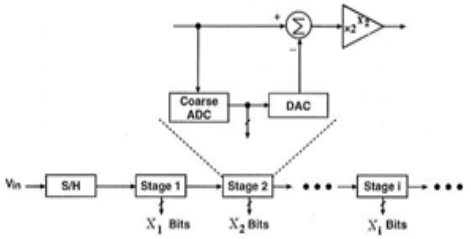

Figure 3: Architecture of multistep ADC

Here the conversion process is used as.

- In first stage the X_1 bits are processed only when the sampling of input is completed.
- The residue is generated after subtracting from the original input and then the bits are converted back to analog form.
- The input is passed to the next stage and multiplies the residue by $2X_1$.
- The unprocessed X_2 bits are obtained from the second stage.

There is a greater reduction in number of comparators used from 2^{N-1} to the $2(2^{N/2}-1)$. Two step flash ADC requires only 30 comparators whereas 255 comparators are required in a general 8-bit Flash ADC.

C. Successive Approximation Adc

SAR ADCs is one of the simplest as compared to other types. This ADC has high resolutions and high speed with minimal area. The SAR ADC follows a simple method of conversion first carries a binary search across all quantization levels and finally merges the output. The architecture of SAR ADC is shown in Figure 4.

The N-bit shift register will indicate start and end of conversion, the bit B_0 to B_{N-1} indicates the status of conversion process. This bits are given to SAR unit where D_{N-1} is initially set to '1' and rest other bits are set to '0s'. The outcome of SAR is converted back to analog using N-bit DAC. When the MSB bit '1' the DAC output becomes $V_{REF}/2$, if V_{IN} greater than $V_{REF}/2$ the comparator output is '1' else it is resets. The above steps repeat until there is an end of conversion indication. It is noted by LSB bit of N-bit shift register is set to '1' and it takes N+1 clock cycle to complete N-bit conversion.

SAR ADCs accuracies are determined from the comparator accuracy and the DAC resolution.

Figure 4: Architecture of Successive Approximation ADC

D. Dual Slope Type Adc

The architectural modifications like simple in structure and linearity makes more popular and finds the wide applications in measuring instruments. The architecture of dual slope ADC [23] is shown in Figure 5.

Dual slope ADC follows the method of conversion when S_2 connect to the V_{REF} if $S_1$is open with respect to the input of opamp.V_M goes high linearly when If V_{REF} is negative for the slope, V_{REF}/R_1C_1.The switch S_2 is connected to input voltage after some time t_1.Then V_M decreases with a slope $-V_M/R_1C_1$. The t_1 and t_2 values are used by the comparator to detect zero crossing time t_2 and ratio will be calculated as t_1/t_2.

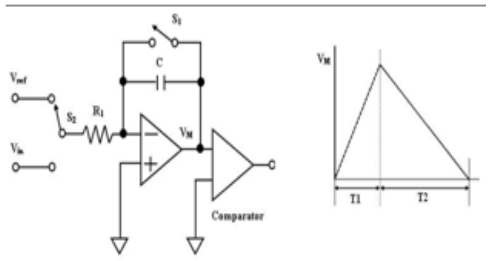

Figure 5: Architecture of dual slope ADC and its Characteristics.

The final digital output of a counter is controlled by the comparator. This method cancels the dependency between R and C the output of comparator controls a counter which finally gives the digital output.

$$\frac{|V_{IN}|}{V_{REF}} = \frac{D}{2^N} \quad \ldots\ldots\ldots\ldots \quad 16$$

Where D- digital output and

N- Number of bits of conversion

E. Pipelined Adc

The architecture of Pipeline ADC is shown in Figure 6. Multistep architecture is similar to Pipeline ADC but sample and hold circuit is employed at every stage of Pipeline ADC [18]. The clock supply is provided to the successive S/H circuits which are operated by alternate clock phases. This leads to residue amplification at every clock phase and carry out the conversion. While the next stage is performing this carries the pervious stage residue and makes the hardware ready to fetch on the next sample. The structure of ADC is modified through a technique of pipeline which greatly reduces architectural efforts. The multistep ADC circuit complexity will increase exponentially where as the pipeline ADCs complexity increases linearly. The bits are converted and transferred to the next stage where each stage decides number of bits as a residue and converted into next level of bits.

There are many sources of errors in pipeline ADC to least a few ADC resolution, DAC resolution, inaccurate settling of the opamp, and gain error. High throughput is one the major significance in pipeline converter. After every clock cycle the output is generated with a minimum latency. As the bit length increases the circuit complexity also increases equivalently, extra stages will be added as the bit length increases. The error must be eliminated in the first stage itself or else the error will amplify as it moves on to the next level.

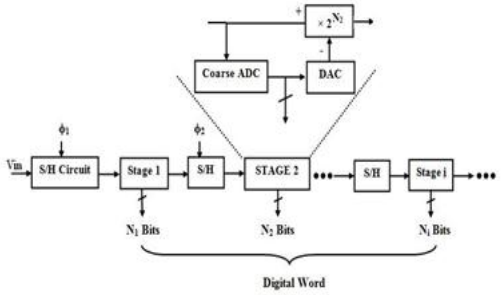

Figure 6: Architecture of Pipelined ADC

F. Cyclic Or Recursive Adc

Cyclic or recursive ADC is quite different from the pipeline ADC in such a way that it uses repeated same stages results in minimum utilization of hardware components. In the beginning ADC converts the sampled inputs into N_1 bits during Φ_1 phase. The remaining bits are passed to sample and hold circuit at phase Φ_2. Once the first stage is completed the position of the switch is changed from '1' to '2' then it takes N_2 bits for the conversion. The architecture of cyclic or recursive ADC as shown in figure 7.

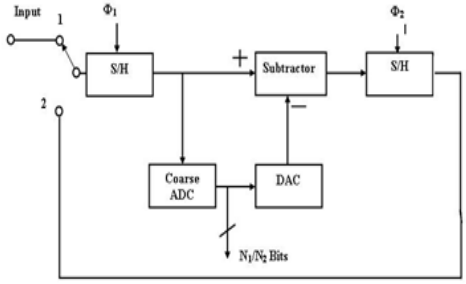

Figure 7: Architecture of Cyclic or Recursive ADC

It converts all the bits with a carry of residue factor. Due to cyclic method hardware utilization is reduced on the other hand increased the time of conversion.

V. SYSTEM COMPONENTS

A. Sample And Hold Circuits

Sample and hold circuit is one the significant block in an A/D converter. The charging of capacitor is kept constant in hold mode and releases during the sampling mode to complete the conversion.

Track and hold circuit comes into picture because analog input will vary during sampling period. Hold mode maintained the track value of the analog input at the time of sampling and the same as shown in figure 8. (a) and (b)

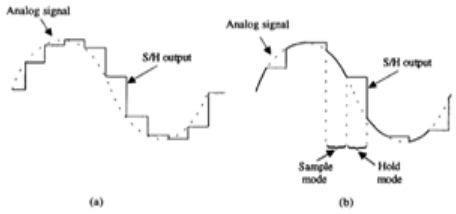

Figure 8: (a) Sample and Hold circuit output (b) Track and Hold circuit

B. Comparator

Comparators are one of the significant blocks in the A/D converter and are classified into static and dynamic comparators.

The comparators produces logic '1' when $V_{IN}+ < V_{IN}-$ else it gives logic '0'. An output buffer, preamplifier and a decision making circuit are the three inbuilt blocks in a static comparators.

Comparator design [21] in sub ADCs becomes easier when error correction techniques are considered in the design. The power consumption is reduced in pipeline ADC though the dynamic comparators will exhibits high offset and then digital error correction is used the remove the error.

Comparators are known as 1-bit ADCs and for that reason they are mostly used in large abundance in ADC. In the ADC process, it is necessary to first sample the input. This sampled signal is then applied to a combination of comparators to determine the digital equivalent of the analog signal. The decision making time in the comparator which affects the process of conversion speed. The condition is determined whether the sampled input is smaller or greater than zero by the CMOS comparator. This result to compare between reference and input signal depending on the comparison.

C. Digital To Analog Converter

The structure of ADC consists of Digital to Analog Converters (DAC) for the conversion logic. A typical schematic of DAC as shown in Figure 9.

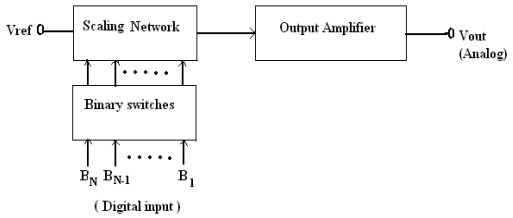

Figure 9: A typical schematic of DAC

Various combinations of scaling network components of V_{REF} are connected to the switch and it is controlled by digital binary input. The voltage signal is received from output amplifier after conversion from input signal, which is not affected for the scaling network. DAC shows the various architecture. The different types of DAC architectures are current steering DACs, charge scaling DACs and voltage scaling DACs.

The design of sub-converter is very difficult to achieve the desired accuracy in D/A conversion. A comparator is treated as 1-bit DAC and without using an opamp a 2-bit ADC can be implemented. In an R-2R ladder networks different resolution of DACs are implemented and ADC will have DAC structure as a part of sub conversion.

D. Residue Amplifier

The residue amplifier [19]-[21] in pipeline ADC consists of one key block the residue amplifier. These residue amplifier blocks are then connected in series, forming a pipeline. Figure 17 below shows a block diagram of the residue amplifier. The amplifier compares the analog input, V_{in}, to a reference voltage and then generates two outputs. The digital output, D[n], represents the n^{th} data bit of the ADC. R(n) is an analog signal representing the scaled residue or scaled remainder of the signal after comparison. This can be represented with the following mathematical model.

$$D[n] = \begin{pmatrix} 0, & V_{in} < V_{ref} \\ V_{DD}, & V_{in}\, V_{ref} \end{pmatrix} \quad R(n)$$

$$= 2 * V_{in} + D[n] \quad \ldots\ldots\ldots \quad 17$$

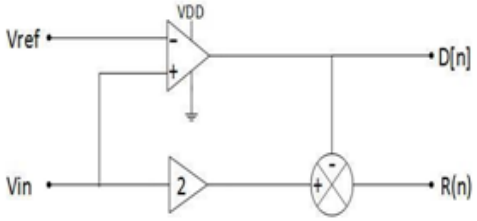

Figure 10: Residue amplifier block diagram

If set = 2, the data bit, D[n], represents the most significant bit of the ADC conversion. The input-output characteristics for V_{DD} = 5V and V_{REF} = 2.5V. The data bit goes "high" when the input is greater than the reference. More importantly, if it look at the residue signal, it can see that it would generate the next less significant bit of data if it onto pass it into another comparator. In this way, it can chain together several of these residue amplifier stages to generate a multi-bit ADC conversion.

Table 1: Comparison of different ADC architectures

Sl. No.	**References/ Parameters**	Ref [1]	Ref [2]	Ref [3]	Ref [4]	Ref [5]	Ref [6]	Ref [7]	Ref [8]	Ref [9]
1	**ADC Architectures**	CD pipelined ADC	Pipelined/SAR	TB ADC	Ring amplifier Pipelined	Pipeline-SAR	Zero-Crossing-Based Pipeline ADC	Pipelined-SAR	PN calibration techniqu e	zero-crossing-based pipeline ADC
2	**CMOS Technology[nm]**	180	65	65	28	65	65	65	180	130
3	**Resolution(bits)**	12	11	8	12	10	9	11	12	10
4	**Speed of Conversion rate/Sampling rate(sps)**	250M	1G	1.1G	1G	500M	1GHz	450M	250M	200M
5	**INLE/ DNLE(LSB)**	0.45/1.7	0.8/0.7	0.9/0.7	1.14/1.85	1.7/0.6	18.0/9.87	0.7/0.4	0.6/0.25	-0.47/0.83
6	**SNDR(dB)**	65.3	55.9	43.3	57.1	52.8	47.26	60.8	69.92	53
7	**SFDR(dB)**	78.1	60.05	51.6	74.6		62.64		81.17	63
8	**FoMfJ/conv.step**	237	449.2	32	45	46	246.5	21	864	552
9	**Power(mW)**	85	230	3.5	24.8	8.2	46.52	7.4	395	38
10	**Area(mm^2)**	2.24	2.5	0.029	0.54	0.046	0.313	0.07	2.5	0.7

VI. COMPARISON

The table gives the detail analysis of various pipeline ADC architecture. For the comparison major parameters like technology on which the design is implemented, number of bits, INL/DNL and speed of conversion are considered. The design is mainly targeted on the Electronic design automation platform implementation so the VLSI constraints like power, area and speed of conversion in terms of Msps(Mega samples per second) are taken to reference for the discussion.

It is observed that the technologies and resolution makes greater impact on the conversion speed. As the resolution increases the power and area increases proportionately. Ideal parameter of ADC converter for pipeline type is considered and actual non-idealities are compared.

This clearly shows that as the bits/resolution and technology of implementation increases the speed of conversion also increases equivalently.

VII. CONCLUSION

A brief description of various ADC architectures has been presented including flash, multistep, successive approximation, dual slope, pipelined, cycle or recursive ADCs. The performances and limitations of the various ADC architectures are summarized in this review. The various parameters of ADC design are analyzed with respect to the existing work done and the observations are drawn. It shows that technology and conversions are increases proportionally.

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